PROJECTE FINAL DE CARRERA

Development and implementation of a contactless inductive power transfer Qi compliant system.

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Resum del projecte

La transferència d'energia sense fils es una tecnologia emergent que ha atret molt d'interès en el mercat electrònic actual, i la seva contribució jugarà un paper molt important en un futur pròxim gràcies a la seva àmplia varietat de camps d'aplicació i les seves interessants característiques. Mitjançant l'ús d'aquesta tecnologia es permet la carregar de bateries en diferents aparells electrònics; com els de consum, en implants mèdics, en robots, en automòbils, sense la necessitat de cablejats o connexions físiques.

El principal inconvenient dels sistemes de transferència sense fils es la relativa poca eficiència, inferior al 70 %, principalment degut a les pèrdues en la conversió de corrent alterna a corrent continua en el receptor. Per la seva simplicitat i baix cost, aquesta conversió d'energia típicament s'ha realitzat mitjançant un pont rectificador, per la qual cosa fa reduir l'eficiència per la caiguda de voltatge en els díodes. El principal objectiu d'aquest projecte és el desenvolupament d'un prototip receptor de transferència d'energia sense fils amb components discrets compatible amb l'estàndard Q_i canviant els díodes per transistors d'efecte de camp, i implementar un control de commutació per aquests que millori l'eficiència del rectificador i el faci un sistema més factible. També s'ha desenvolupat el transmissor basat en l'estàndard Q_i per analitzar tot el sistema i estudiar el seu comportament. Per això, s'han realitzat transferències d'energia mitjançant acoblament inductiu de baixa (5 W) i mitjana potencia (15 W) reproduint les tècniques de l'estat de l'art per al control del rectificador.

S'han implementat 2 controls per a la commutació dels transistors de potencia del rectificador; basats en la detecció de creuament per zero de la corrent i la detecció de creuament per zero del voltatge d'entrada del rectificador. Aquests transistors són controlats amb l'ajuda d'una FPGA. Diferents mesures experimentals comparen el rectificador tradicional, amb el mètode implementat, obtenint millores d'eficiència del 68 % al 83 % per 5 W de potència de sortida. Inclús millors eficiències es poden obtenir, per sobre de 90 %, per a més baixa potència (1 a 2 W).

Paraules clau: Inducció magnètica, Rectificador actiu, Rectificador síncron, Estàndard Q_i, Prototip de transmissió d'energia sense fils.

Resumen del proyecto

La transferencia inalámbrica de energía es una tecnología emergente que ha atraído mucho interés en el actual mercado electrónico, y desempeñará en un futuro próximo, un papel importante debido a su gran variedad de campos de aplicación i sus interesantes características. Mediante el uso de esta tecnología es posible la carga de baterías en diferentes dispositivos electrónicos; como los de consumo, en implantes médicos, en robots, en automóviles, sin la necesidad de cableados u otra conexiones física.

El principal inconveniente de los sistemas inalámbricos de energía es su relativa poca eficiencia, inferior al 70 %, principalmente debido a las pérdidas en la conversión de corriente alterna a corriente continua en el receptor. Por su simplicidad y bajo coste, esta conversión de energía típicamente se ha realizado mediante un puente rectificado, por lo que se reduce la eficiencia por la caída de voltaje en los diodos. El principal objetivo de este proyecto es el desarrollo de un prototipo receptor de transferencia inalámbrica de energía con componentes discretos compatible con el estándar Q_i remplazando los diodos por transistores de efecto de campo, e implementar un control de conmutación para estos que mejore la eficiencia del rectificador y lo haga un sistema más factible. También se ha desarrollado el transmisor basado en el estándar Q_i para analizar todo el conjunto del sistema y estudiar su comportamiento. Para esto, se han realizado transferencias de energía mediante acoplamiento inductivo de baja (5 W) y mediana potencia (15 W) reproduciendo las técnicas del estado del arte para el control del rectificador.

Se han implementado 2 controles para la conmutación de los transistores de potencia del rectificador; basados en la detección de paso por cero de la corriente y la detección de paso por cero del voltaje de entrada del rectificador. Estos transistores son controlados con la ayuda de una FPGA. Diferentes medidas experimentales comparan el rectificador tradicional, con el método implementado, obteniendo mejoras en la eficiencia de 68 % a 83 % para 5 W de potencia de salida. Incluso mejores eficiencias se pueden obtener, por sobre de 90 %, para baja potencia (1 a 2 W).

Descriptores: Inducción magnética, Rectificador activo, Rectificador síncrono, Estándar Q_i, Prototipo de transmisión inalámbrica de energía.

Abstract

Wireless Power Transfer (WPT) is an emerging technology which has attracted a lot of attention in the current electronic market and its contribution is going to play an important role it in the near future thanks to its wide variety of applications fields and to its interesting features. Ranging from consumer electronics to medical implants devices to robotics to automotive applications, this technology it is used to charge the battery of these devices without wiring connections.

The major drawback of currently available wireless power systems is the relatively low efficiency (<70%) mainly because of the receiver AC-DC power conversion. This power conversion has been typically performed with a bridge rectifier because of its simplicity and low cost, but with considerable power losses because of the diodes voltage drop. The main target of this project is to develop a WPT receiver prototype with discrete hardware compliant to the Qi standard replacing these diodes by MOSFET transistors and implementing a switching control for them which increases the efficiency of the rectifier and makes the system reliable. The transmitter is also developed to analyze the whole WPT system and study its behaviour. Therefore, a contactless inductive power transfer is implemented for low (5W) and medium power (15 W) to reproduce the most recent rectifier techniques of the state of art.

Two different rectifier control approaches has been performed based on the Zero-crossing Voltage Detection (ZVD) and the Zero-crossing Current Detection (ZCD) methods. With the help of a FPGA the rectifier power switches are controlled using the ZVD and ZCD information. Several experimental results compares the traditional simple rectifier, with the method implemented, showing increasing efficiencies from 68 % up to 83 % for 5 W output power. An even higher efficiencies (over 90 %) for low output power [1 - 2 W].

Keywords: Wireless prototype, Magnetic induction, Active rectifier, Synchronous rectifier, Q_i standard, Wireless energy transmission, Contactless inductive energy transmission.

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1. CHAPTER I: Introduction

1.1. Context of the project

Since the discovering of electromagnetic waves a technological race began to take advantage of transferring information wirelessly; radio, television, cellular phones, RFID, etc. as an example. Nowadays the needs has been increased and this concept has evolved not just to transfer information whereas to transfer amounts of power efficiently. This technology, which is not new at all, is being called wireless power transfer (WPT[1]). By definition wireless power or wireless energy transmission is the transmission of electrical energy from a power source to an electrical load without man-made conductors.

The father of this technology was Dr. Nicola Tesla who experimented for the first time in the 1880s with the wireless transmission of energy based on two loop resonators [Fig. 1]; the transmitter loop resonator and the receiver loop resonator. As he pioneered, wireless power transfer can be radiative or non-radiative depending on the energy transfer mechanisms.

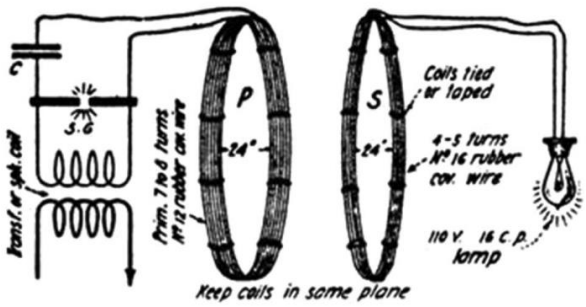


Fig. 1: A diagram of one of Tesla's wireless power experiments [1]

Radiative power relies on the emission of power from an antenna over long distance (much larger than the dimension of the antenna) in form of electromagnetic wave. Since power is emitted omnidirectional the efficiency of this technology is very low. On the other hand, non-radiative wireless power transfer depends on the near-field magnetic coupling of conductive loops which can operate with much efficiency. Depending on the application range they can

[1] Apart from this terminology (WPT), there are other terms describing the same phenomenon. Some of these terms are contactless energy transfer (CET), contactless inductive energy transfer (CIET), contactless inductive power transfer (CIPT), inductive power transfer (IPT), contactless power transfer (CPT).

be classified as short-range (few cm) and mid-range applications (up to few meters). In this project, short-range non-radiative technology is studied and WPT specifically refers to transfer of electric power between two isolated electric circuits by means of magnetic induction. The distance of isolation along the energy is transferred is of order of the dimension (such as the radius or the diameter) of the coupled coils

In our days non-radiative WPT technologies are becoming an important field of study and research because of its multiple advantages and range of applications [Fig. 2], especially in consumer electronic devices. The main intention behind WPT is to use the energy transmitted to charge the device target battery, i.e. at the wireless receiver output a DC-DC converter operating as a charger is connected. Some of the advantages [2] of this technology allows to:

- Power multiple portable devices at the same time from one socket, avoiding multiple wire connections.
- Make devices safer by eliminating the sparking hazard associated with conductive interconnections.
- Make devices more reliable by eliminating the most failure prone component in most electronic systems, the cables and connectors.
- Bio-medical application more feasible.
- Make the device truly waterproof.
- Make devices more convenient.

However, there are some drawbacks [2]:

- Less efficient than wired charging. Current inductive charging systems are not quite as efficient as charging with a cable.
- Nowadays there is a lack of united standard specifications for WPT.
- Less flexibility when charging. Electronic devices being charged wirelessly have to be left in one place or the charging process will be interrupted (the induction coils need to be close together for the system to work), specially in magnetic induction technology.

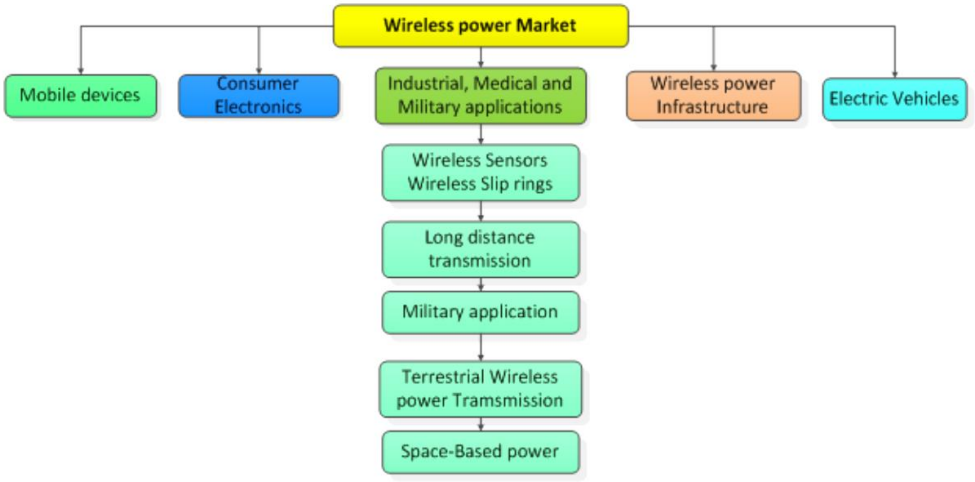


Fig. 2: Wireless power market. Source [3]

1.2. Goals and objectives

The main goal of this project is to demonstrate WPT as a feasible technology for charging applications and to understand the effects and the implications of such technology. The principal objective is to develop a wireless power transfer prototype with discrete hardware compliant to the Qi standard implementing new rectifier control techniques at the receiver to optimize the efficiency of the bridge rectifiers based on diodes. Power transmitter design it is intended to be fully compliant with the standard in order to provide consistent power and voltage levels to the power receiver, consequently less flexible and limited in terms of design. On the other hand, much more freedom is possible to the power receiver. From the simulation and the experimental results obtained from the wireless receiver prototype the plan is to implement posteriorly an IC.

Since the intention is to develop a WPT prototype focusing on the power receiver performance, the communication between transmitter and receiver, typical in WPT systems, is it out of scope and is not programmed. That is, no receiver detection is implemented and the transmitter is always sending power whether there is a power receiver detected or not (no standby power).The purpose of the WPT prototype is to view its behaviour and perform several measurements to check:

- The resonance frequency
- Efficiency vs output power
- Rectifier control techniques
- Coupling factor
- The system behaviour when a DC-DC charger is connected to the output.

2. CHAPTER II: Background

2.1. Wireless Power Transfer Technologies

Nowadays several wireless power transfer technologies exist and they can be classified in terms of frequency, distance or power transferred. Their common aim is to guarantee that the maximum power emitted is received, namely to have the best efficiency in order to make the system economical. This characteristic differs from the wireless telecommunications systems where the proportion of energy received becomes critical only if it is too low for the signal to be distinguished from the background noise [4]. In thus applications the energy transferred it is just small amounts of power (several mil-watts), enough for exchanging information. Depending on the WPT technology is possible to transmit up to tens of W, tens of kW or even tens of MW of power (not implemented yet) [2].

Basically, there are 2 different methods of wireless energy transmission defined by the physical phenomena of electromagnetic field propagation: near-field and far-field [Fig. 3].

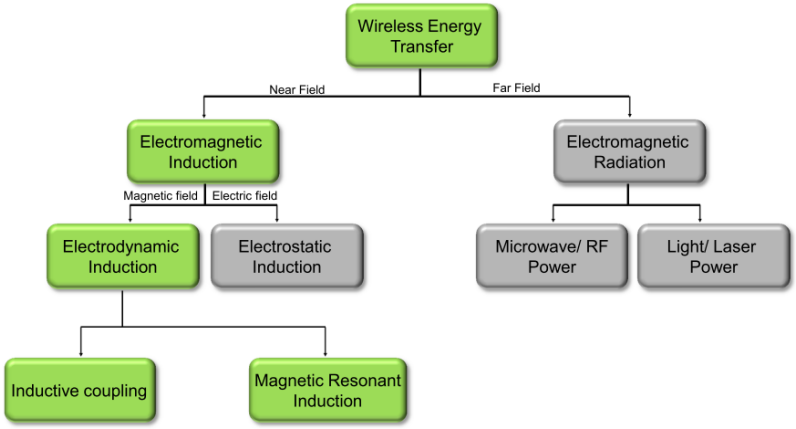


Fig. 3: Classification block diagram of the main energy transfer technologies

A summary of the existing technologies features is shown in Table 1. For all these technologies it is still not known which solution will be adopted for the future development, but if the highest levels of power should be transferred then the directional (beam) methods are more likely to be used (microwave power transmission). This method is capable to transport energy in gigawatts power levels. Anyway, each technology has its range of

application and most of them may be used in the near-future. In this project the technology used is the inductive coupling.

	Inductive coupling	Magnetic resonance coupling	Capacitive coupling	Microwave power transmission	Laser
Received power	several W to hundreds of kW	hundreds of W	up to 1 W	up to tens of kW	expected MW
Operating distance	up to several cm	up to several m	up to several mm	up to tens of km	up to tens of km
Operating frequency	several kHz to tens of kHz	several MHz	up to MHz	up to 300 GHz	Higher than 1 THz
Convenience	acceptable level	high level	acceptable level	high level	high level
Efficiency	highest	high	low	medium	medium
Biological Impact	minor	medium	minor	significant	significant

Table 1: Comparison of the existing methods. Source [5]

2.1.1. Near Fields Methods

Near-field transmissions involve non-radiative application to transport energy across relatively short distances, (usually much lower than 1 meter, exceptionally reaching up to a few meters).

2.1.1.1. Introduction to inductive coupling and resonance magnetic coupling

It is not immediately to distinct both technologies, some literature differs this two types of theories in terms of resonance but in the end they both are using a resonance circuit and they are coming from the same principle, based on the magnetic induction. Each one is referred to a certain WPT standard; Qi and PMA for the inductive coupling and A4WP for the resonance [see chapter 2.4 - WPT Standards]. Anyway they can be distinct in terms of frequency operation, design architecture, and application distance range.

The principle of the inductive coupling and the resonance magnetic coupling technologies consist in passing an alternating current through a coil (the transmitter or the primary coil) in order to generate a magnetic field that will induce a voltage to another one (the receiver coil or the secondary coil) [Fig. 4]. Therefore an electric current will be generated in the receiver coil which can be used to power a low-power device (several W) or charge a battery.

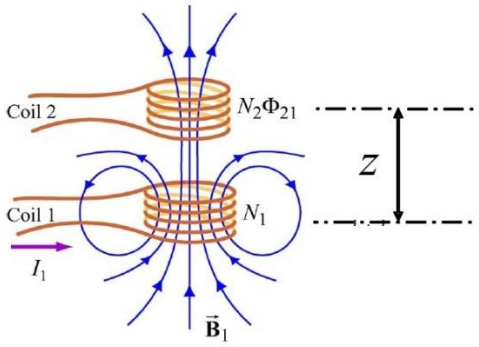


Fig. 4: Magnetic coupling with transmitter coil (1) and receiver (2) coils separated by a distance z

This mechanism of induction also exists in the typical transformers. However, in a transformer the magnetic field is confined to a high permeability core whereas in contactless inductive power transfer it simply flows in the air. Consequently the non-resonant induction method is limited to short range (few cm) because over greater distances is inefficient and wastes much of the transmitted energy just to increase range. An exponential decay of the power transfer efficiency over distance is shown in Fig. 5.

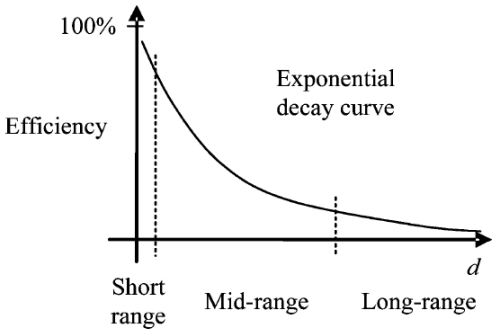


Fig. 5: Magnetic induction system efficiency versus distance

To enhance the power transfer capability, the coupled coils generally need to be compensated capacitively to obtain the current magnification resulting from the resonance effect. Capacitive compensation is crucial to the implementations of these applications; therefore a resonance circuit is added. The use of resonant frequency is to compensate the leakage impedance of the power flow path [6].

In inductive coupling or magnetic induction technology (MI) a resonance circuit is added to operate between a certain frequencies ranges close to the resonant frequency. In contrast, in the resonance magnetic technology (MR) is based on the same frequency of resonance on

both sides to transmit energy to longer distances. In MR two resonant loops oscillate in the same frequency tunneling the energy which is reached by the receiver.
Since the electromagnetic waves are tunneled, they do not propagate through the air to be absorbed or be dissipated, and do not disrupt electronic devices or cause physical injury if no system or human body is placed between.

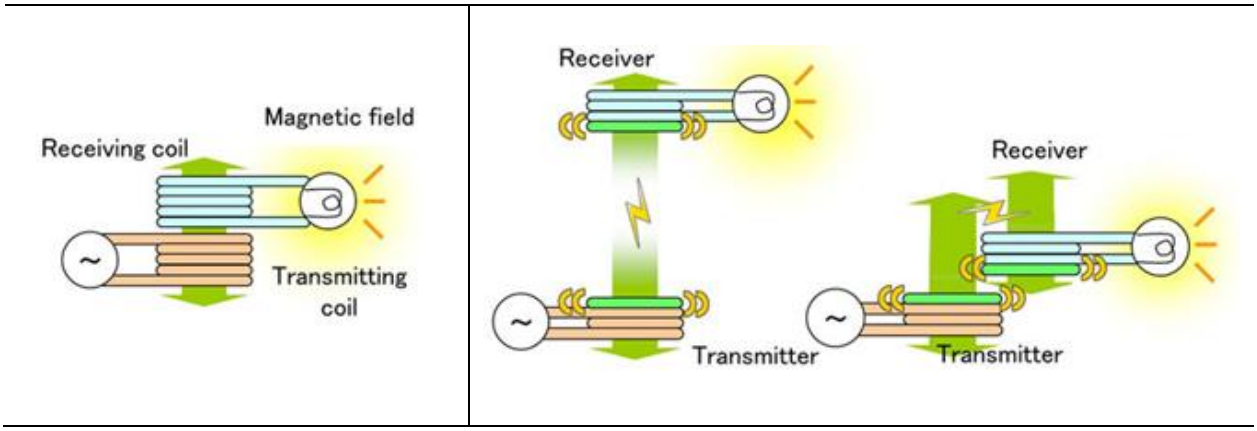


Fig. 6: The electromagnetic induction method operates based on the electromagnetic force that arises between coils in the presence of magnetic flux (left) . The magnetic resonance method: uses coils as resonators and uses magnetic resonance to send electrical power (right)

2.1.1.2. Magnetic induction (MI) and magnetic resonance (MR) architecture

Development of high performance power management architectures has a big impact in the implementation of successful MI and MR solutions. Both technologies have similar structures but the design complexity in magnetic resonance systems is much higher, see Fig. 7 and Fig. 8. The architecture of a MI and MR system can be divided by the three blocks: the transmitter block which is responsible of the conversion of the DC input voltage to AC, the coupling structure which is the link of the energy transferred, and the receiver which receives the energy coming from the transmitter and converts it again to DC power.

Differences in both technologies are presented in each block. The power conversion unit from DC to AC which takes places on the transmitter side, in MI is done by a simple half bridge or a full bridge inverter whereas in MR current is induced through a power amplifier. Power amplifier architecture and classification can vary based on the frequency, standby current, efficiency, size, and integration requirement of the application.

Concerning the coupling structure in MI technology is used small precise inductor coils which make it easy to transfer high power over higher frequencies, i.e. the coupling is tight. On the other hand in MR, rather than the small inductor coils, opts for a larger and more

powerful electromagnetic field generated from a much larger coil. This accomplishes a much larger distance range by using a finely tuned resonance circuit to induce a current in the receiving device. In this case the coupling is it referred as loosely coupling.

At the receiver side differences between MI and MR are related on the type of the rectifier employed.

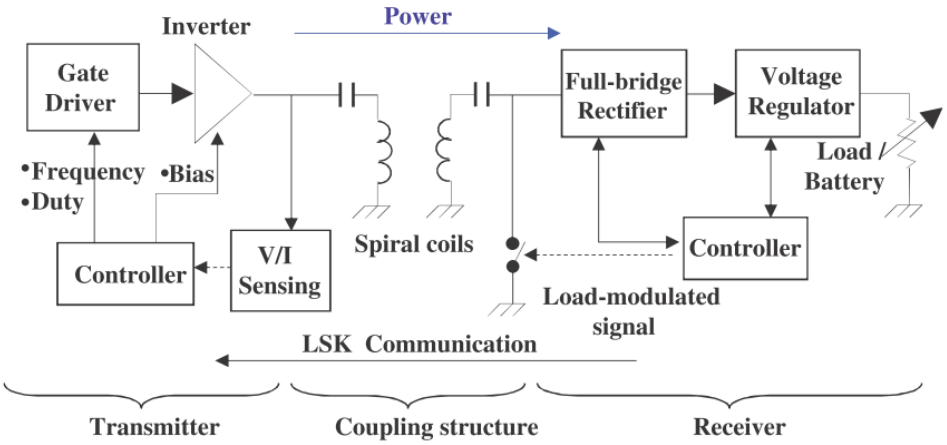


Fig. 7: Magnetic induction WPT system with tightly coupled coils and a varying load

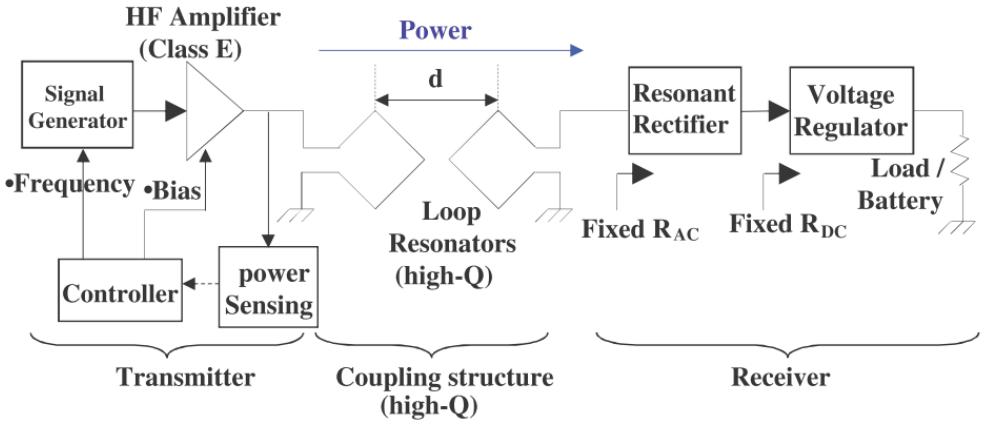


Fig. 8: Resonant WPT system with two high-Q loop resonators with a fixed load

2.1.1.3. Critical review between MI and MR

Both technologies are strongly competing to jump to the to the consumer electronic market; especially for smart phones, tablets, etc. They both have advantages and disadvantages. One important advantage of MI over MR, as it has been presented, is its easy implementation and high efficiency in close transmission. Besides its simple HW architecture comparing to MR,

also the regulation control it is not as complex. Self-inductances of both sides are increased considerably when the distance between them is reduced to few mm (less than 10) because of the mutual inductance. This provokes that the resonant frequency is shifted. In MI technologies where the power can be transferred over a wide range of frequencies this is not a problem but for MR a special control has to be implemented to match impedances.

A particular attention in order to maintain high efficiency in MI systems is to keep the primary and the secondary coils perfectly aligned. The use of magnets within the coils can help to avoid misalignments. Another techniques implies to use multiple tightly couple resonator arrays in order to create a larger charging area [7]. However it obviously consumes a lot more power to have the entire matrix of individual coils switched on.

It is still not known which technology would be the most effective way of charging, but seems that will depend on the application, i.e. each one will be suitable for a specific purpose. For example MR systems are able to transfer higher power for a longer distances but this may increase problems. Since the electromagnetic waves are tunnelled, they do not propagate through the air to be absorbed or be dissipated, and do not disrupt electronic devices or cause physical injury if no system or human body is placed between. However, MR operates at higher frequencies because it is difficult to realize high-Q resonant coils with dimensions feasible for consumer electronic devices; meaning a higher impact and risk to affect the human body [8]. Therefore some may limit the power and range of a product utilizing this technology.

2.1.1.4. Electrostatic induction technique (capacitive coupling)

The idea of capacitive coupling was patented by A. Rozin in 1998. Capacitive coupling is the transfer of energy between two electronic circuits due to mutual capacitance between them. The power is transmitted between metallic plates (thus forming one or more capacitors) by the oscillation of a high-frequency electric field (MHz). At the receiver side, the device or the battery is supplied by the transported high frequency capacitive current after a rectification process. Unfortunately, to obtain a reasonable power levels this electric field must achieve too high intensity and the surface must be considerable, this fact limits possible applications.

The main advantage of capacitive charging is that energy can be transferred through metal, while the inductive charging will induce flowing current in metal. The efficiency of this method is limited by the distance between the transmitter and receiver plates (i.e. the capacitance). This technique is applicable in sensor supply systems, smart card equipment or in small robots.

2.1.2. Far Field Methods

Far-field electromagnetic transmission methods permit long-range power transfers and typically involve beamed electromagnetic power (lasers, microwave). Since the project is not concentrated in these methods a brief overview is given.

2.1.2.1. Microwave power transmission

Microwaves are a part of the electromagnetic radiation which occupies the higher frequencies at 300 MHz to 3 GHz of the RF. Besides power transmission, they are typical used in wider applications like heating and high-bandwidth data transmission systems. In this technology power is transmitted by a microwave energy beam. It consists of a combination of a rectifying circuit and an antenna, called rectenna. The antenna receives the electromagnetic power and the rectifying circuit converts it to DC electric power. The amount of power that can be transferred is limited. For safety reasons, the transmitted power is limited by regulations, for instance by the Federal Communications Commission (FCC).

One possible application of the Wireless Power Transmission via microwave electromagnetic emission is the Solar Power Stations. It consist in placing large solar panel cells on a geostationary orbit to collect and convert sunlight into microwaves, beamed afterwards to a large antenna on the Earth, to be converted into conventional electrical power [Fig. 9]. Because of the technological difficulties and the increasing health and safety risks it has not yet been implemented, even though several projects and plans are already being studied [9].

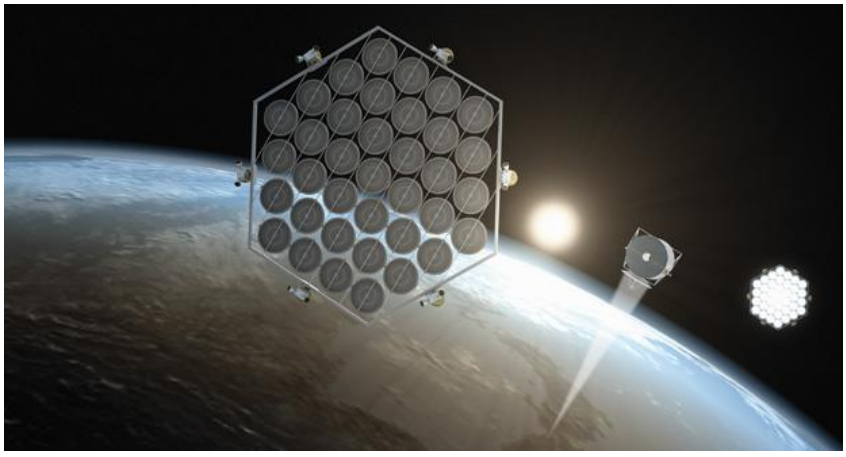


Fig. 9: Project of the solar energy reception from the space by rectennas. Extract from [9]

2.1.2.2. Laser beamed power transmission

In contrast to the previous technology explained where the power transmission was done by a microwave energy beam, in this case a laser beam it is used. Once the electricity is converted into a Laser beam the energy is transferred pointing the beam itself towards a photovoltaic cell receiver, which in turn converts the received light energy back into electricity.

Laser is ideal for power transmission at a distance: it provides a coherent, almost non divergent beam with high energy density, thus allowing smaller diameter of the antenna. Unfortunately, certain disadvantages reduce the benefit of laser: the imperfection of existing technologies leads to the loss of the most of energy during the transformation of the laser beam into electric power. Before making the method effective, more efficient solar cells must be developed. Another significant drawback of laser is safety: the danger of hitting any object in the area of the beam. On the other hand, laser energy transmission allows much higher energy densities, a narrower focus of the beam and smaller emission and receiver diameters in comparison with microwave energy transmission.

Laser beaming is already used successfully in models and prototypes developed by specialized companies, e.g. Laser Motive. This Seattle-based company developed a space elevator prototype supplied by a laser beam (about 1 kW) to lift 50 kg (Fig. 10).

Fig. 10: Prototype of space elevator (LaserMotive)

2.2. State of the art of WPT based on electromagnetic induction

The first industrial application appears in the 1990s with the electric toothbrushes. Since the creation of the Wireless Power Consortium (WPC) [10] in 2008 among other consortiums and alliances, the WPT technology has been standardized and several products are showing to the current electronic market. WPC launched the world's first Wireless Standard ''Qi'' in 2010 for wireless charging of portable electronic devices up to 5 W.

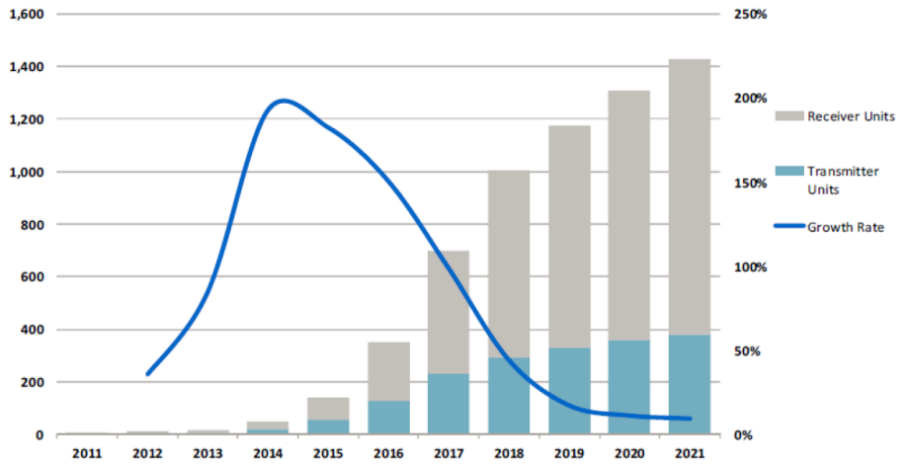


Fig. 11: Current Growth Projection for Wireless Power Market. Source [11]

The wide applications of WPT technology is pointing to a promising future [Fig. 11]. IMS research predicts a grown of receiver units almost 50 % by each year. Some companies have already come up with innovative solutions of powering or charging consumer electronic devices using. The concept is to wireless charging of mobile electronics like cellphones, laptops etc., and direct wireless powering of stationary devices like TV's, desktop PCs, speakers, kitchen appliances, etc. But most of these applications are still being studied. Besides consumer electronic devices WPT has also an area of application in bio-medical. Direct wireless power interconnections and automatic wireless charging for implantable medical devices like ventricular assist devices, pacemakers, defibrillators etc. is being researched. Fig. 12 shows some of the wireless powering and charging solution existing in the market or being introduced in the market in near future.

Fig. 12: Top left) Sonicare Philips toothbrush mounted on a charger. Top right) Inductive Power Transfer wireless charging used in Turin buses [12] . Below left) A tether-free Left Ventricular Assist Device (LVAD) [13]. Below right) Qi Wireless Charger Station

2.3. State of art of synchronous rectifiers

The aim of this project is to improve the efficiency of the power receiver, and therefore the state of art of WPT receiver techniques is analysed. As it is explained in the next chapters, the main power losses of the power receiver are present in the rectifier. Various publications regarding optimum controls of the rectifier are studied to overdue this problem:

- Active Rectifier with dual back telemetry [14].
- Integrated synchronous rectifier adopting a high speed comparator [15].
- Simple synchronous rectifier with a simple control scheme [16].

The implementation presented in article [14] is intended to use in RFID application but the rectifier structure can also be employed in wireless power receivers. The rectifier structure consist of two low-side NMOS switches which are self-driven by the rectifier input waveform, and two upper PMOS switches which are driven based on the comparison of the body diode voltage between the input and the output [Fig. 13]. This comparison may give unpredictable result at the start-up because of the very low output voltage. To avoid this problem P_3 and P_4

switches are turned on to generate a temporary stable supply for the output voltage till it stabilizes.

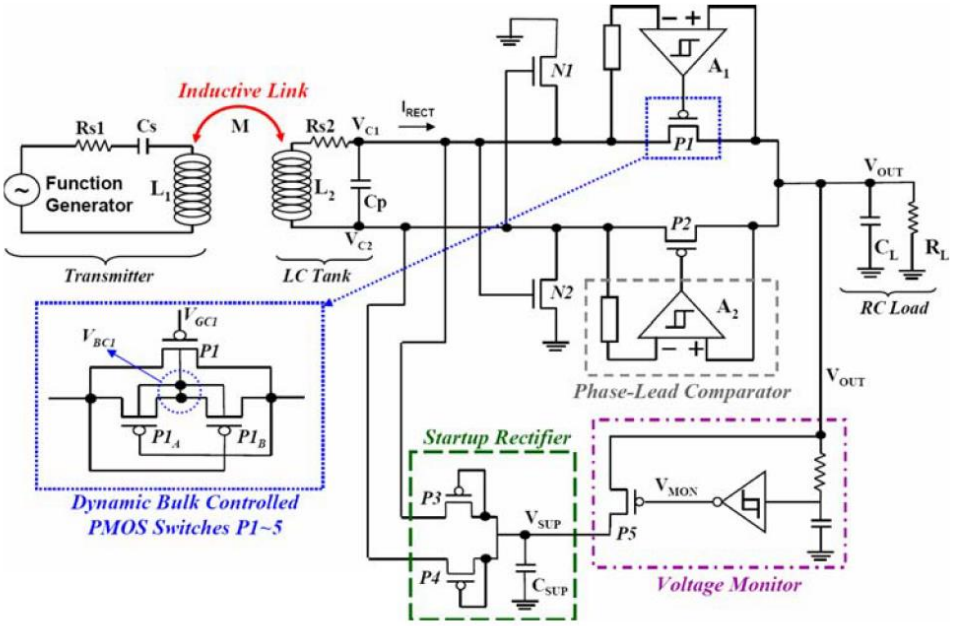


Fig. 13: Complete power transmission schematic incluiding the rectifier structure proposed in [14]

The proposed integrated prototype can reach efficiencies up to 84'4 % when 20 mW are transferred.

- Integrated synchronous rectifier adopting a high speed comparator [15].

The proposed rectifier architecture [Fig. 14] consists in sensing the rectifier input voltage with two high speed comparators in order to drive the low-side NMOS switches. Upper PMOS switches are self-driven with the quasi square waveform of the rectifier input. The high speed comparators permit to minimize the turn on/off delay of power transistors that can cause leakage problems for high operating frequencies (13'56 MHz).

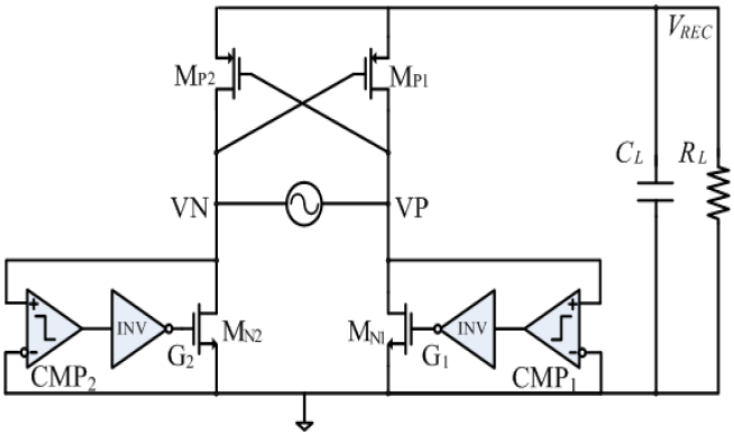


Fig. 14: Architecture of cross-coupled comparator based active rectifier. Extract from [15]

This rectifier structure, which by experimental results with an integrated circuit can achieve power conversion efficiencies up to 92 % when 6'7 mW are transferred, benefits of no need of external control circuitry to drive the switches and no need of power transistor drivers. However, presents problems to power-up and down because the input signal waveform at start-up is too small.

- Simple synchronous rectifier with a simple control scheme [16].

This implementation pretends to overdue the problems of the two last researches commented. On one hand solves the issues off power-up and down of the rectifier [15] and on the other hand reduces the high speed and complexity control of [16]. In contrast with the last articles, this discrete HW prototype is able to transfer higher amounts of power (several W) with efficiency up to 75 % for 5 W, according to the Qi specification.

The rectifier structure is form with the low-side switches M_3 and M_4 (see Fig. 15) , which are cross-connected and self-driven with the input voltage waveform, and the upper PMOS transistors which are controlled based on the low-side control signals, *IN*. The control scheme proposes to turn on simultaneously the two pair of switches (M_1& M_4 or M_2 & M_3) based on the rectifier input waveform and to turn off the upper switches before the low side switches for proper operation. This time which the upper switch is turned off before the low side is calculated with a counter. The counter value is determined by the *IN* signal on time of the previous cycle minus an additional time.

The problem of startup is avoided performing a passive power up, utilizing the body diodes of the MOSFETs. Once the rectified voltage reaches a predetermined value, the control of the rectifier bridge is activated.

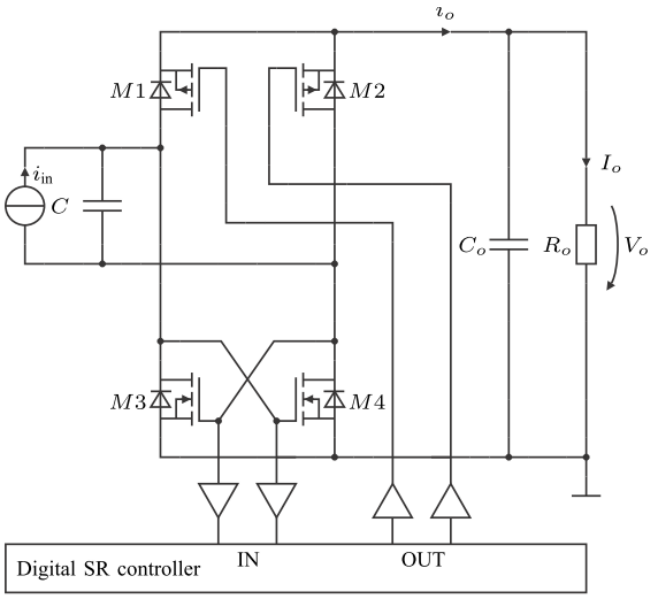


Fig. 15: Proposed full-bridge rectifier in [16]

The efficiency results of this article are compared in chapter 5.3.8 with the experimental results done in the WPT prototype of this project. Also some issues are shown at light loads for operating frequencies close to the resonance that may produce problems to these self-driven rectifier structures.

2.4. WPT Standards

A certain number of organizations and industrial consortia are investing some effort to develop specifications and standards relating to wireless power transfer systems. Nowadays the three most popular alliances which are involved in WPT are: the Wireless Power Consortium (WPC), the Power Matters Alliance (PMA) and the Alliance for Wireless Power (A4WP) [Table 2]. At the time of writing the leading standard at the moment (based on the number of commercially available products) is "Qi" launched by the WPC, now comprising over 203 companies worldwide [10].

	WPC	A4WP	PMA
Full Name	Wireless Power Consortium	Alliance for Wireless Power	Power Matters Alliance
Logo			
Basic Technique	magnetic induction	magnetic resonance	magnetic induction
Member Number	180	100	60
Certified Product	380	0	0
Main Member	Philips, Panasonic & HTC	Qualcomm, Samsung & NXP	BlackBerry, Starbucks & NEC

Table 2: WPT consortium and alliances (January 2014). Source [17]

There are two alliances adopting magnetic induction technique, WPC and PMA. A4WP adopts magnetic resonance.

	Power frequency band	Tightly coupled Tx & Rx	Spatial freedom (x/y/z)
WPC	100 – 205 kHz	Yes (no magnet)	Yes. Adaptive resonance
PMA	277 – 357 kHz [18]	Yes (with magnet)	No
A4WP	6.78 MHz [19]	No	Yes Magnetic resonance

Table 3: WPT standard specifications

3. CHAPTER III: WPT System overview

3.1. Introduction

From now on the WPT is specifically based on Q_i specification. A typical WPT system consist of a base station, i.e. the power transmitter, capable to supply energy to the system wirelessly and the powered device, i.e. the power receiver, which is the one that receipt that energy and converts it, in general, to DC power. Also a complete communication is necessary between both stations for device detection, power saving and amount of energy required to transfer. A complete overview of a WPT system example is shown in Fig. 16.

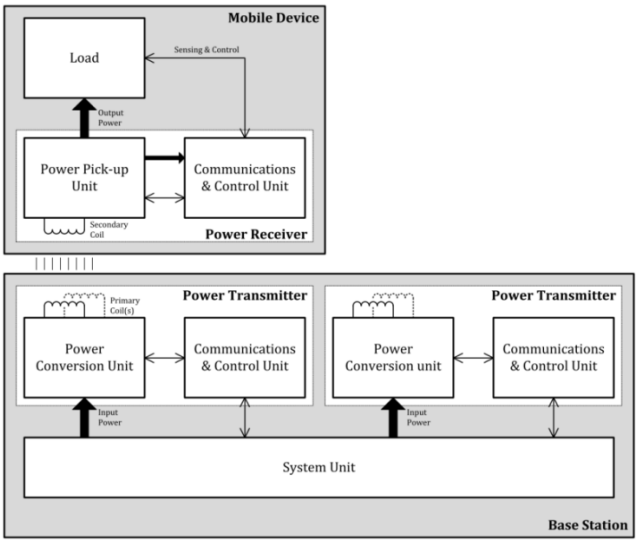


Fig. 16: WPT basic system overview. Source [7]

Besides power conversion and power pick up, a typical WPT system contains a communication between both stations. With this interaction, the power transmitter can detect if a receiver is present, how much power does it require, and when it is fully charged. Consequently the transmitter is not transferring power if the communication with the receiver was not successful or if the receiver does not require energy, which permits a power saving.

In the context of this project, since the main interesting part is to analyse an efficient receiver (transmitter design it is mainly defined following the Qi standard specifications), the wireless communication system between transmitter and receiver is out of the scope. Therefore, it is not implemented and any exchange of information is wired through the FPGA.

Also no power saving it is developed, i.e. the power transmitter is sending power whether there is a receiver or not detected.

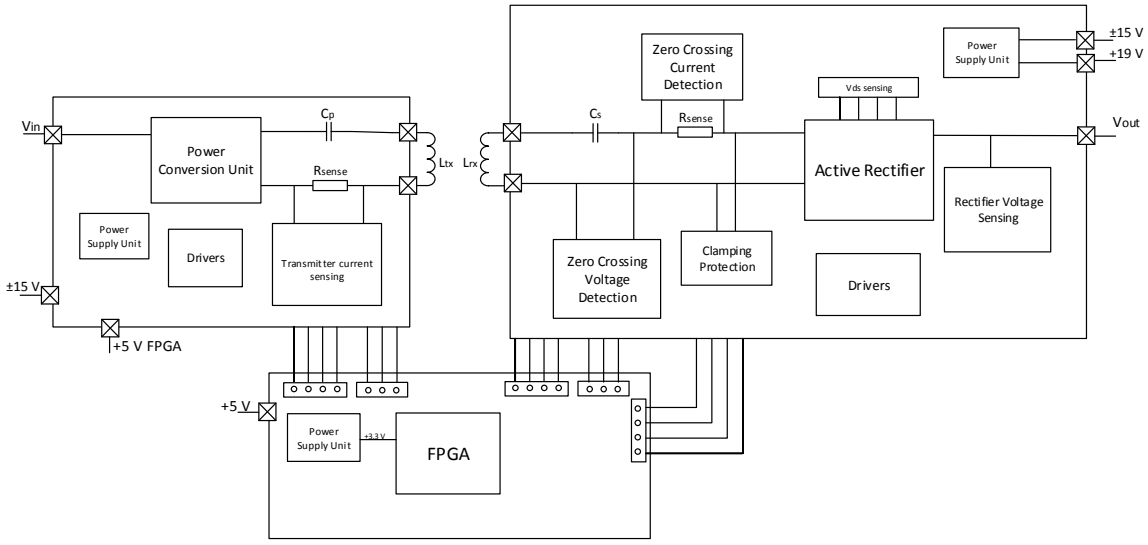


Fig. 17: WPT system implemented (find electric schematic in appendix 8.4 and 8.5)

The system implemented [Fig. 17] consists of a power transmitter PCB [Fig. 18], a power receiver PCB [Fig. 19], a mechanical coil separation equipment [Fig. 20], the transmitter and the receiver coils, and an evaluation FPGA board [Fig. 21].

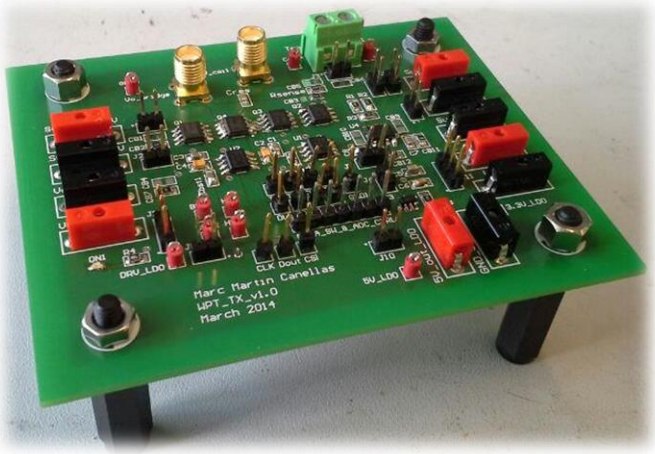


Fig. 18: 2 layer transmitter PCB (see appendix 9.2 for more info regarding PCB spec. and layout)

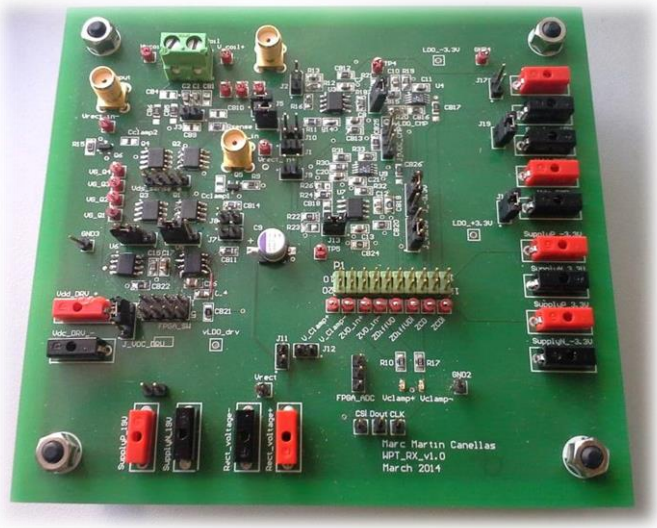


Fig. 19: 2 layer receiver PCB (see appendix 9.2 for more info regarding PCB spec. and layout)

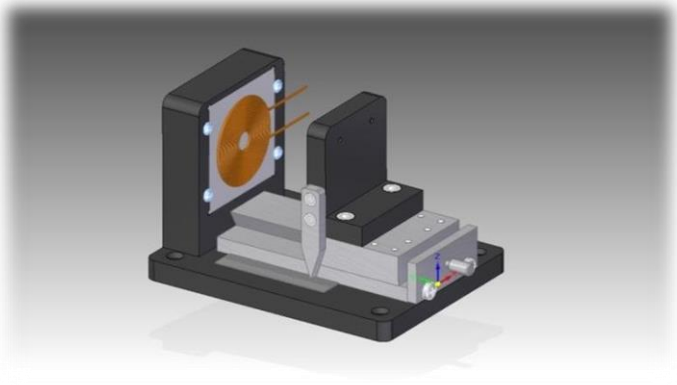


Fig. 20: Mechanical coil separation prototype

The mechanical coil separation equipment accomplishes two functions; on the one hand it permits to accurately separate transmitter and receiver coils to a certain range in order to test the behaviour of the WPT prototype for different distances. And on the other hand, since coils must be proper aligned to transmit power efficiently, see next section, with the equipment they can be fixed for different tests and measurements.

It consists of two vertical platforms where coils are fixed with screws. One of these platforms has been designed to move precisely along the rail (up to 5 cm), with steps of 100 µm. The parts are mostly made of plastic and aluminium and the helix is made of brass. So every component has been designed to be nonmagnetic in order to not interfere with the prototype.

A Xilinx FPGA has been chosen to perform the required power control algorithms and methods for the power conversion of the transmitter, to control the transmitter current ADC and the rectifier output voltage ADC, to switch and control the rectifier, and to monitor additional peripherals required for the operation of the system.

The FPGA evaluation board used was a standalone board customized for another project which contains the XSC40001A device. This board is supplied with 5 V and includes an oscillator on board of 60 MHz for the reference clock of the FPGA. PROM can be utilized to store the bit file that is loaded during start up into the FPGA. 22 device input/outputs are accessible through pin headers together with 4 pushing buttons which are enough for the requirements. Accessible I/Os are coming from two of the four FPGA banks. Power supply of these banks was necessary to replace to 3.3 V by changing the 1.8 V LDO to fit the requirements of the transmitter/receiver signals.

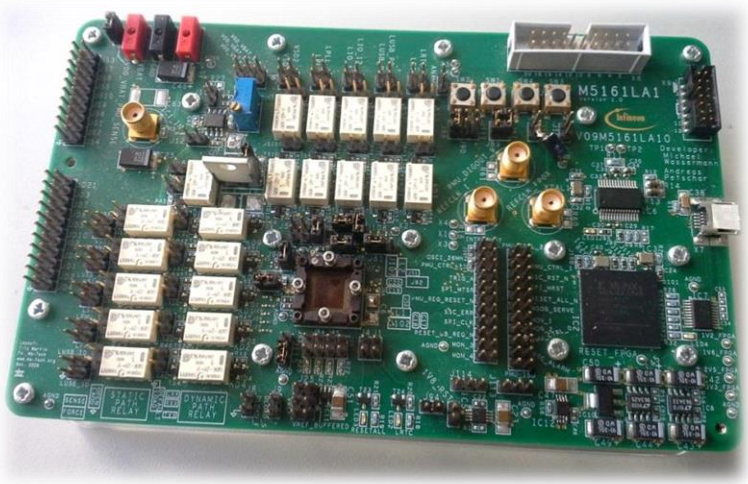


Fig. 21: Standalone customized FPGA board used

3.2. Transmitter and receiver coil

The proper design of the transmitter and the receiver coil plays an important role to the efficiency of any wireless power transfer system since they are the primary components. The energy is transferred over a relatively distance, which is of the order of the dimension (such as the radius or the diameter) of the coupled coils. Taking a look back to Fig. 5 shows that inductive power transmission over a large distance, e.g. into a space, is very inefficient. On the other hand, is very efficient under close proximity settings. However, looking at the following plot [Fig. 22] is representing that an increase of the distance between the coils is not the only

parameter which reduces the transmission efficiency. Also the diameter size difference between the transmitter (D) and the receiver (D_2), the smaller coil, is determining the efficiency. The efficiency plot values are shown as a function of the distance between the coils (z) and the diameter of the coil (D).

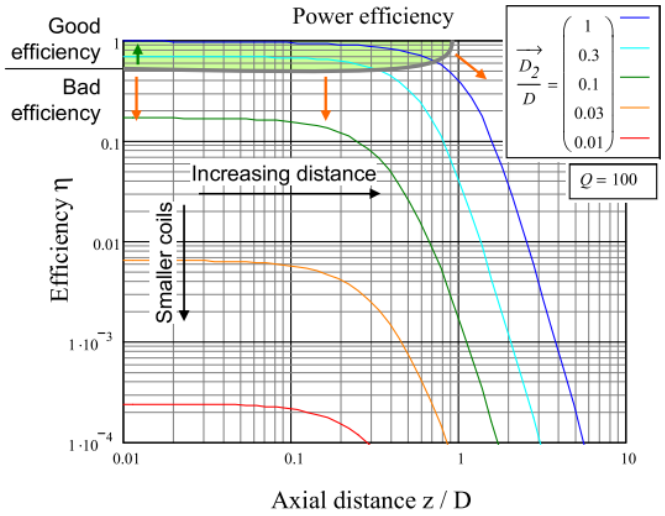


Fig. 22: Power efficiency as a function of relative distance between the coils. Calculated for a quality factor of Q = 100. Extract from [10]

From the plot [Fig. 22] two main definitions can be extracted:

- The efficiency drops dramatically at larger distance ($\frac{z}{D} > 1$) or at a large size difference of the coil ($\frac{D_2}{D} < 0.3$).
- A high efficiency (>90%) can be achieved at close distance ($\frac{z}{D} < 0.1$) and for coils of similar size ($\frac{D_2}{D}$ =0.5..1).

Two important coil parameters which are related to this behavior are the quality factor and the coupling factor.

3.2.1. Coupling factor

Depending on the distance between the transmitter and receiver coils, only a fraction of the magnetic flux generated by the transmitter coil penetrates the receiver coil and contributes to the power transmission. The more flux reaches the receiver the better the coils are coupled. The grade of coupling is expressed by the coupling factor *k,* defined as (1).

$$k = \frac{M}{\sqrt{L_{11}L_{22}}} \quad (1)$$

L_{11} is the self-inductance of the primary coil, L_{22} is the self-inductance of the secondary coil, and M is the mutual inductance[2] of primary and secondary coils. k factor values are between 0 and 1; 1 expressing perfect coupling, i.e. all flux penetrates the receiver coil, and 0 expressing none coupling at all, i.e. both sides are totally oscillated between each other.

The coupling factor is determined by the distance between the inductors and their relative size. It is further determined by the shape of the coils and the angle between them. If coils are axially aligned, a displacement causes a decrease of k [Fig. 23].

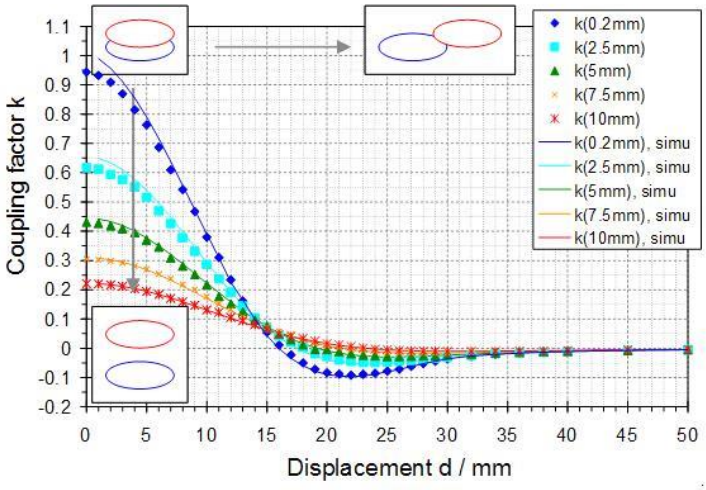


Fig. 23: Measured (points) and calculated (lines) coupling factors for two planar coils with 30 mm diameter. Extract from [10].

Fig. 23 shows the quality factor value for different distances between coils (vertical axis) and misalignment distances (horizontal axis). From the plot can be concluded that a little change of misalignment implies a considerable change in the coupling factor. Coupling factors in the range of 0.2 to 0.7 are typical [6].

[2] Also referred as a coupling inductance in WPT systems

3.2.2. Quality factor

The other important coil parameter is the quality factor Q which is mainly dependent on the shape and size of the coil as well as the materials used. It is defined as (2).

$$Q = \frac{\omega L}{R} \tag{2}$$

Since the ratio of the inductances L to the resistance R of a coil remains constant, the voltage induced in an inductor, scales with the frequency f and thus the apparent power in the device. The general definition of the quality factor is based on the ratio of apparent power to the power losses in a device. The quality factor Q values are between 0 and infinity, although it is difficult to obtain values far above 1000 for coils, typical values are around 100. A quality factor below 10 is not very useful.

In the case of resonant coupling technology, since the power is transferred only at a certain resonant frequency, Q factor is large and requires very close resonant impedance network matching in the receiver and transmitter. On the other hand, in magnetic induction coupling Q factor value can be lower and also the size of the coils allowing transferring power over higher frequencies. Fig. 24 shows the importance to have a high quality factor coils especially for MR and how is affected the efficiency in Fig. 25.

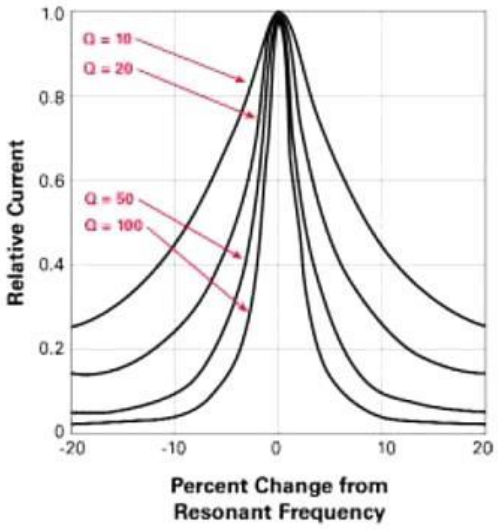


Fig. 24: An example of Q-factor percentage. Source [18]

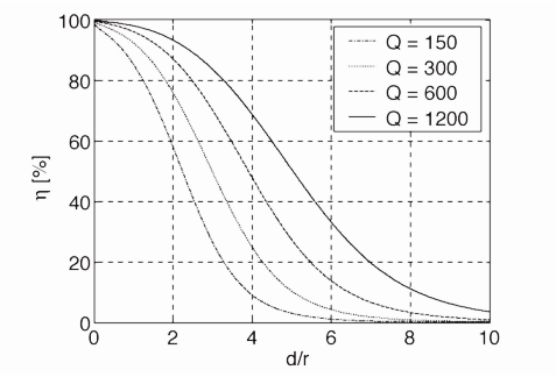


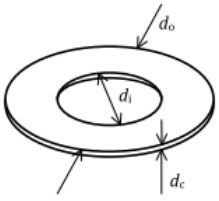
Fig. 25: Calculated maximum power transfer efficiency of a pair of circular coils with quality factor Q for different normalized distances. *d:* distance between coils, *r:* radius of the coil. Extract from [20]

3.2.3. Receiver and transmitter coils used

The inductance values can be obtained by examining the standard or existing products. Taking [21] as a reference, it can be found typical values for the primary (L_P) and the secondary coil (L_s):

$$L_P = 25\ \mu H$$
$$L_S = 10\ \mu H$$

The primary coil [Fig. 26] is a wire-wound type based on the Qi standard specification. Primary and secondary coils chosen are Würth Elektronik coils [Fig. 27 and Fig. 28].



Parameter	Symbol	Value
Outer diameter	d_o	$43^{\pm 0.5}$ mm
Inner diameter	d_i	$20.5^{\pm 0.5}$ mm
Thickness	d_c	$2.1^{+0.5}$ mm
Number of turns per layer	N	10
Number of layers	–	2

Fig. 26: Primary coil power pransmitter design A1 specifications

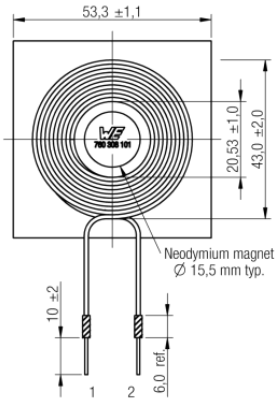


Fig. 27: Würth Elektronik primary coil dimensions

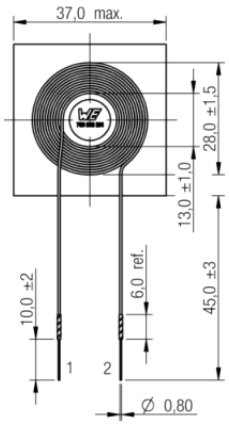


Fig. 28: Würth Elektronik secondary coil dimensions

Both coils contains a permanent magnet in the center for better alignment. Even though some experiments shows a reduce of performance on power transmitters that contains a permanent magnet, e.g. a longer charging time [7]. Therefore measurements with the coils selected have been done over the operating frequency [100 kHz to 205 kHz] in order to measure the quality factor and the self-inductance when a magnet it is placed or not.

Primary coil measurement was done with a permanent magnet and quality factor and inductance values are shown in Fig. 29. These results are fitting with datasheet specification [Fig. 30] and close to resonant frequency (100 kHz) the highest quality factor it is obtained. Even higher quality factor is presented with non-permanent magnet [Fig. 31]. Consequently for the different WPT measurements primary coil without magnet is used.

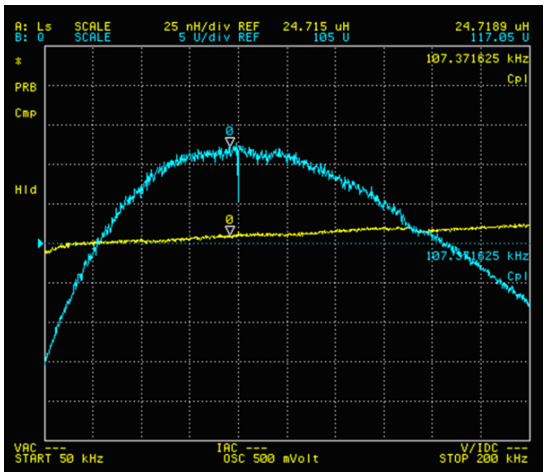


Fig. 29: Q-factor vs frequency measurement of the transmitter coil within the permanent

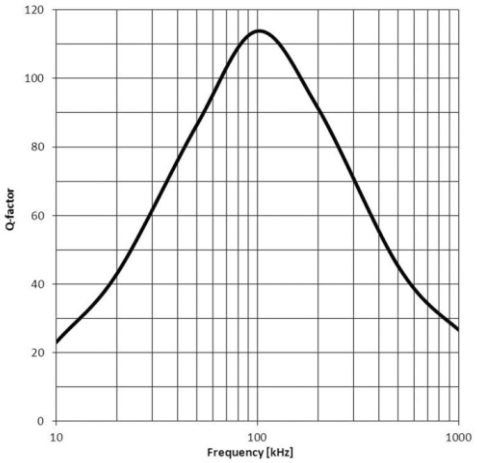


Fig. 30: Typical Q-factor vs frequency from the transmitter coil datasheet

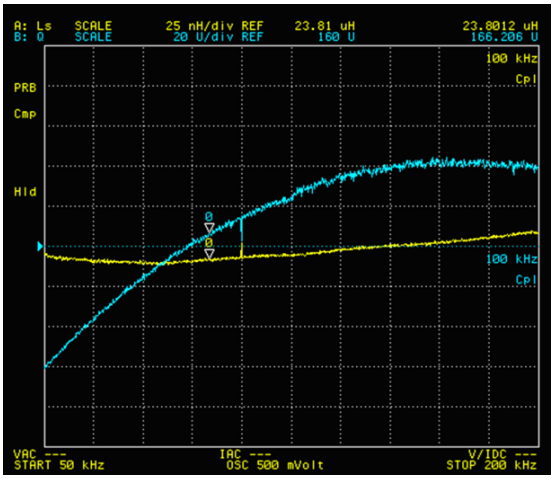


Fig. 31: Q-factor vs frequency measurement of the transmitter coil without the permanent magnet

On the other hand no Q-factor difference is present for the receiver coil comparing the measurements with [Fig. 32] and without magnet [Fig. 34] which are fitting with the specification datasheet [Fig. 33]. That is, the WPT measurements are done using the receiver coil with the permanent magnet.

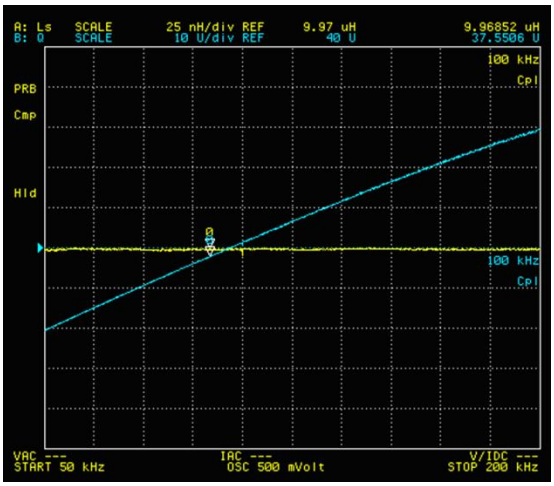


Fig. 32: Q-factor vs frequency measurement of the receiver coil within the permanent magnet

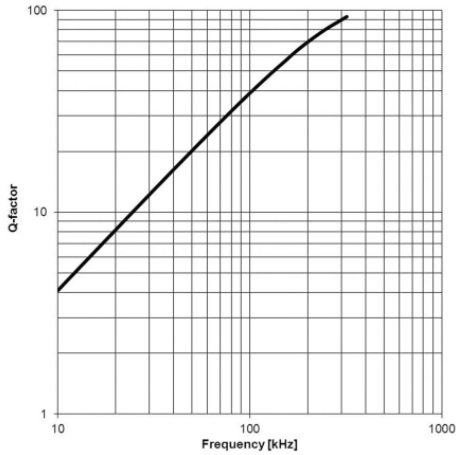


Fig. 33: Typical Q-factor vs frequency from the receiver coil datasheet

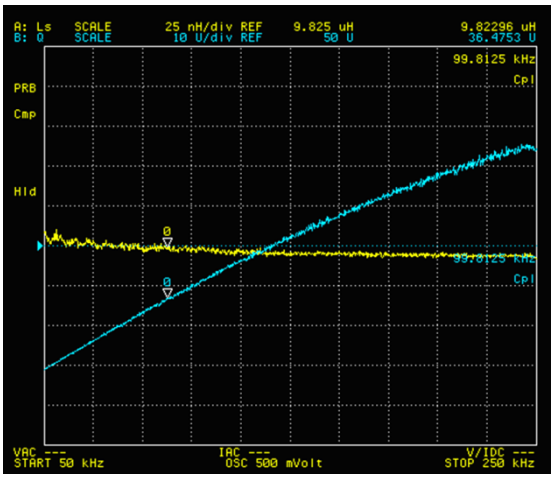


Fig. 34: Q-factor vs frequency measurement of the receiver coil without the permanent magnet

3.3. Compensation resonant circuit

As already has been mentioned in the magnetic induction and resonance section to enhance the power transfer capability, the coils needs to be compensated capacitively. Capacitive compensation is used in both the primary and secondary windings. The purpose of compensation in the secondary winding is to reinforce the power transfer. The primary compensation is used to decrease the Volt-Ampere rating of the source side converter thereby ensuring power transfer at unity power factor. These capacitors essentially store and supply

reactive power to and from the secondary and primary windings, reducing the amount of reactive power drawn from the supply.

There exist different types of compensation topologies; Series-Series (SS) compensation, Series-Parallel (SP) compensation, Parallel-Series (PS) compensation and Parallel-Parallel (PP) compensation [Fig. 35].

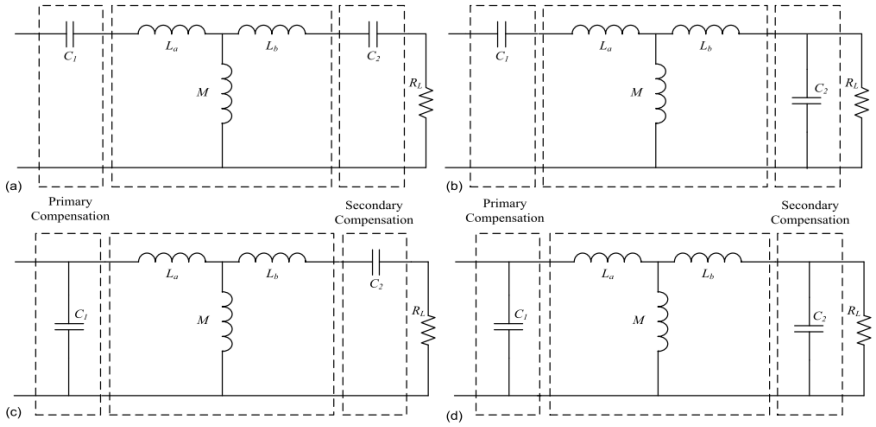


Fig. 35: Compensation topologies (a) SS (b) SP (c) PS (d) PP

Following the Qi standard specifications the SS compensation is implemented in the system designed [Fig. 36].

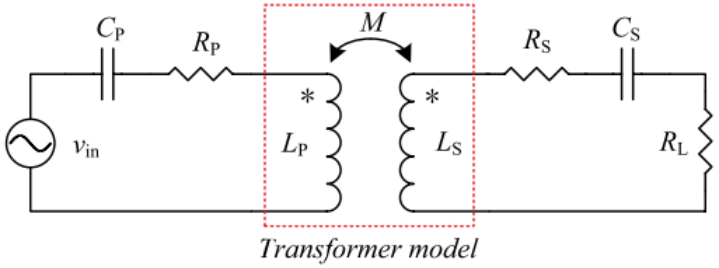


Fig. 36: Series-series compensation topology

In Fig. 36 the input signal is a sinusoidal voltage source with amplitude V_{in} at frequency ω. The primary and the secondary coils are represented by the inductors L_p and L_s respectively, followed by the compensation capacitors C_p and C_s. R_p and R_s resistances are the parasitic resistances (including both ohmic and radiative losses) of the coil and the resonant capacitor for the respective resonators. M is referred as the mutual inductance, given by (3). The load is represented by an equivalent AC resistance R_L.

$$M = k\sqrt{L_s L_d} \tag{3}$$

The values of the resonant capacitances can be extracted from the resonant frequency defined in the Qi Standard, i.e. 100 kHz. Knowing that:

$$\omega_{res} = \frac{1}{\sqrt{L_P C_P}} = \frac{1}{\sqrt{L_S C_S}} \tag{4}$$

Resulting the following values for the primary and the secondary resonant capacitors:

$$C_P = \frac{1}{\omega_{res}^2 L_P} = 105{,}54\ nF \tag{5}$$

$$C_S = \frac{1}{\omega_{res}^2 L_S} = 253\ nF \tag{6}$$

Chosen commercial values of results equation (5) and (6):

$C_P = 100\ nF$ with ± 5 % of tolerance (50 V rating voltage)

$C_s = 220\ nF$ in parallel with 20 nF (± 5 % and 50 V rating voltage)

3.4. Circuit analysis and efficiency of the system

An analysis of the circuit to study the efficiency of the system is done. From the schematic circuit [Fig. 36] an equivalent circuit model can be extracted [Fig. 37].

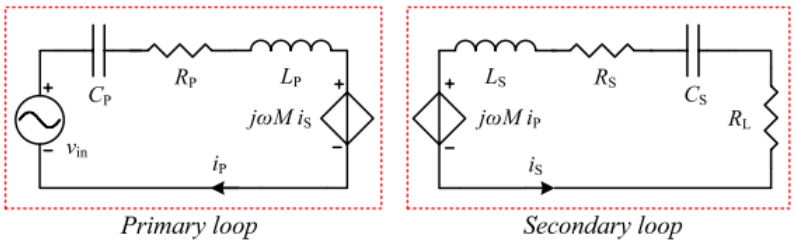


Fig. 37: Equivalent circuit model

The values of the DC resistance of the primary and secondary coils can be derived by the quality factor.

$$Q_P = \sqrt{\frac{L_P}{C_P}}\frac{1}{R_P} \quad \textbf{(7)}$$

$$Q_S = \sqrt{\frac{L_S}{C_S}}\frac{1}{R_S} \quad \textbf{(8)}$$

By inspection of Fig. 37, the current-controlled source in the primary side can be replaced by impedance Z_r, by dividing $\omega M i_s$ by i_p

$$Z_r = \frac{\omega^2 M^2}{Z_S + R_L} \quad \textbf{(9)}$$

where $Z_S = R_S + j\omega L_S + \frac{1}{j\omega C_S}$ is the impedance of the secondary network.

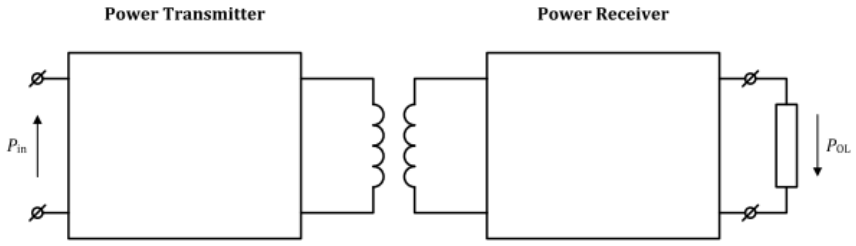


Fig. 38: WPT top schematic system overview

The WPT schematic diagram [Fig. 38], consisting of a power transmitter and a power receiver, is representing the DC input power (P_{in}) and the amount of DC power that is consumed in the load (P_{OL}). In most of the WPT applications this load correspond a DC-DC converter which would charge a battery. The system efficiency is defined as (10):

$$\eta_{system} = \frac{P_{OL}}{P_{in}} \quad \textbf{(10)}$$

Efficiency and low standby power are important aspects for wireless charging systems. Lower efficiency translates into longer charging times, increased heat dissipation, and overall waste of electrical energy. The wireless charger system should also contain some communication to detect presence of a receiver. In case there is no receiver the wireless power transmission should be switched off to have a low or preferably near-zero standby power consumption.

The overall efficiency can be easily calculated by considering the efficiencies of the primary and the secondary separately (11) and (12).

$$\eta_P = \frac{V_{source\_p} \cdot I_P}{V_{IN} \cdot I_P} = \frac{\Re\{Z_r\}}{R_P + \Re\{Z_r\}} \tag{11}$$

$$\eta_S = \frac{R_L}{R_S + R_L} \tag{12}$$

where the real part of the impedance Z_r is equal to

$$\Re\{Z_r\} = \frac{\omega^2 M^2 (R_S + R_L)}{(R_S + R_L)^2 + X_S^2} \tag{13}$$

The total efficiency is given by (14), where η_P is the primary side efficiency (the power transmitter) and η_S the secondary side (the power receiver).

$$\eta_T = \eta_P \eta_S \tag{14}$$

4. CHAPTER IV: Transmitter and Receiver Circuit design

Fig. 39 shows Qi-compliant WPT circuit using an A1 transmitter design as specified in the WPC standard [7].

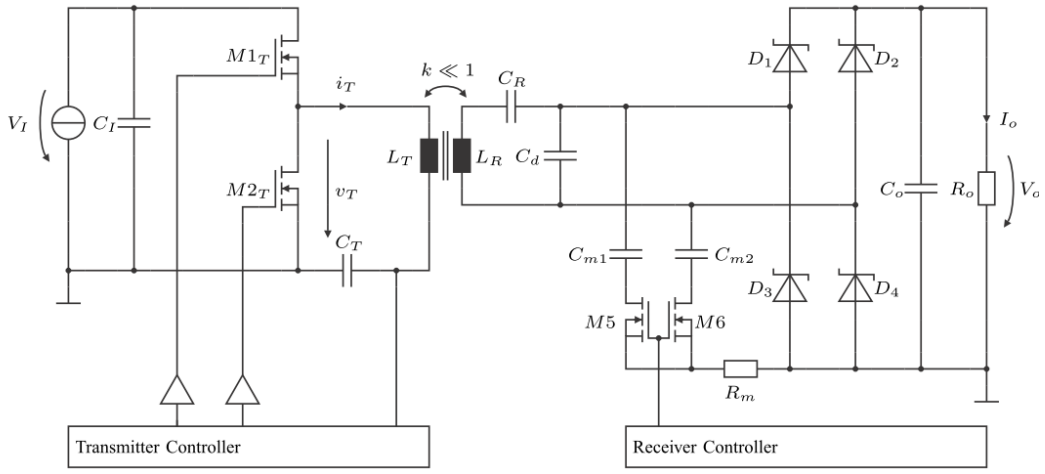


Fig. 39: Principal basic blocs of the A1 Power Transmitter (low power version) and the receiver designed. No sense nor control it is represented

4.1. Test Power Transmitter design

Flexibility of the power-transmitter design is limited to the Qi standard and the different blocks are in this chapter presented. A reference with the improvements and failures of the power transmitter PCB implemented is shown in the appendix Transmitter and Receiver PCB problems, redesign and improvements.

4.1.1. Qi Power Transmitter variants

As it has already been mentioned, in wireless power magnetic induction systems a correct alingment of the transmitter (primary) and the receiver coil (secondary coil) it is crucial to have a good coupling, and consequently an efficient energy transfer. Taking in count to this feature Qi Power Transmitter designs, which at the time of writing the WPC defines, are grouped in two basic types [7]; Type A and type B.

Type A Power Transmitter designs are based on a single Primary coil (either fixed position or moveable) and Type B Power Transmitter designs have an array of Primary Coils. This means that, while in Type A designs is necessary to realize proper alignment of the Primary

Coil with the Secondary Coil (a Guided Positioning) [Fig. 40] in Type B designs since an array of coils is present in the transmitter a Free Positioning of coil can be performed [Fig. 41].

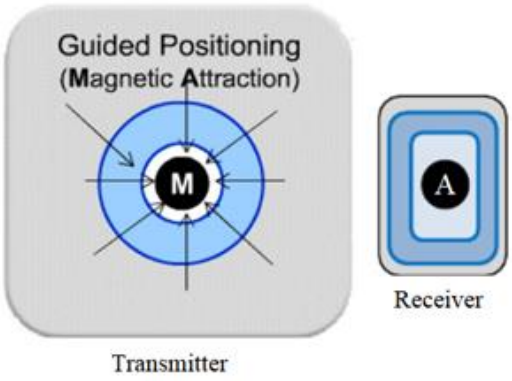


Fig. 40: Transmitter with guided positioning with magnet (M) at center of the primary coil and receiver equipped with magnetic attractor (A). Extract from [6]

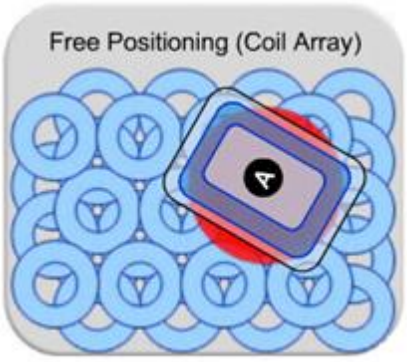


Fig. 41: Transmitter with free positioning - having matrix of primary coils (active primary coils are indicated by a red color). Extract from [6]

Since the goal of this project it is to experiment with one receiver, free positioning and coil array it is skipped, and guided positioning it is used. The permanent magnet in the primary and the secondary coil, showed in Fig. 40, helps to have a better alignment with both coils.

4.1.2. Power Transmitter requirements

Two Qi variants of transmitter have been implemented in the power transmitter PCB. One is based on the Low Power-A1 (LP) design defined in the Qi Low Power standard [7] for low power mode, and the other based on the Medium Power A10 (MP) defined in [22]. Both designs use the operating frequency and duty cycle of the power signal (19 V) in order to control the amount of power that is transferred. For this purpose, the operating frequency of the WPT system range from close to resonant frequency (110 kHz) up to 205 kHz. Frequency and power operation are shown in Table 4.

	Range values
Resonant frequency	100 kHz
Operational frequency	110 kHz – 205 kHz
Maximum Output Power	5 W (LP) – 15 W (MP)

Table 4: Q_i WPT specification

A higher operating frequency or lower duty cycle result in the transfer of a lower amount of power and otherwise. To achieve the desired power transfer an accurate adjustament of the amount of power has to be done.

4.1.3. Power Transmitter implemented overview

The power transmitter PCB implemented compromise of the following blocks (Fig. 42):

- Inverter: is the power conversion unit; converts the DC input to an AC waveform that drives a resonant circuit, which consists of the primary coil plus the compensation capacitor in series.
- The current sense: is the sensing circuit; monitors the primary coil current.
- Control Unit: is the FPGA; executes the relevant power control algorithms and drives the frequency of the AC waveform to control the power transfer.

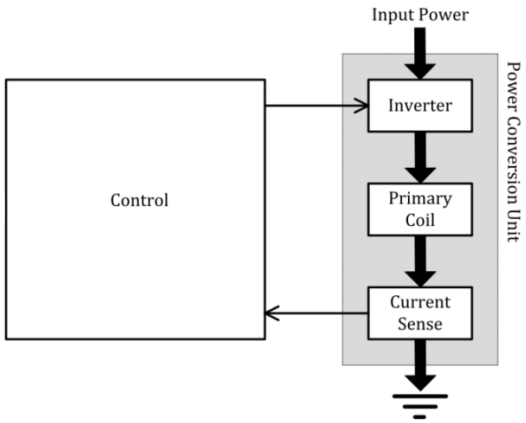


Fig. 42: Functional block diagram of the power transmitter design

Taking a deeper look to the hardware system design of the power transmitter [Fig. 43] it can be split into the following analog parts which are later described:

- Power stage design: full/half bridge inverter
- Pre-driver circuit design
- Sensing circuit design
- Auxiliary DC power supply design

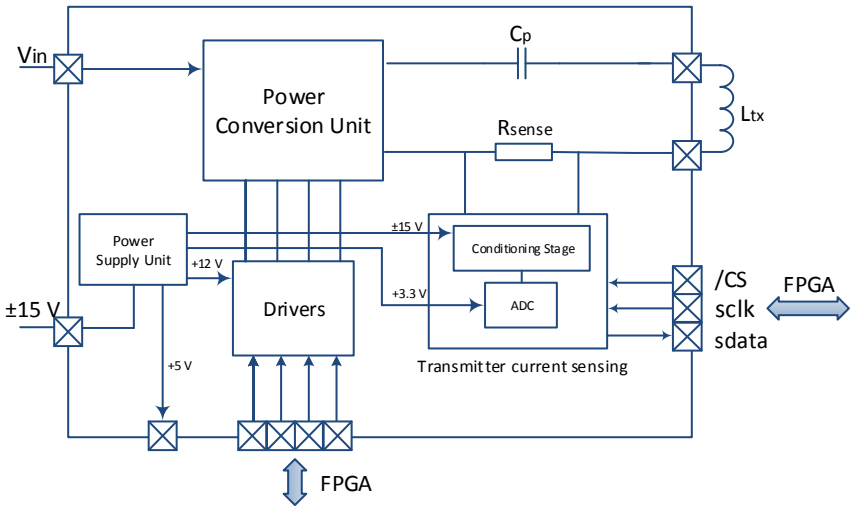


Fig. 43: Power transmitter system concept design

4.1.4. Power Transmitter specification

Power transmitter operates up to 19 DC input voltage together with a ±15 V auxiliary voltage and transfers enough power to meet the 5 W (5V/1A) load requirements for the low power configuration, and the 15 W for the medium power configuration. All the discrete hardware devices necessary for the operation of the transmitter can be externally and independently supplied from the input voltage or supplied from the on board dedicated linear voltage regulators. The key parameters are listed:

- Power conversion efficiency (DC - AC): 96,4 %
- Input voltage range: 5 V - 19 V DC
- Auxiliary voltage: ±15 V
- Operation frequency: 110 kHz up to 357 kHz (PMA)
- Power stage topology: half bridge and full-bridge
- Transmitter sensing current

4.1.5. Power Transmitter Blocks design

4.1.5.1. Power Stage: Full/half Bridge Inverter design

As it has been described previously the transmitter prototype can support low power and medium power transfer. To achieve these requirements and according to Qi specifications half bridge and full bridge are necessary respectively. The half-bridge inverter generates a

square wave signal at the switching node with an amplitude of 19 V. The square wave is then coupled to the primary coil and transmitted to the receiver. The transmitter can regulate the amount of power that is transmitted by adjusting the switching frequency and the duty cycle of the half-bridge.

As shown in Fig. 44, Power Transmitter design A1 uses a half-bridge inverter to drive the primary coil (L_p) and the primary resonane capacitance (C_p). In the Medium Power standard, a full-bridge inverter is recommended. MP-A1 structure design is shown in Fig. 45. BSO110N03MS Infineon transistors are placed for the full and half bridge configuration. These NMOS switches provide excellent gate charge and $R_{DS(on)}$ product (10 nC and 10 mΩ). Like typical MOSFET the gate source voltage has a limitation of 20 V. Having a requirement of input voltage range close to 20 V (19 V), this presents a problem to drive the high side switch. Therefore, a driver plus a bootstrap circuit it is necessary when the voltage drop between gate and the input voltage is less than the gate source voltage threshold. In the following chapter this circuitry is described.

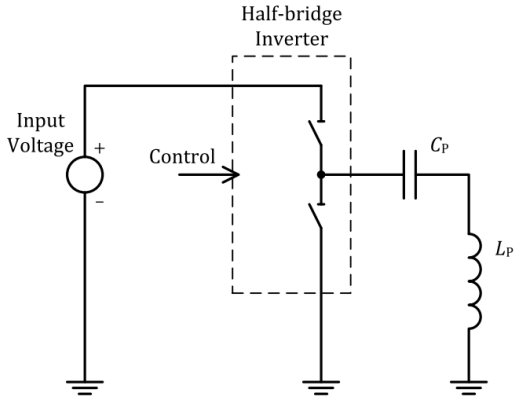


Fig. 44: Electrical diagram (outline) of Power Transmitter design A1 [7]

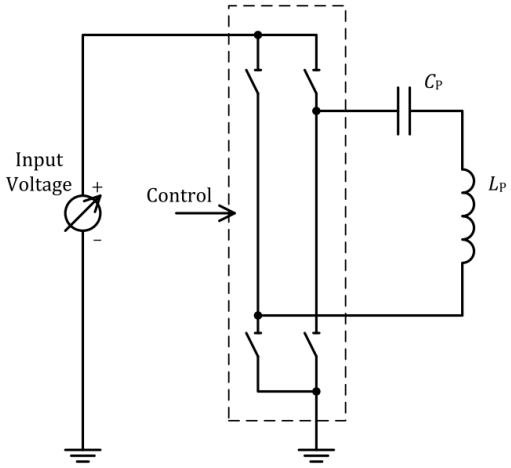


Fig. 45: Electrical diagram (outline) of Power Transmitter design MP-1 [22]

4.1.5.2. Transmitter Driver Circuit design

For driving the high-side and low-side a half-bridge MOSFET driver is required together with a bootstrap circuit [Fig. 46]. The DC supply net corresponds to the input voltage (19 V), Q1 and Q2 to the BSO110N03MS NMOS.

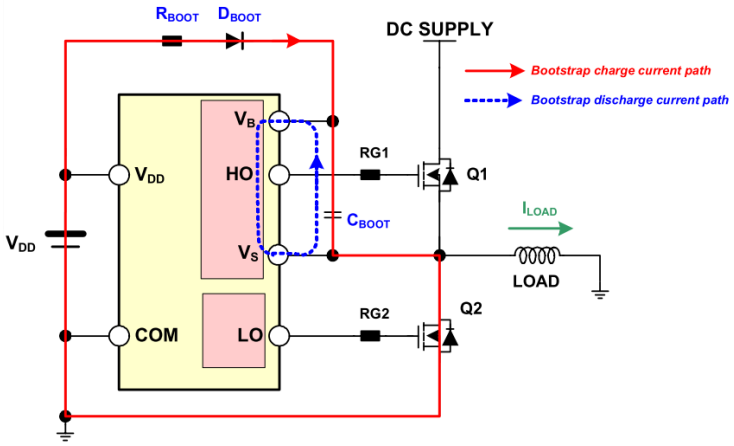


Fig. 46: Bootstrap power supply circuit

The bootstrap circuit charges the boot capacitor from V_{DD} when the low-side MOSFET is on. Then, when the high-side MOSFET is active this charge is used to ensure a proper supply for the high side MOSFET driver. With this, it pushes the high side gate voltage above the switching node voltage. Boot diode is necessary to block the rail voltage from the driver supply voltage when the low side switch is turned off and high-side switch is turned on.

NMOS bridge MAX15019A driver is used. Operating supply voltage range goes from 8 to 12,6 V. It allows to independently control both channels which are driven by the FPGA. Then, dead time and signal waveforms can be digitlally fixed. A schematic of the driver an the bootstrap capacitor is shown in [Fig. 47]. Following datasheet recommendations a 100 nF capacitor is placed. Some of the driver features are:

- Very short propagation delay from input to output (35 ns): perfectly suitable comparing to the switching operating frequency range.
- TTL input logic control: FPGA control.
- Low on-resistance: to reduce power losses.
- On-chip bootstrap diode: to reduce PCB complexity and lower external components.
- None inverting.

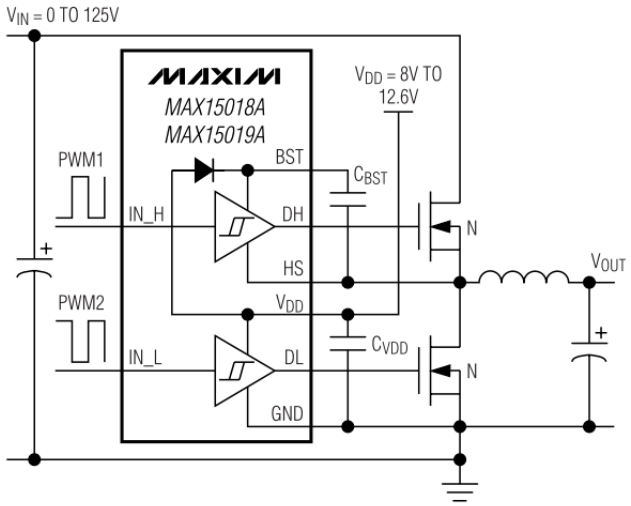


Fig. 47: MAX15019A NMOS driver together with the required external components

4.1.5.3. Transmitter Coil Current sensing

For the rectifier output voltage regulation loop a current sensing circuit has been designed to detect whether it is necessary to send more or less power by the power transmitter. According to Qi specifications in order to guarantee sufficiently accurate power control is required to measure the transmitter current amplitude with a resolution of less than 7 mA [7]. The sensing circuitry designed can be split in two sub blocks; the sensing element plus the conditioning stage and the processing part where an ADC converts the analog information in to digital to be processed by the FPGA.

The sensing circuitry should be able to measure frequency signals up to 200 kHz (357 kHz for the PMA standard), and withstand common voltage of ±20 V (or even much higher when the frequency it is close to the resonant frequency).

Several design approaches exists for current sensing [Table 5]. In order to fulfill the design requirements this approaches were studied:

- Resistive sensing: Resistor is the sensing element.
- Optical sensing: Infrared led is the sensing element.
- Hall Effect sensing: No sensing element it is used.

Type	Current range	Isolated	Accuracy	AC response	Non-Intrusive	Cost
Resistive	Very Low/ High	No	High	Medium/ High	No	Low
Optically isolated resistive	Medium/ High	Yes	Low/ Medium	Low/ Medium	No	Low/ Medium
Magnetic	Medium/ Very High	Yes	Medium	Medium/ High	Yes	High

Table 5: Common current measurement methods [23]

To reduce power losses in the power transmitter a good approach would be to use a Hall Effect sensor to avoid introducing any sensing element with results of a better efficiency of the whole WPT system. However, Hall Effects sensors have a bandwidth limitation too low for the application, typical between 10 kHz–25 kHz [24]. Optical sensing method introduces an IR LED as a sensing element but the sense signal is isolated from the conditioning circuit. Despite this interesting characteristic, its low-medium accuracy makes a discard method.

Resistive sensing circuit was selected [Fig. 48] because it's accuracy and simplicity circuitry. Besides that, thinking of a possible integration of the power transmitter in an IC the resistive sensing is the method which fits closer. A very small resistor of 10 mΩ it is employed to reduce power loses at the rectifier.

Some current shunt monitors were studied for the resistive sensing circuitry but were discarded because its limited gain-bandwidth. Therefore a high GBW and precision instrumentation amplifier (IA) was chosen, the AD8421. IAs provide high impedance non-inverting inputs, i.e. no load is added on the sensing circuit, allowing to sense small currents. Limitation due to common-mode voltage is avoided thanks to its input protection to 40 V

from opposite supply necessary in case that high voltage is present in the transmitter coil. Dual supply configuration of ±15 V is providing the power on the AD8421 IA.

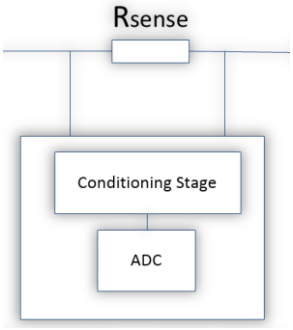


Fig. 48: Transmitter coil current sensing

An offset of half of the ADC voltage supply (1'65 V) is set to the output to shift the signal from ground for conditioning the signal for the ADC. Following AD8421 application notes for the reference voltage implementations, a buffer is placed to reduce impedance voltage source [Fig. 49].

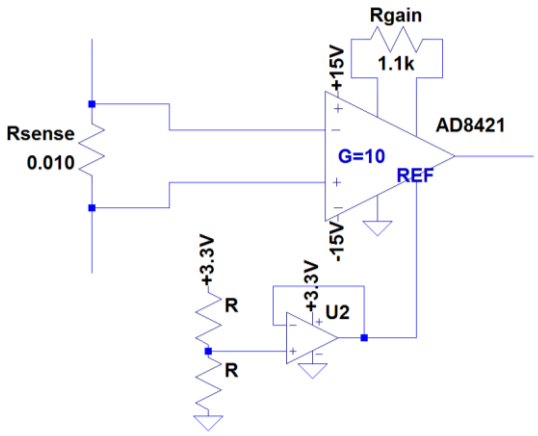


Fig. 49: Conditioning and sensing stage

The processing stage is done by the ADS7884 ADC with a conversion rate of 3 MSPS and 10 bits of resolution. ADS7884 offers an output serial data communication which reduces wire connections. It operates with a 3.3 V voltage supply.

4.1.5.4. Transmitter Power Supply design

Several linear voltage regulators are placed on board to supply each sub-circuit from the +15 V auxiliary supply in order to make the test setup more manageable; +3.3 V is needed for the ADC power supply, ±15 V is needed for the instrumentation amplifier, +12 V for the MOSFETs drivers and + 5 V for the FPGA.

4.2. Test Power Receiver design

While design of the power transmitter is restricted to keep it WPC-compliant, much more freedom is permitted to the power receiver [25] which typically is a portable device.

4.2.1. Power Receiver Qi requirements

Power receiver must withstand 5 to 15 W output power, for Low and Medium Power configurations and it should include the following blocks:

- Dual resonant circuit, consisting of the secondary coil and two resonant capacitors C_s and C_d with resonance frequencies of 100 kHz and 1 MHz, respectively.
- A rectification circuit, which can be realized both passively (e.g. diode bridge) or actively (with a MOSFET full bridge);
- A sensing circuit, to measure the rectified voltage and/or current.
- A communications modulator typically implemented with a switchable capacitor and/or resistor.
- An output disconnect switch: At the output of the receiver, instead of the output disconnect switch, a linear regulator (LDO) or a switch-mode DC-DC converter are typically placed to regulate the output voltage/current that is then provided to the load, i.e. the battery.

A typical architecture of a WPT receiver is shown in [Fig. 50].

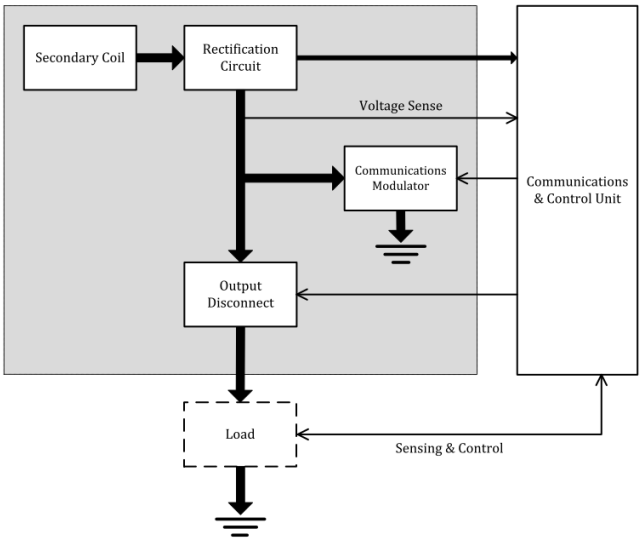


Fig. 50: Functional block diagram of a typicyal power receiver

4.2.2. Power Receiver implemented overview

The power receiver it is slightly different from the Qi specification. No communication circuit nor output switch nor dual resonant circuit it is implemented [Fig. 51]. The power receiver PCB implemented contains the following analog blocks:

- Resonant circuit consisting of the secondary coil and the resonant capacitors C_s with resonant frequency of 100 kHz.
- NMOS bridge rectifier circuit.
- A sensing circuit, to measure the rectifier output voltage.
- Zero-crossing current detection
- Zero-crossing voltage detection
- Clamping technique to protect the switches
- Auxiliary DC power supply design

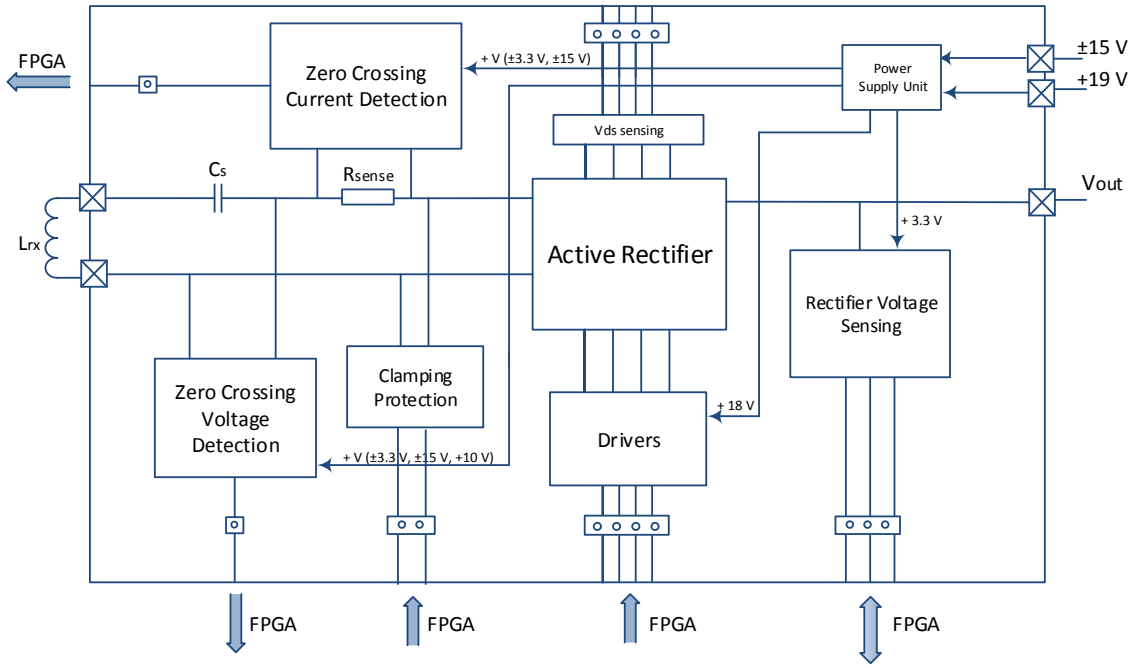


Fig. 51: Power receiver sytem concept design

4.2.3. Power Receiver blocks design

4.2.3.1. Rectifier

The rectifier is the key component of the receiver and therefore, comprehensive review is given. Its task consists, with the help of a capacitor, in converting the AC voltage coupled in the receiver coil to a certain DC voltage. Rectifiers can be broadly categorized in two types, half wave rectifier and full wave rectifier. The simplest of all the rectifier circuits is the half-wave rectifier which uses a single diode that conducts current in one direction [Fig. 52]. However, in terms of efficiency it is really poor as it just uses one half of each complete sine wave of the RF signal to convert it to a DC voltage. In the other hand, full wave rectifier makes use of the whole input signal to deliver a DC signal. There are several ways of connecting diodes to make a rectifier, but bridge rectifier is the most popular version.

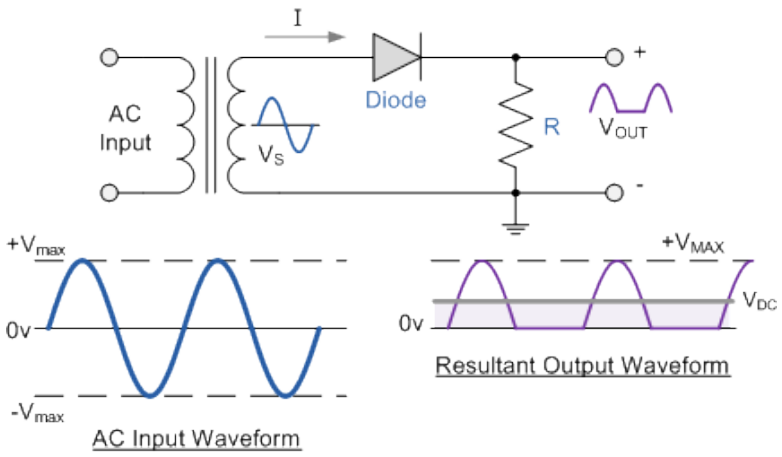


Fig. 52: Half wave rectifier

A full wave bridge rectifier along with a capacitor converts both polarities of the input signal to a DC signal. The arrangement requires four diodes as shown in Fig. 53, whereby, a pair of diodes is responsible for rectification of each signal cycle. When the input voltage is positive, D_1 conducts to deliver power to the load and D_2 regulates the current path from the load to the ground. In the negative cycle D_3 and D_4 are responsible for the current conduction. This structure benefits from high power efficiency and smaller output ripple compared to half wave rectifier. However, there is an unavoidable forward voltage drop (V_f) of the two diodes each signal cycle when current is flowing. Therefore, the output voltage is given by,

$$V_{out} = V_{in} - 2V_f \tag{15}$$

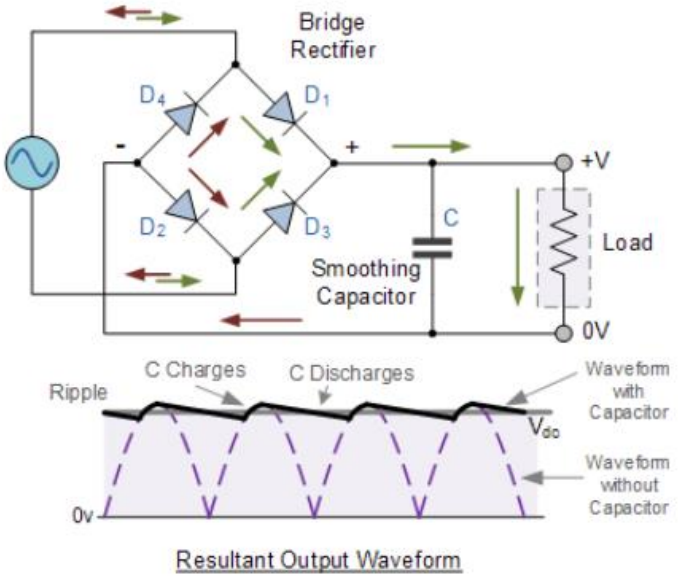


Fig. 53: The conventional full wave diode bridge

Depending on the forward voltage drop and the final application it may reduce considerable the efficiency. For a conventional silicon diode of 0'65 V this total voltage drop could be 1'3 V making none-feasible for low voltage applications. A simple solution to try to avoid this problem is to use low forward voltage diode like the Schottky diodes. A more challenging solution to really reduce it to practically zero and to enhance the efficiency is to use replace diodes for MOSFETs because the $V_{ds,on}$ losses can be much lower.

The active rectifier or synchronous rectifier is the structure developed in the system to achieve more output power and efficiency. The idea of the active rectifier is to replace the diodes of the conventional full wave rectifier with MOSFETs (Fig. 54), i.e. switch from the "passive rectifier" (no-control switching) to the active rectifier (switching control).

For IC rectifiers an especial attention has to be taken care to decide which type of MOSFETs should be used (NMOS or PMOS) for the bridge. Since for the same features PMOS devices are at least twice larger than the NMOS devices, a 4 NMOS bridge structure would reduce area size. However, to commutate the high-side NMOS switches an upper voltage than the rectifier output voltage is necessary which the IC cannot supply, i.e. an external boot strap circuitry would be needed plus. Utilizing the PMOS devices for the high-side switches would avoid the need for an additional pin due to the external boot strap capacitor.

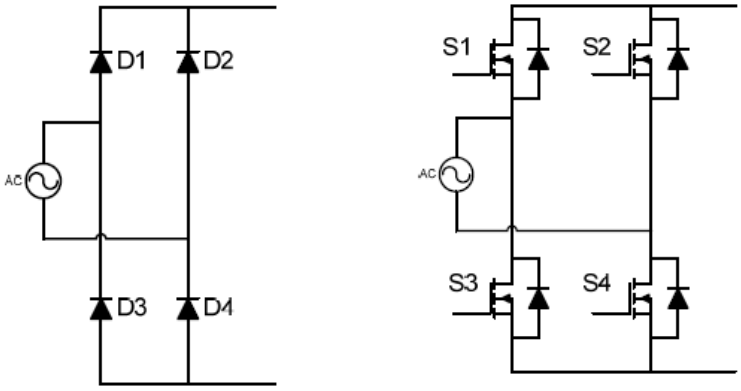


Fig. 54: Diode bridge, i.e. "passive rectifier" (left). Active rectifier (right)

BSO110N03MS Infineon NMOS switches are used. They provide very low on resistance (10 mΩ) to reduce power losses and low input capacitance to have fast transitions.

4.2.3.2. Rectifier Output Voltage sensing

A sensing circuit is necessary to monitor the rectifier output voltage for the regulation control loop and for protection of the power rectifier switches. Since not a high voltage resolution (some mV) neither high conversion rate is required the ADCS7477 ADC with 10 bits resolution and 1 MSPS is used. Despite the fact that less bit resolution and conversion rate could have been taken, equal devices costs made decide for this option. It provides serial output communication interface (SPI) reducing wire connections. A 3'3 V supply is employed to keep same communication voltage levels as the FPGA. Therefore, a voltage divider and a protection circuitry is placed at the input of the rectifier to not exceed supply voltage levels [Fig. 55]. 1/5 voltage division has been implemented, to limit the maximum ADC input voltage when the rectifier output voltage reaches maximum output levels (16'5 V).

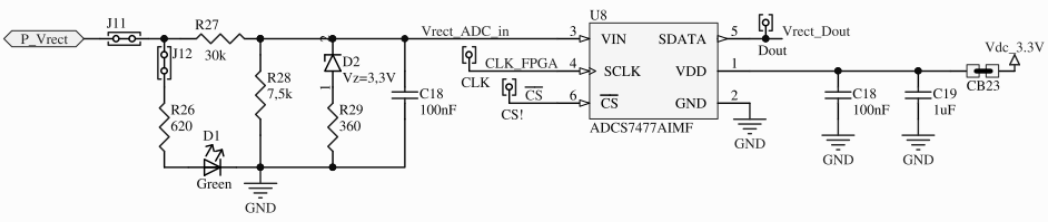


Fig. 55: Rectifier output voltage sensing

4.2.3.3. Zero Voltage Detection (ZVD)

The task of this analog block is to detect when the AC coupled voltage changes its polarity at the input nodes of the rectifier. This information it is used to control the switches of the rectifier. Two approaches of zero voltage detection have been implemented in the power receiver [Fig. 56]; a comparator detection of each node with respect to ground, which participates with the control of the rectifier, and a differential comparison of both nodes with respect to ground, which is more intended as a backup solution for possible experimental controls.

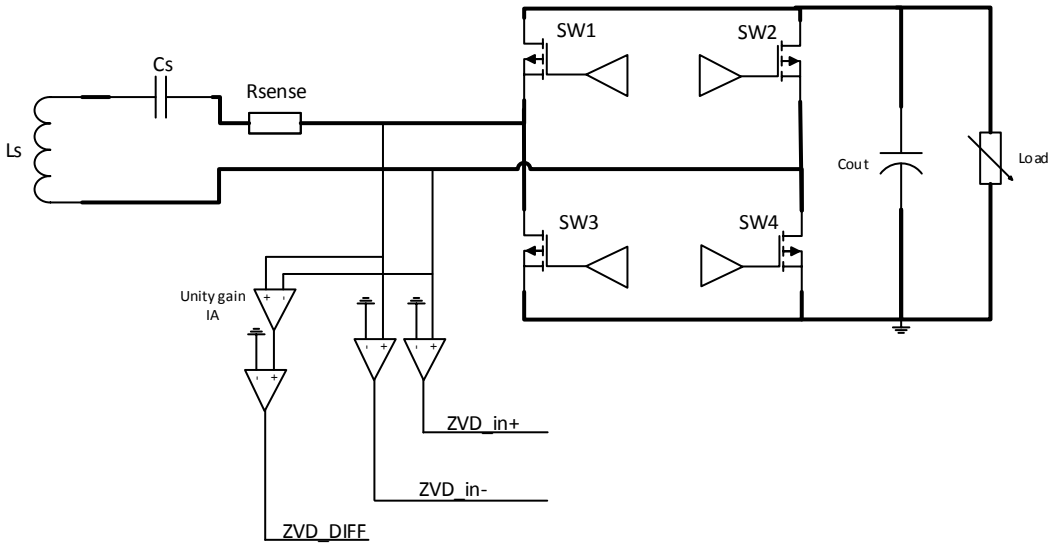


Fig. 56: ZVD circuitry

For the ZVD of each rectifier input branch a high performance comparator was required with:

- High common mode voltage: to withstand rectifier input voltages.
- Fast response time: to perform fast zero crossing detection.
- Low offset: to reduce ZVD errors.
- 3.3 voltage supply: to guaranty FPGA voltage levels.

The LT1719 ultra-fast comparator (4'5 ns), low offset (0'4 mV), and with isolated supply voltage for the input and the output is used. Due to its split supply is capable to accept higher common voltage levels. A 10 V single voltage supply is employed for the comparator input stage (no negative voltage is present to its inputs) and a 3'3 V for the output stage. A voltage

divider circuit can be added in case that the rectifier voltage exceeds: $V_{CC} - 1.2\,V$ (from the datasheet).

When the rectifier input signal crosses zero voltage level the ZVD circuit commutes to a high logic level Edge detection event is done with the FPGA. A hysteresis circuit has been added to the comparator to avoid undesired detections due to the noise coupling. For the ZVD comparator to ground the following hysteresis architecture is necessary [Fig. 57]. With this structure no input load is present to the hysteresis calculation.

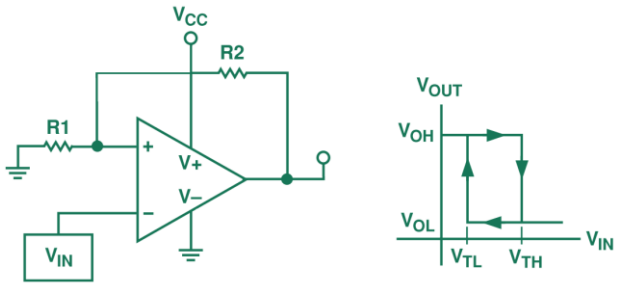


Fig. 57: Comparator using inverting input with external hysteresis circuitry

$$V_{TL} = \frac{(R_1 \cdot V_{OL})}{R_1 + R_2}$$

$$V_{TH} = \frac{(R_1 \cdot V_{OH})}{R_1 + R_2}$$

$$V_{hyst} = V_{TH} - V_{TL}$$

By checking LT1719 specifications: $V_{OL} = 0'4\,V$ and $V_{OH} = V_{cc} - 0'4\,V = 2'9\,V$

To have approximately +20 mV hysteresis over the zero crossing voltage detection the given function must be,

$$V_{TL} = 0\,V \qquad V_{TL} \approx 20\,mV$$

Therefore,

$$R_1 = 160\,\Omega \quad \text{and} \quad R_2 = 27\,k\Omega$$

Since the LT1719 operational amplifier provides a push-pull output no pull-up resistor was needed, whereas with an open drain comparator it would be needed to define the high logic level. The *Vdc_cmp* signal, showed in Fig. 58, is the input stage supply voltage of the comparator (up to 10 V) and the *Vdc_3.3V* signal the supply voltage for the output stage. *Vrect_in+* is the net connection to one of the nodes of the input rectifier.

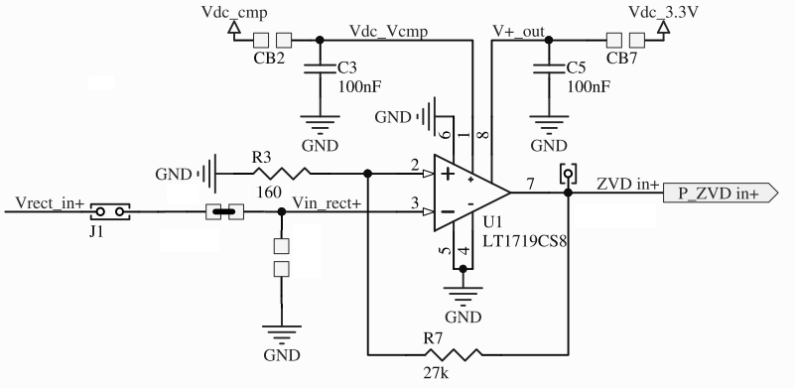


Fig. 58: Hysteresis comparator configuration for the ZVD

For the differential ZVD an instrumentation amplifier with unity gain is employed. The AD8421 instrumentation amplifier is the same as the one used in the transmitter coil current sensing circuit. Since the IA has complementary outputs a hysteresis structure can be implemented without having a reference voltage [Fig. 59].

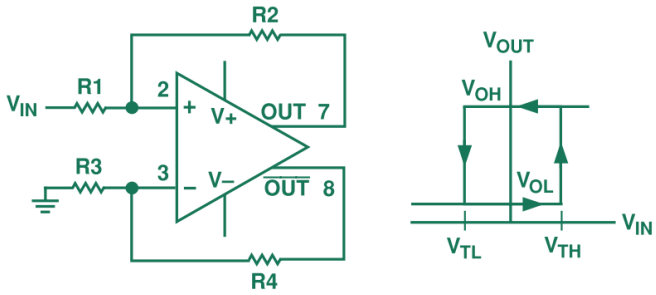


Fig. 59: Dual supply comparator with bipolar input and complementary output

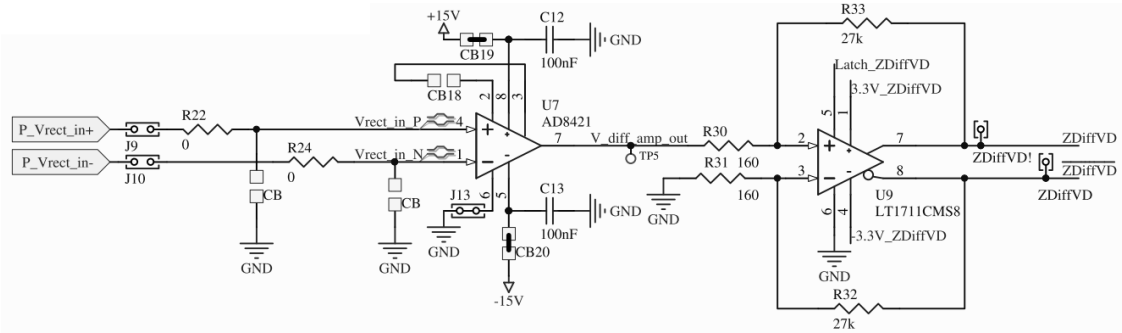


Fig. 60: IA with unity gain together with a dual supply comparator with external hysteresis

4.2.3.4. Zero Current Detection (ZCD)

This block detects when the AC current flowing into the rectifier is crossing to zero, i.e. the AC input signal changes its polarity. The detection is done on a very small sense resistor (10 mΩ) and after the resonance circuit in order to be in phase with the switching activity. To reduce power losses, this detection must be as fast as possible.

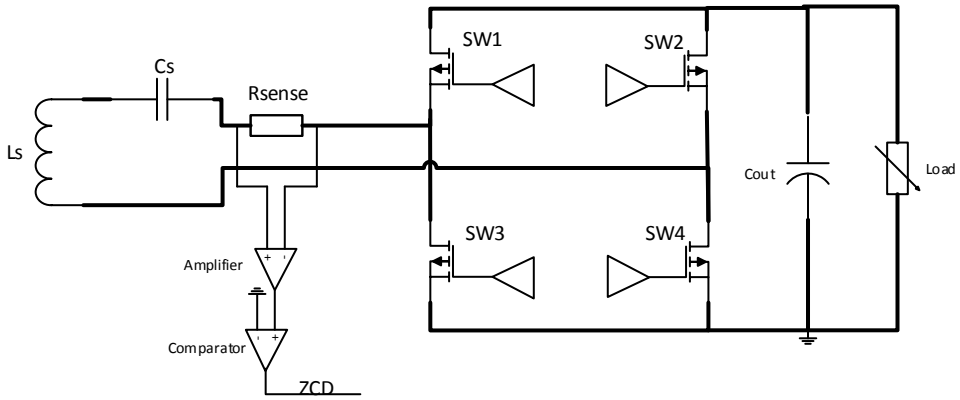


Fig. 61: ZCD circuitry

The implementation of this block consists of an amplifier and comparator to ground. The amplifier first amplifies the sense resistor voltage drop to be significantly relevant to compare to ground. For low currents, for example 50 mA, the voltage drop on the resistor it is only 0,5 mV. A gain amplification of almost 50 it is required.

Requirements for the amplifier were quite rigorous to fit like in the transmitter current sensing; low input voltage offset (less than mV), a GBW over 10 MHz[3] for unity gain, high common mode voltage (more than 15 V). Several differential amplifiers have been studied to fulfill these needs. The high precision amplifier ISL28217 was chosen because it's high operation voltage range, up to ±20 V, and high GBW, 10 MHz.

[3] Calculation based on the product of the maximum operating frequency (200 kHz) and the gain (50).

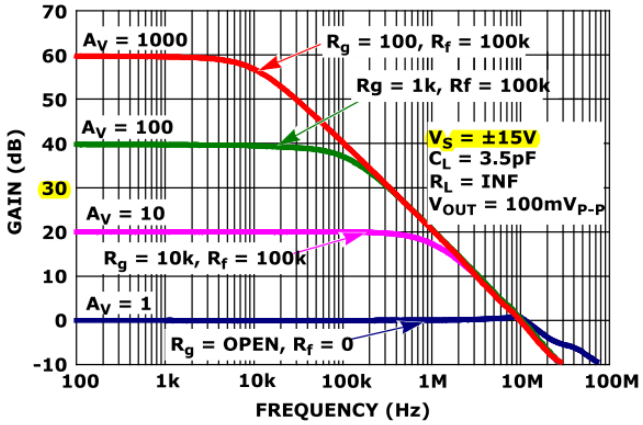


Fig. 62: Frequency response vs closed loop gain of the ISL28217 amplifier

Following the amplification structure [Fig. 63] of the difference amplifier the gain was set to 50.

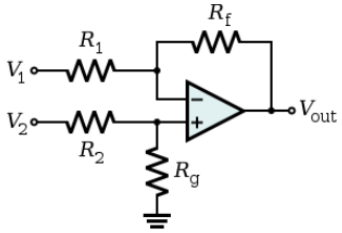


Fig. 63: Differential inverter amplifier

With $R_1 = R_2$ and $R_g = R_f$ the differential amplifier equation is given by,

$$V_{out} = \frac{R_f}{R_1}(V_2 - V_1) = G(V_2 - V_1) \quad \textbf{(16)}$$

To obtain an amplification of the signal by 50, these following resistors values have been chosen:

$$R_1 = R_2 = 1\ k\Omega \quad \text{and} \quad R_g = R_f = 5\ k\Omega$$

For the conditioning circuit a fast complementary output comparator was used, the LT1711, with two complementary outputs. Some simulations have been performed to check the behavior and the time response of the zero crossing detection [Fig. 64].

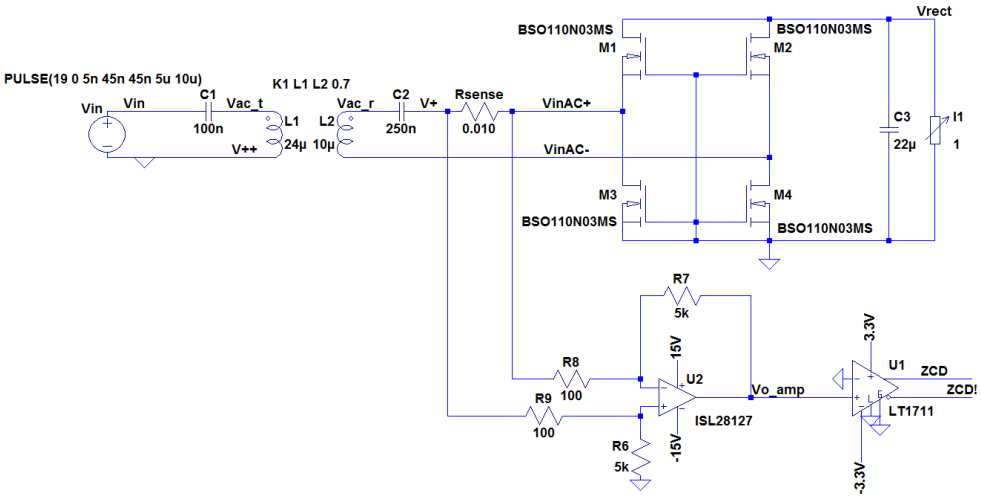


Fig. 64: Spice WPT schematic to test ZCD circuitry

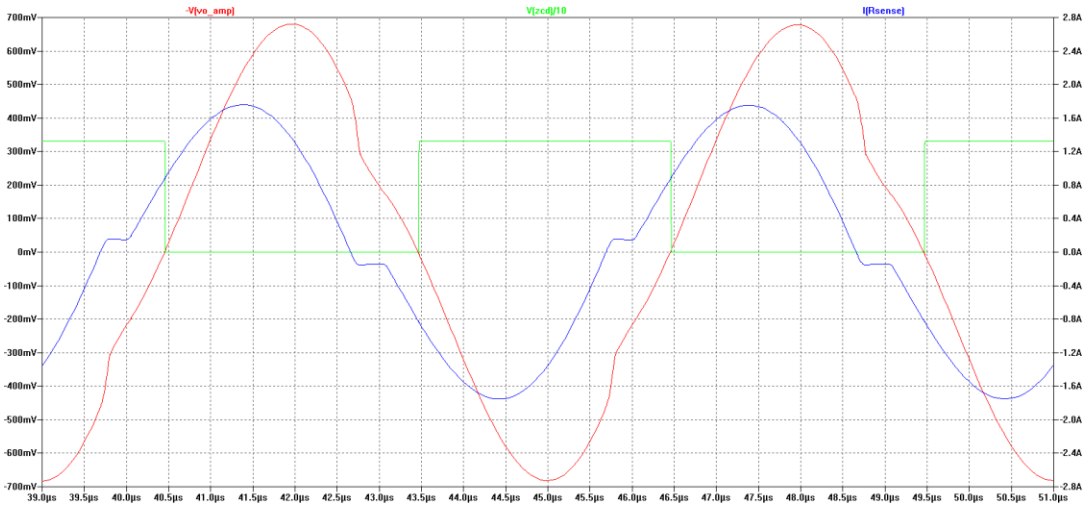


Fig. 65: ZCD simulations using ISL28217 amplifier. Receiver current through the sense resistor (blue), amplifier output voltage (red), zero crossing current detection divide by 10 (green)

As it shows in the simulation [Fig. 65], the amplification is very slow when the gain is set to 50, around 750 ns, consequently the detection as well. So it was decided to go for an instrumentation amplifier instead of the differential amplifier, the AD8421. This IA can operate up to ±15 V supply voltage and can withstand input voltages up to 40 V from opposite supply.

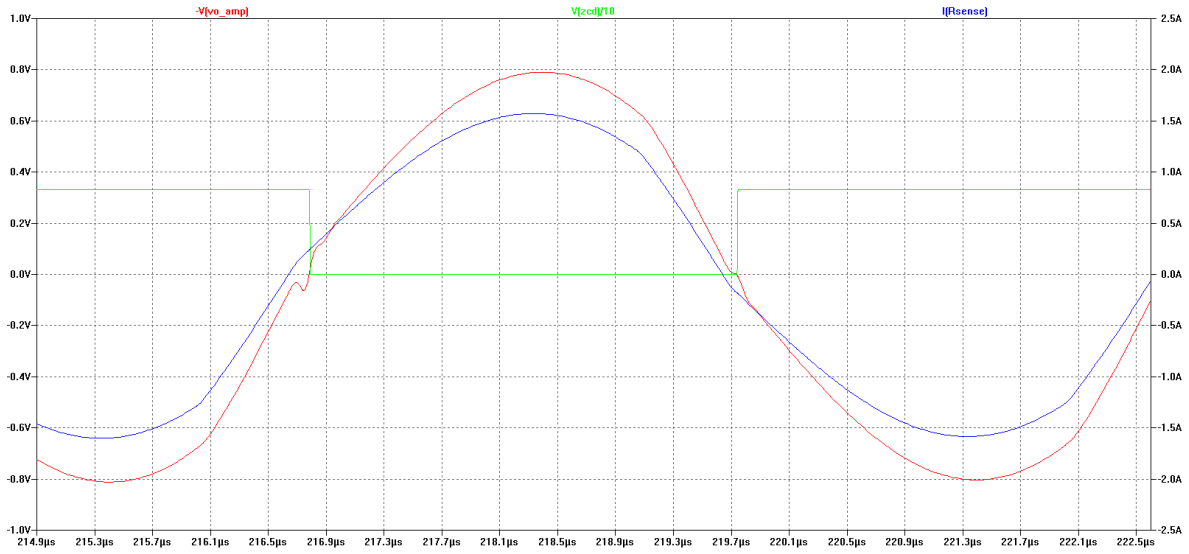


Fig. 66: ZCD simulations using AD8421 amplifier. Receiver current through the sense resistor (blue), amplifier output voltage (red), zero crossing current detection divide by 10 (green)

Fig. 66 is showing the improvement in response time, less than 100 ns, of the ZCD using the AD8421. Since some perturbation might occur, as showed in Fig. 67, the same hysteresis structure as for the differential ZVD has been added [Fig. 59]. The hysteresis voltage calculation can be extracted from the structure Fig. 68 and given by (17) and (18).

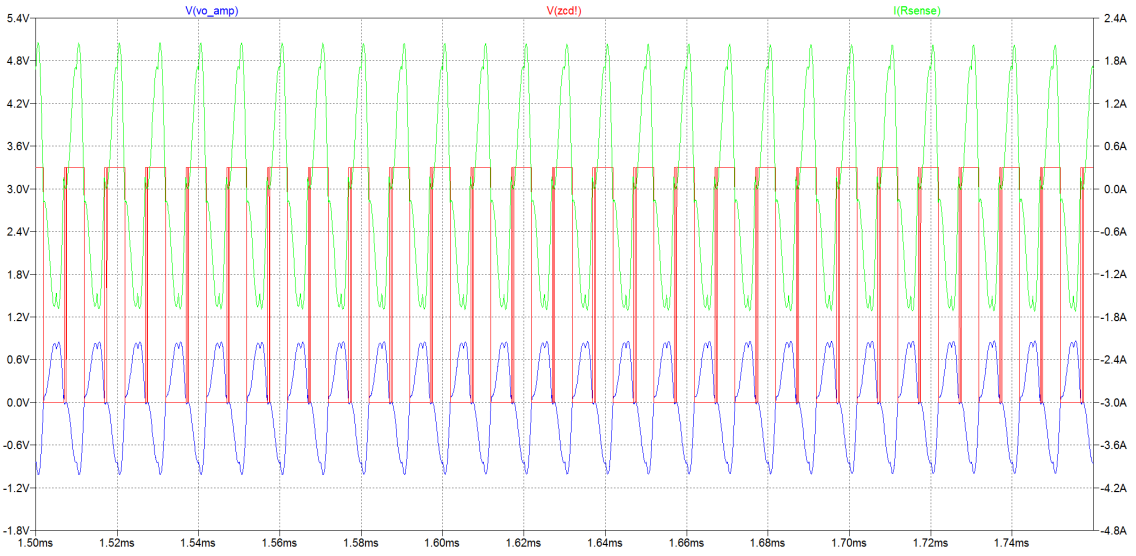


Fig. 67: ZCD simulation when perturbances are present. Receiver current through the sense resistor (blue), amplifier output voltage (green), zero crossing current detection (red)

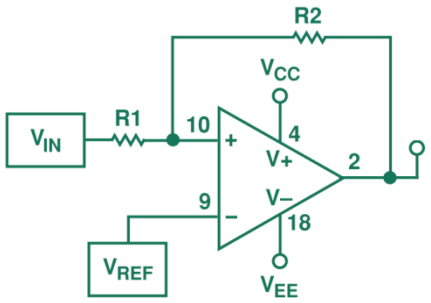


Fig. 68: Non inverting hysteresis comparator with reference voltage

$$V_{TH} = \frac{(R_1 + R_2) \cdot V_{REF} - (R_1 \cdot V_{OL})}{R_2} \quad \textbf{(17)}$$

$$V_{TL} = \frac{(R_1 + R_2) \cdot V_{REF} - (R_1 \cdot V_{OH})}{R_2} \quad \textbf{(18)}$$

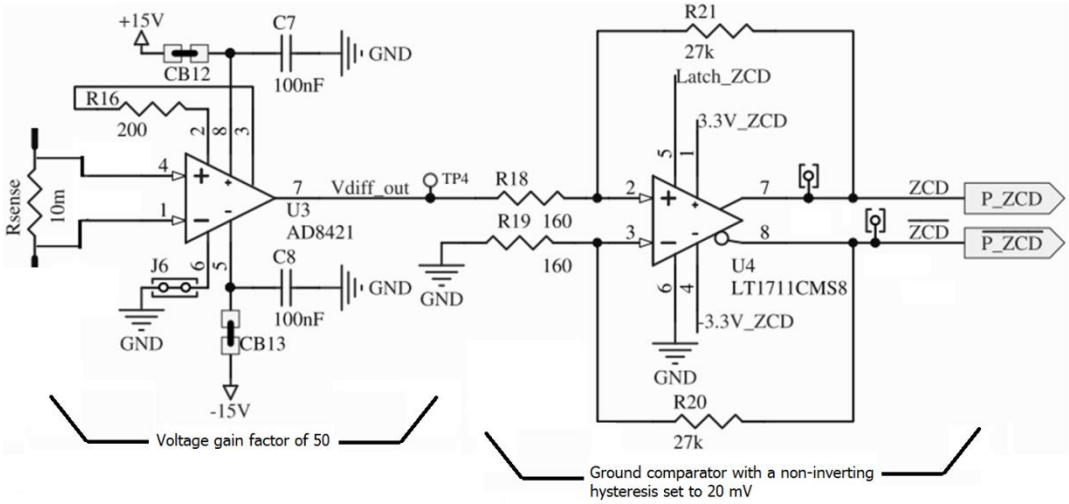


Fig. 69: ZCD circuit implementation

Fig. 70 shows that after implementing the hysteresis structure the perturbations do not affect the ZCD.

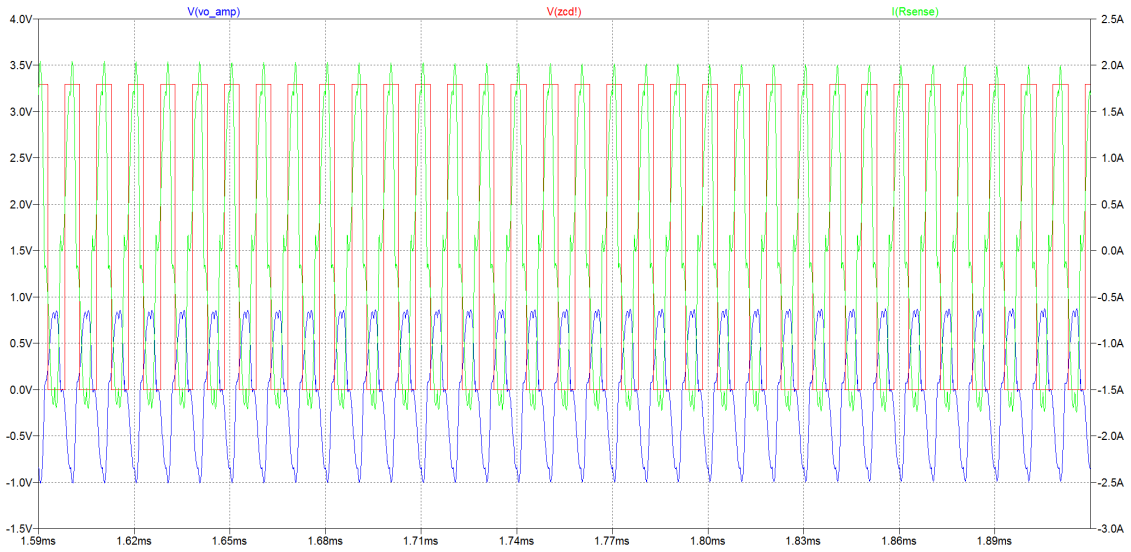


Fig. 70: ZCD simulation when perturbances are present. Receiver current through the sense resistor (blue), amplifier output voltage (green), zero crossing current detection (red)

4.2.3.5. Receiver Driver Circuit design

A simple driver circuitry has been utilized to drive the rectifier switches. In this case, no external bootstrap circuitry is needed since the dual MAX4427 driver can operate up to 18 V supply voltage; enough to drive the high-side NMOS switches of the rectifier when the rectifier output voltage reaches levels of 15 V. MAX4427 [Fig. 71] is a dual non-inverting power MOSFET driver with short delay time (typical 20 ns). This driver is TTL input compatible and can be driven directly from the FPGA with 3'3 V voltage levels.

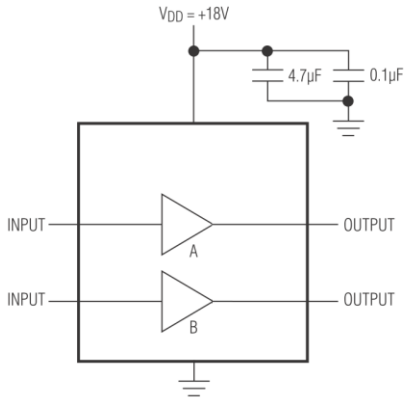


Fig. 71: MAX4427 driver connections

4.2.3.6. Clamping Circuit design

The clamping circuit [Fig. 72] is place to protect the rectifier MOSFETs when the voltage of the rectifier exceeds a specified voltage level. When this occurs, clamp is activated and current is steered away from the rectifier inputs through the clamping capacitors. The clamp is released when the rectified voltage drops below a predefined hysteresis window. The clamp activation and the hysteresis control is implemented by FPGA. Two low voltage level transistors (BSS138L) with small package size are turned on for the clamping activation. 470 nF clamping capacitors are used [28].

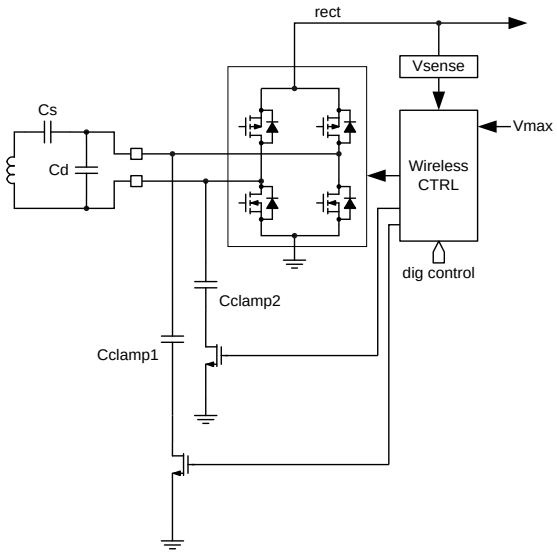


Fig. 72: Conventional clamping method

4.2.3.7. Receiver Auxiliary Power Supply design

The auxiliary power supply provides supply voltages for the different analog components of the receiver: +3.3 V is needed for the ZVD and the ADC, ±15V and ±3.3 V for the ZCD, +10 V is needed for the ZVD comparators and +18 V for the drivers.

4.2.4. Power Receiver Applied control

The main objective for the active rectifier bridge control is to imitate the diode bridge behavior. Due to the shape of the input-side waveforms [Fig. 73], the rectifier could be fully self-driven. However, for low loads and operating frequencies close to resonance the rectifier input waveform shape is not anymore square; see experimental results in chapter 5.3.5. For

this reason the detection signal is treated by the FPGA before directly connect to the switch gate [Fig. 74] and [Fig. 75].

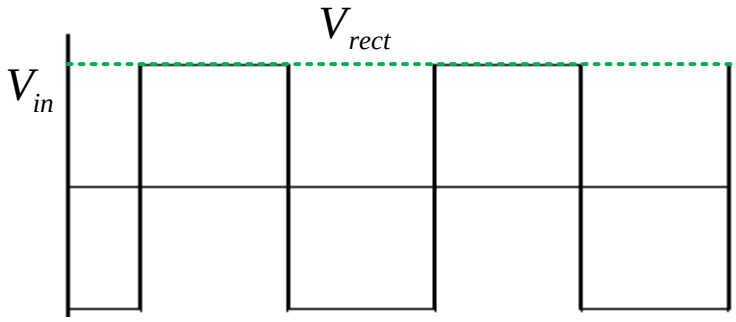


Fig. 73: Input voltage of the rectifier and the dc-output voltage (green)

The applied control method for the active rectifier is based on the comparator controlled rectifying switches which is currently considered the most promising solutions for overcoming the forward voltage drop issue [15], [26], see Fig. 75. However, these structures have problems at the start-up, and they must be power up passively. That is why another technique for driving the NMOS rectifier switches is added in the prototype, the zero-crossing current detection [Fig. 74].

In the ZVD both input branches of the rectifier are compared to ground to detect a zero-crossing voltage, and imitating the diode bridge, a pair of NMOS is activated for rectification of each signal cycle. The same procedure is developed with the ZCD but just one signal is processed to detect the direction of the current.

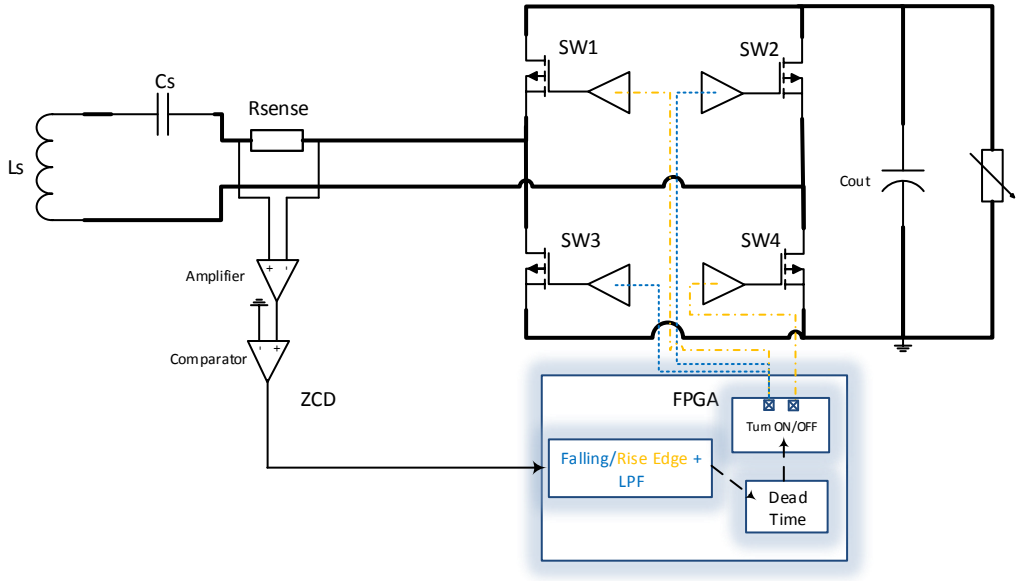


Fig. 74: ZCD implementation scheme with the FPGA

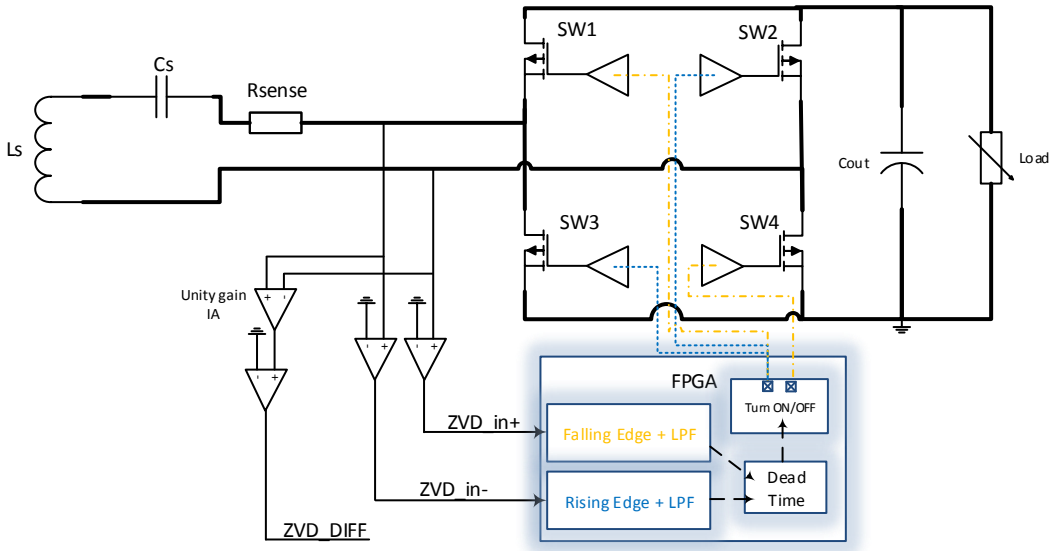


Fig. 75: ZVD implementation

An alternative control method could be to control the low-side switches as explained before and turning on the high-side MOSFET when the corresponding body diode starts conducting. This is detected by monitoring the voltage across the body diodes of the high-side switches. However, this control scheme would also slightly penalize the efficiency due to the body diode conduction.

CHAPTER V: System control – FPGA integration

The whole digital system implemented is able to control both the current and voltage ADCs, to set the operation frequency of the transmitter bridge, to control the rectifier with the feedback information of the circuit, and to protect the power switches of the rectifier. A view of the digital system implemented can be shown in [Fig. 76] and [Fig. 77]. An output voltage regulation control can be added to the WPT system to set a fixed voltage at the output using the PID coefficients given in the Qi standard specification. Because of the difficulties to achieve a proper control and the low importance, the control loop was skipped.

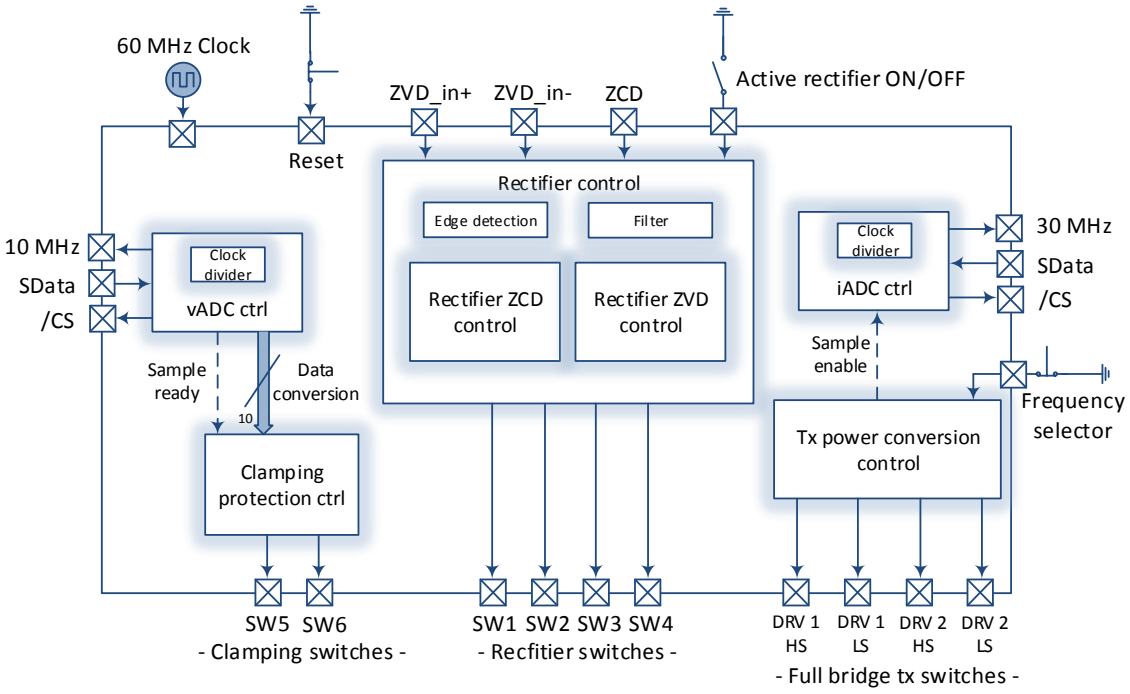


Fig. 76: WPT digital system

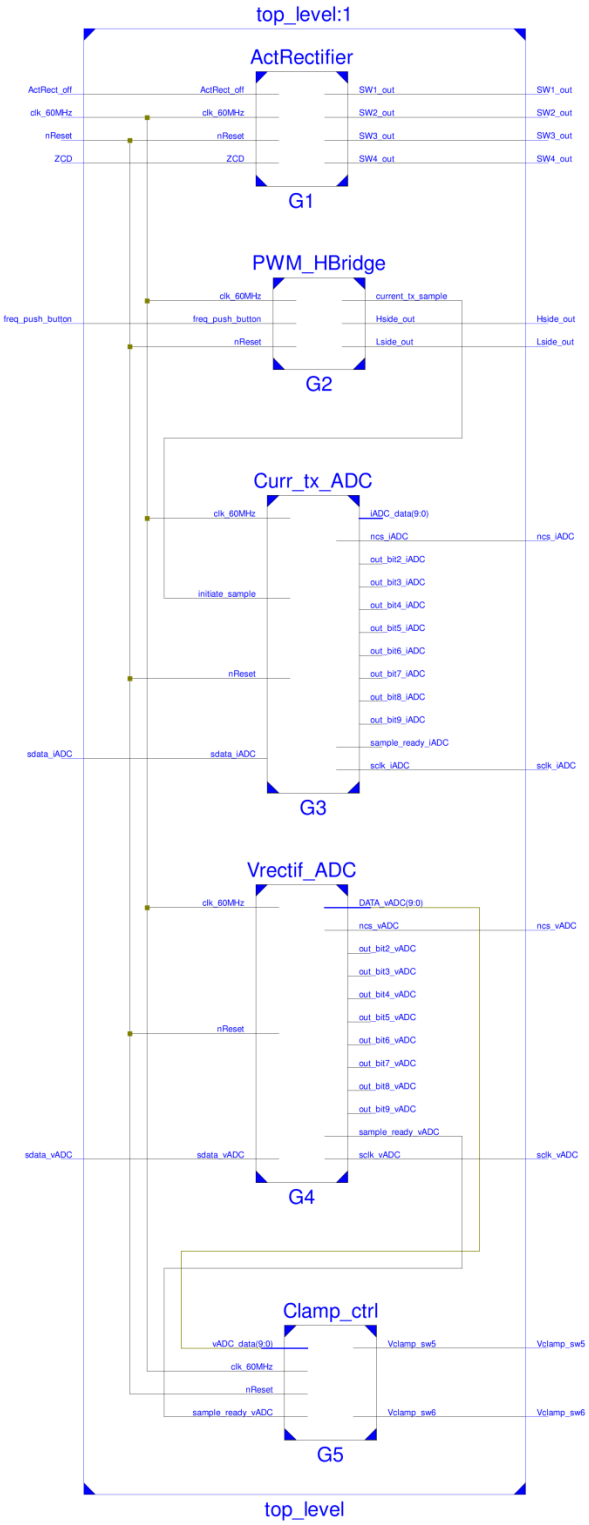


Fig. 77: WPT digital blocks

4.3. ADC's control

4.3.1. Transmitter Coil Current ADC control

This digital block implements the control of the ADS7884 ADC, the lecture of the serial input data, and the conversion in 10 bit data word. The ADS7884 is providing serial communication that contains 3 lines; *sclk* which is the serial clock of the ADC (30 MHz), $\overline{CS}$ referred to the chip select and *sdata* to the serial data. Besides these I/Os, another input signal (*sample enable*) is controlling when the current sample must be taken [Fig. 78]. According to Qi specifications a sense of the transmitter coil current amplitude is necessary for the power control. To achieve this sensing the *sample enable* signal, coming from the transmitter power conversion unit, indicates when the amplitude of the coil current can be measured [Fig. 79].

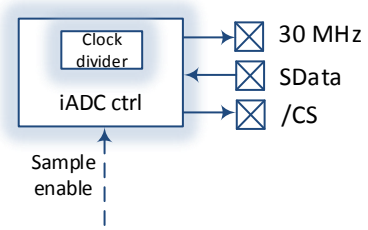


Fig. 78: Digital control block for the ADS7884 ADC

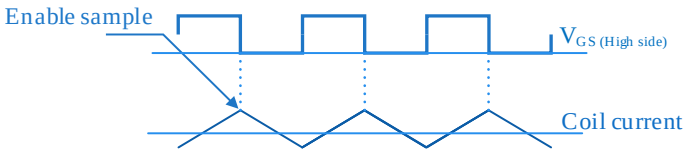


Fig. 79: Current sampling enable

A frequency divider has been implemented to extract from the external 60 MHz oscillator the 30 MHz clock necessary for the iADC. Chip select signal and clock times are respected following the timing diagram of the ADS7884 ADC [Fig. 80]. The source code is given in appendix 4.3.1. Fig. 81 shows the implemented finite state machine (FSM), with the following states:

- Initiation state: where the *chip select* signal remains high
- Conversion: chip select goes low and serial data is read and stored

- EOC (end of conversion): converted data is ready to be processed and waits till the 4 serial null data is send to switch to initiation state to start a new conversion.

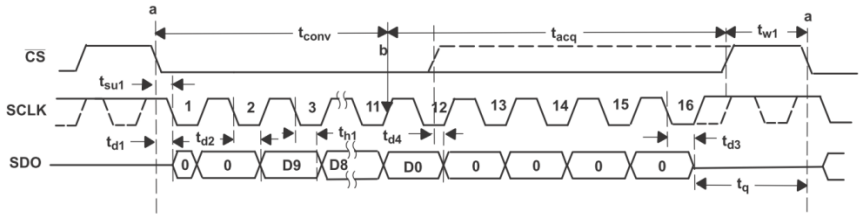


Fig. 80: ADS7884 Serial interface timing diagram (timing specifications in appendix 8.3.1)

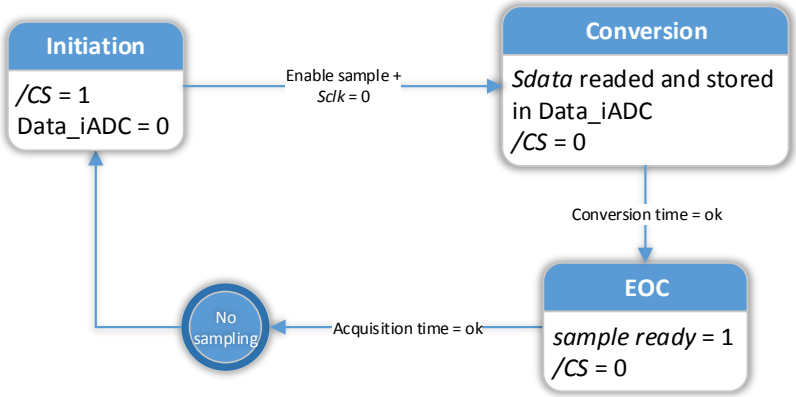


Fig. 81: FSM control for the ADC

4.3.2. Rectifier Output Voltage ADC control

For the rectifier voltage sensing the ADCS7477 ADC is used, much slower than the ADS7884, with a frequency clock of 10 MHz [Fig. 82]. Its FSM structure is the same as in the iADC control and the source code can be found in appendix 8.2.3. The vADC controller has an interaction with the clamping circuitry block sending the conversion data from the ADC and indicating (*sample ready*) when the data can be treated. The big difference with the iADC control is that the vADC control is always sampling and getting data values. Timing diagram for the ADCS7477 ADC is given by Fig. 83.

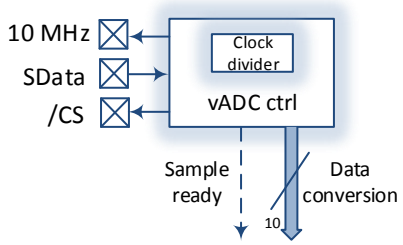


Fig. 82: Digital control block for the ADCS7477 ADC

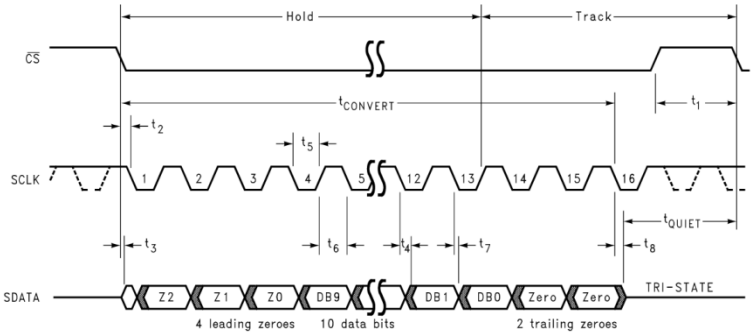


Fig. 83: ADCS7477 Serial interface timing diagram (timing specifications in appendix 8.3.2)

4.4. Transmitter Power Conversion control

This block is controlling either the half bridge or the full bridge transmitter frequency [Fig. 84]. Two inverted PWM controlling signals are set with a 50 % of duty cycle and an optimum dead time which by experimental tests was considered to be 50 ns [Fig. 85]. To achieve that one PWM signal is shifted to this time and reduce its duty cycle. These signals are turning on/off the low side (LS) and high side (HS) power transistors through its driver. An optimum frequency selection from 100 kHz up to 205 Hz with steps of 10 kHz can be done using the external push button. At each falling edge of the *HS* signal the *enable_sample* signal goes high to indicate that current amplitude can be measured. The source code can be found in appendix 8.2.1.

The bridge control implemented for the power conversion is based on the frequency control. Some other efficiency controls [27] may increase the efficiency but they are out of the scope.

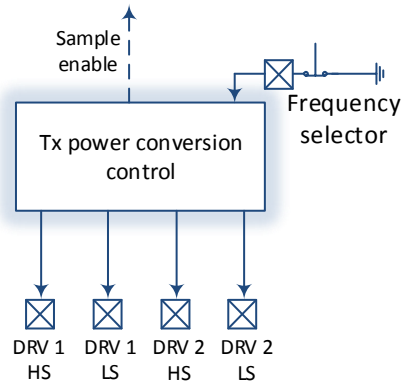


Fig. 84: Bridge control block

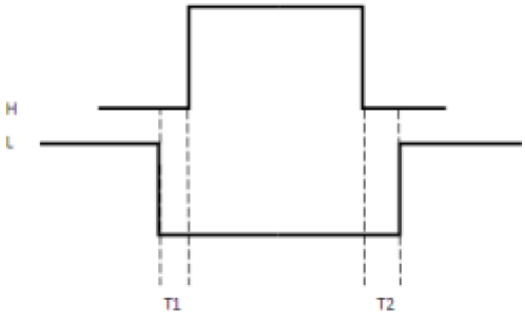


Fig. 85: High side and low side PWM signals with a dead time T_1 and T_2

4.5. Active Rectifier control

Two approaches of rectifier control have been designed as illustrated [Fig. 86:]. One is based on the zero-crossing voltage detection information of each rectifier input (*ZVD_in+* and *ZVD_in-*), and the other based on the zero-crossing current detection information. The ZCD control consists of 2 inputs, the *ZCD* and the enabling signal for the rectifier control (*ActRect_off)*, and 4 outputs which are the control signals of the rectifier switches and are directly connected to its respective driver. On the ZVD control the *ZCD* signal is replaced by the *ZVD_in+* and *ZVD_in-* signals.

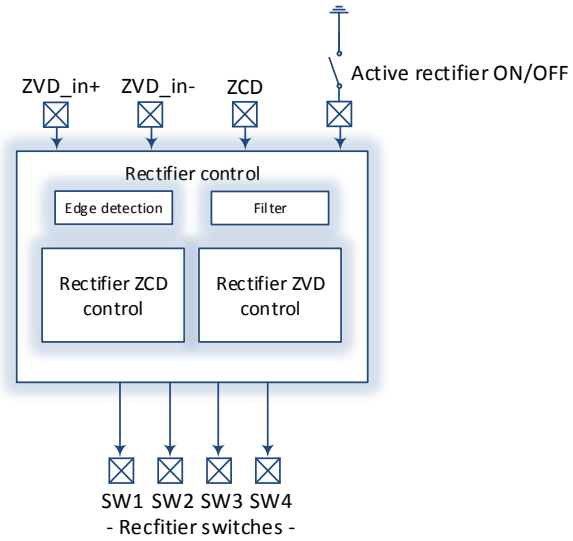


Fig. 86: Active rectifier control block

A logic level change on the *ZCD*, *ZVD_in+* or *ZVD_in-* signals indicates a zero-crossing detection and consequently a change of the switching control is done. Since these signals are external they must be synchronized with the clock before detecting a rising or falling edge of the signal in order to operate properly. This might cause metastability, i.e. the output logic level of the synchronizing flip flop is neither at logic high nor at a logic low but rather in an indeterminate level. Therefore, another flip-flop has been added to reduce probability of metastable failures [Fig. 87]. A low pass digital filter of the input signals has been implemented to avoid double zero crossing issues, see Fig. 118.

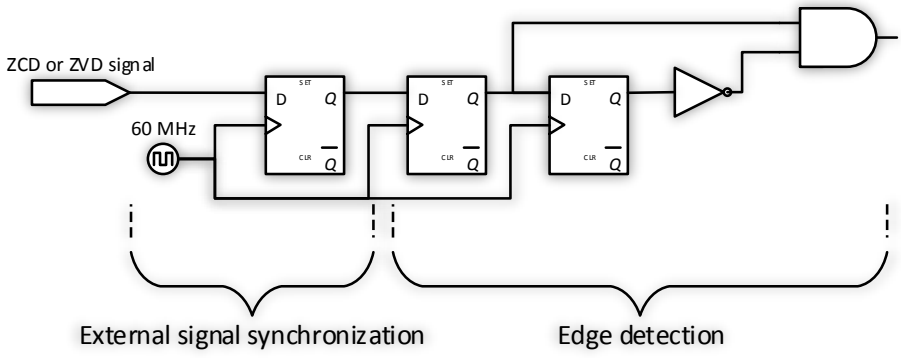


Fig. 87: Signal syncrhonization and rising edge detection

Basically the two control approaches are developed with the same structure and the difference is on the number of input signals. The FSM of the rectifier control based on ZCD is shown in Fig. 89. Once the active rectifier control has been activated by an external switch, the digital blocks checks the ZCD signal to detect whether it is a high (positive current) or low logic value (negative current) to jump to the state where the correct switches must turn on. After this a falling or rising edge of the signal, depending on which previous state, switches the states to turn on the other pair of switches. Before any state transition a dead time has been set of 50 ns to turn off all switches [Fig. 88]. Source code of the ZCD control can be found in appendix 0 and ZVD control in appendix 0.

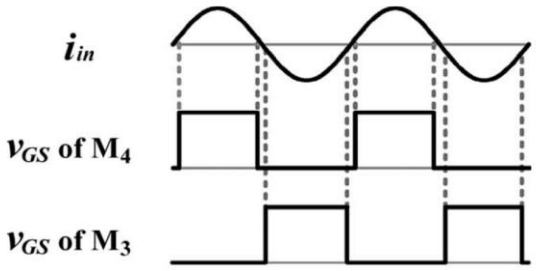


Fig. 88: Receiver coil current (i_{in}) and the PWM signals which drives the rectifier transistors

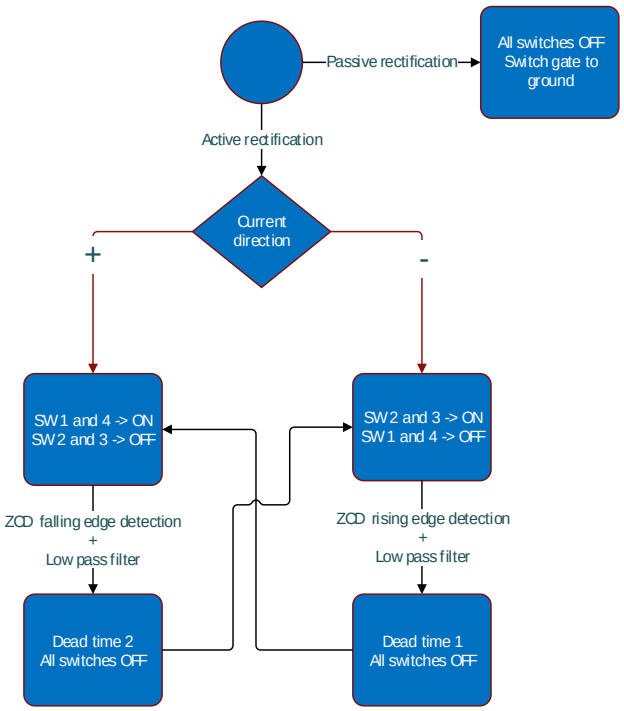


Fig. 89: Diagram of the active rectifier implemented control based on the ZCD

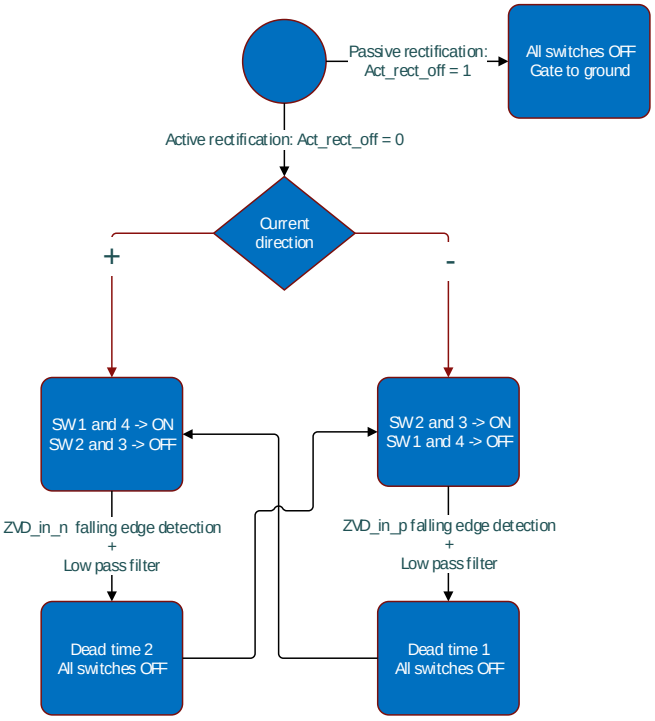


Fig. 90: Diagram of the active rectifier implemented control based on the ZVD

5. CHAPTER VI: Results and Measurements

5.1. Previous Tests

5.1.1. Coupling Factor measurement

A research and experimental tests about measuring properly the coupling factor have been done with the primary and the secondary coils of the WPT prototype. A comparison of the different techniques methods are here presented:

1. WPC proposed method [29]:

The coupling factor can be measured at an existing system as relative open loop voltage u:

$$u = \frac{U_2}{U_1} = k\sqrt{\frac{L_2}{L_1}}$$

Where U_1 and U_2 are de voltages applied to the coils, k the coupling factor, and L_1 and L_2 the self-inductances.

2. Series-aiding, series-opposing method [30]:

The proposed coupling method is based on the inductance measurement when they are in series-aiding [Fig. 91] or series-opposite connection [Fig. 92]. The mutual or the coupling inductance can be given by (19) and consequently the coupling factor by (20).

$$L_{12} = \frac{L_{aid} - L_{opp}}{4} \quad \textbf{(19)}$$

$$k = \frac{L_{12}}{\sqrt{L_1 L_2}} = \frac{L_{aid} - L_{opp}}{4\sqrt{L_1 L_2}} \quad \textbf{(20)}$$

Fig. 91: Series-aiding, L_{aid}

Fig. 92: Series-opposing, L_{opp}

3. Self and leakage inductance method [30].

This method is based on the leakage inductance, i.e. the inductance value when the other coil is shorted. Given that the coupling factor can be calculated as (21). If perfect measurements are made, k_{12} should equal k_{21}.

$$k_{12} = \sqrt{1 - \frac{L_{leak12}}{L_{11}}} \qquad k_{21} = \sqrt{1 - \frac{L_{leak21}}{L_{22}}} \tag{21}$$

L_{leakqr} = inductance measured at winding q when winding r is shorted

Results of the coupling factor measurement methods are collected in Fig. 93 for different distances between coils. As it can be seen, none huge difference is present in k between the techniques. Obtained results are slightly better if they are compared to the coupling factor measurement [Fig. 94] extract from [10].

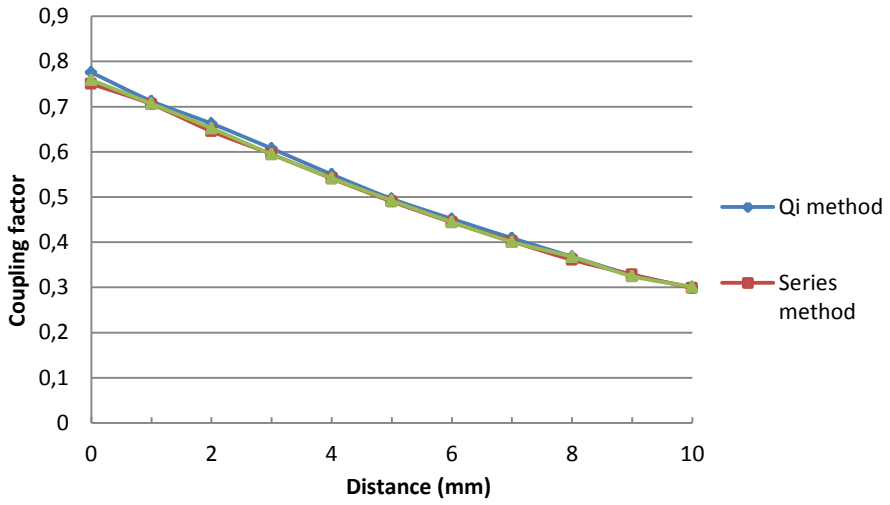


Fig. 93: Measured coupling factor vs distance between coils for different methods

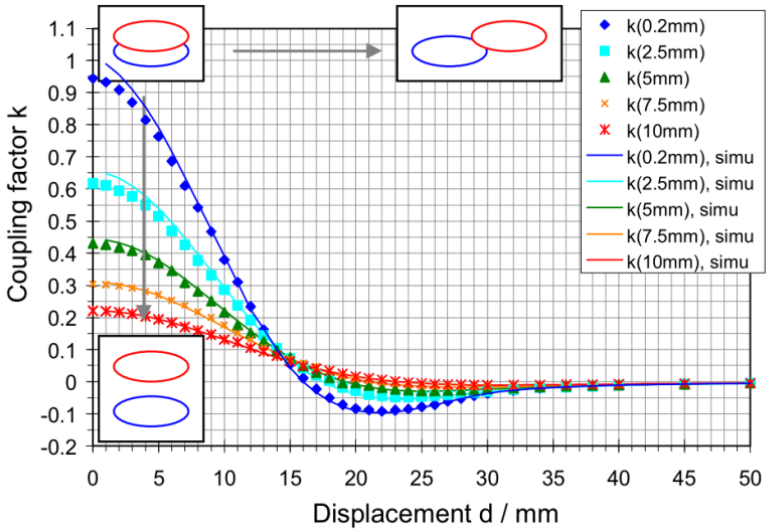


Fig. 94: Measured coupling factors of two planar coils with 30 mm diameter. Source [10].

As it has been mentioned, good coupling factors mean higher power transmission with higher efficiency. For a mobile phones or tablet charging application, where the powered device is laid on the power transmitter the short distance between each coil (≃2 mm for the device cover and around 2 mm more for the transmitter station) gives good values of coupling factor (> 0.5).

The last experiments have showed up that there is an important change in the inductance value when both coils are measured close to each other [Table 6], most probably because some mutual coupling inductance. Because of this, a particular attention must be done in the resonant frequency which it is affected and shifted.

Coil distances (mm)	L_{11} (µH)	L_{22} (µH)
0	43,42	18,97
1	36,56	15,59
2	33,04	13,89
3	30,51	12,76
4	28,81	12,06
5	27,68	11,57
6	26,74	11,28
7	26,17	11,02
8	25,67	10,82
9	25,28	10,62
10	24,99	10,58

Table 6: Primary (24 µH) and secondary coil (10 µH) measured values

5.1.2. Resonant Frequency measurement

The resonant frequency of the WPT system has been set to 100 kHz [Fig. 95 and]. By taking the definition of resonant frequency (22) and the primary coil (24 µH) measured values primary coil, Table 7 shows how is the resonant frequency scaled down when both coils are getting closer to each other with a resonance capacitor (100 nF). For distances above 1 cm this effect is not showing up.

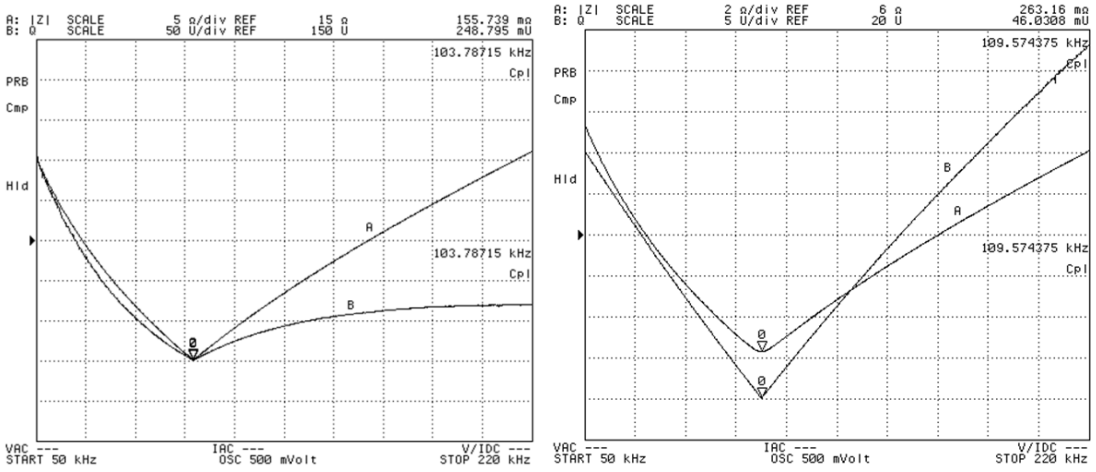


Fig. 95: Transmitter resonant frequency (left), receiver resonant frequency (right)

$$f_{res} = \frac{1}{2\pi\sqrt{LC}} \quad \textbf{(22)}$$

Coil distances (mm)	L (µH)	F_{res} (kHz)
0	43,42	76,4
1	36,56	83,2
2	33,04	87,6
3	30,51	91,1
4	28,81	93,8
5	27,68	95,7
6	26,74	97,3
7	26,17	98,4
8	25,67	99,3
9	25,28	100
10	24,99	101

Table 7: Resonance frequency with 100 nF, distance between coils

5.2. Functionality blocks verification

5.2.1. Transmitter power conversion unit

A test of the transmitter half bridge has been done to check its behavior. Special attention was done to detect possible cross conductions of the transistors and setting an optimized dead time. First measurements were indication a need of bigger input capacitor for the half bridge [Fig. 96]. In Fig. 97 a higher input capacitor was added.

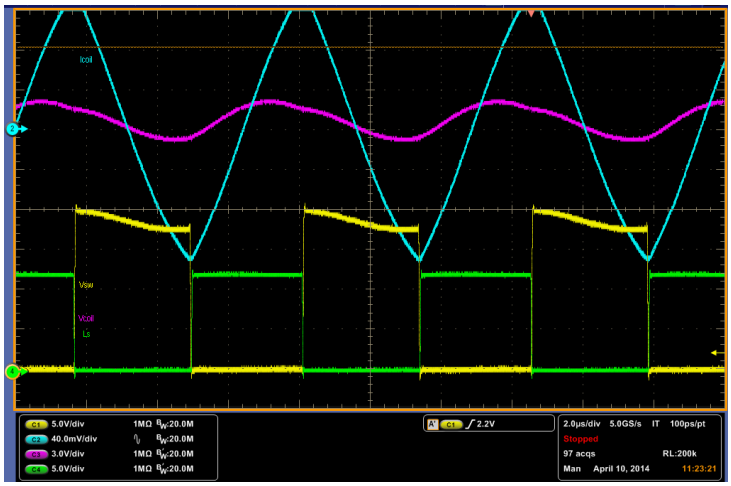


Fig. 96: Driver supply voltage (violet), switching node (yellow), low side switch gate (green), transmitter coil current inverted (blue).

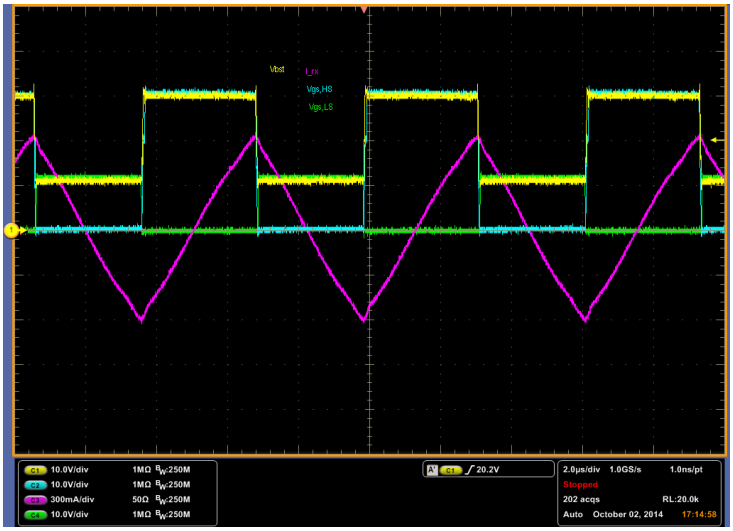


Fig. 97: Low side switch gate (green), high side switch gate (blue), coil current (violet), boost driver voltage (yellow)

5.2.2. Transmitter Coil Current sensing

In the following measurements a verification of the transmitter coil current sensing and analysis of the iADC control has been performed. Fig. 98 shows the serial data communication signals of the ADC when 1'7 V it is applied at the input. Serial clock and chip select signals are matching with the ADC specifications.

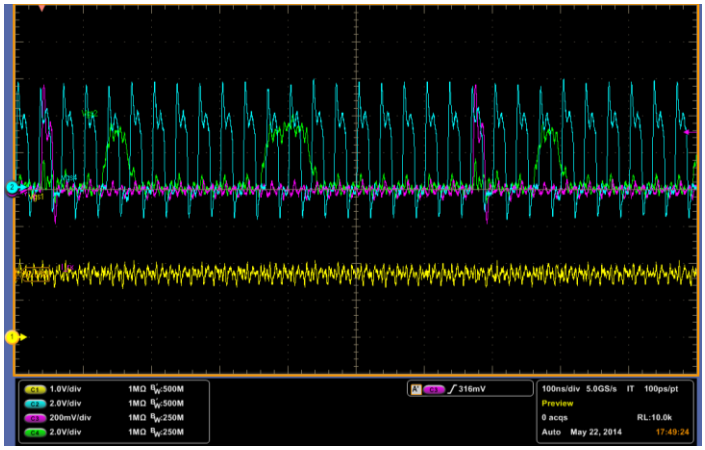


Fig. 98: Serial clock (blue), serial data (green), ADC input voltage (yellow), chip select signal (violet)

With a resolution of 3'3 mV, and the serial data got from Fig. 98 the conversion value is given by (23). Fig. 99 and Fig. 100 are showing in which moment is done the amplitude current sampling.

$$\text{ADC\_output (V)} = res.* (2^9 + 2^2 + 2^1) = 1'669\ V \qquad \textbf{(23)}$$

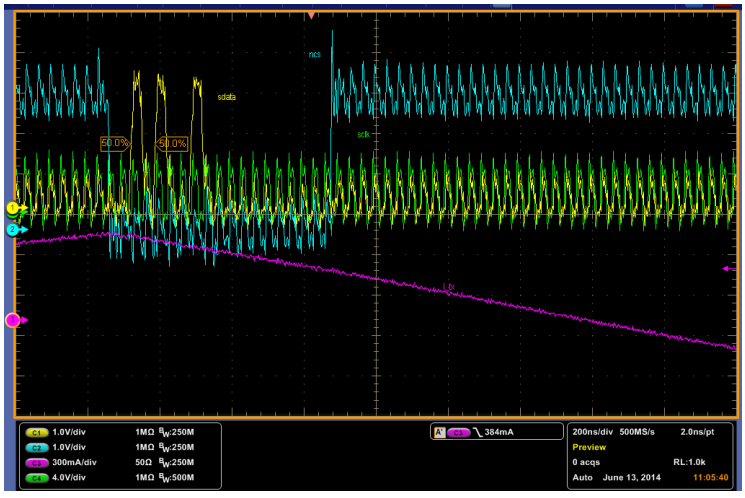


Fig. 99: : Chip select (blue), serial data (yellow), serial ADC clock (green), primary coil current (violet)

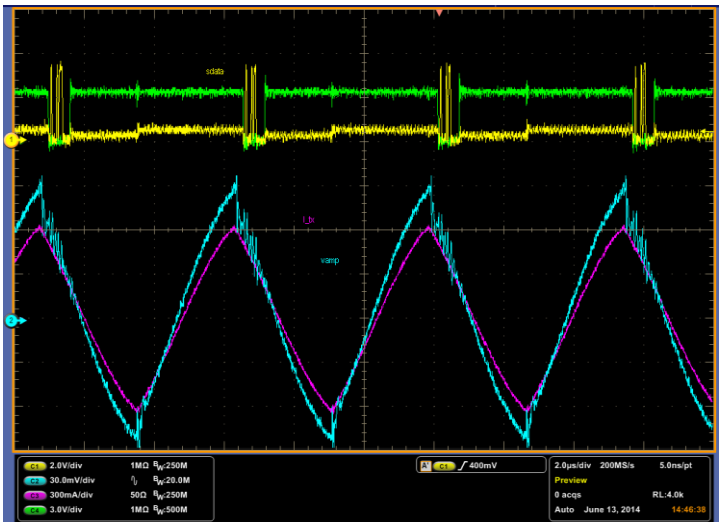


Fig. 100: Amplifier sensing output voltage (blue), serial data (yellow), chip select (green), primary coil current (violet)

5.2.3. Voltage and Current Coupling test

In this verification test, voltage and current coupling waveforms are measured [Fig. 102] and compared with the Spice simulations previously done [Fig. 101]. Test input parameters are defined:

- Input voltage -> 19 V
- Operating frequency -> 180 kHz
- Distance between coils -> 5 mm. (Coupling factor ≅ 0'49)
- Load resistance -> 47'1ohms (RLC receiver structure, without rectifier)

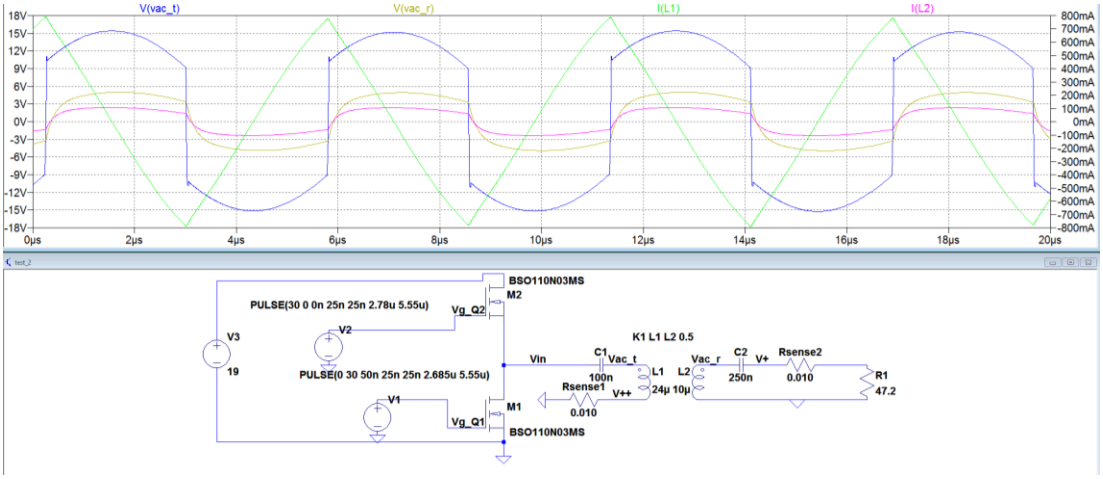


Fig. 101: Coupling waveforms simulations

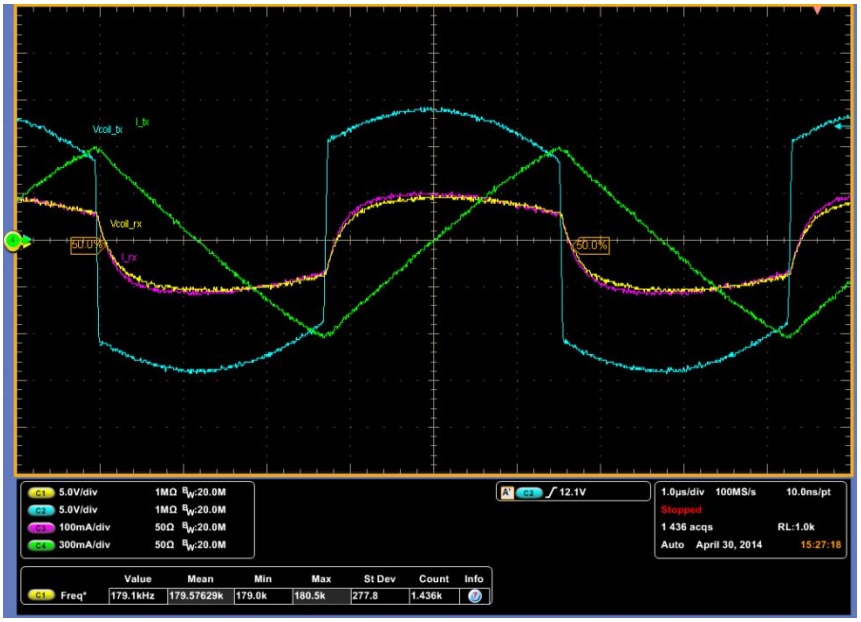


Fig. 102: Transmitter coupling voltage (blue), receiver coupled voltage (yellow), transmitter corrent (green), receiver current (violet)

As shown in the experimental results for a coupling factor of 0.5 the measurements fits with the simulations previously done.

5.2.4. ZCD and ZVD check

Verification of the detection of the zero-crossing current detection and zero-crossing voltage detection has been done [Fig. 103].

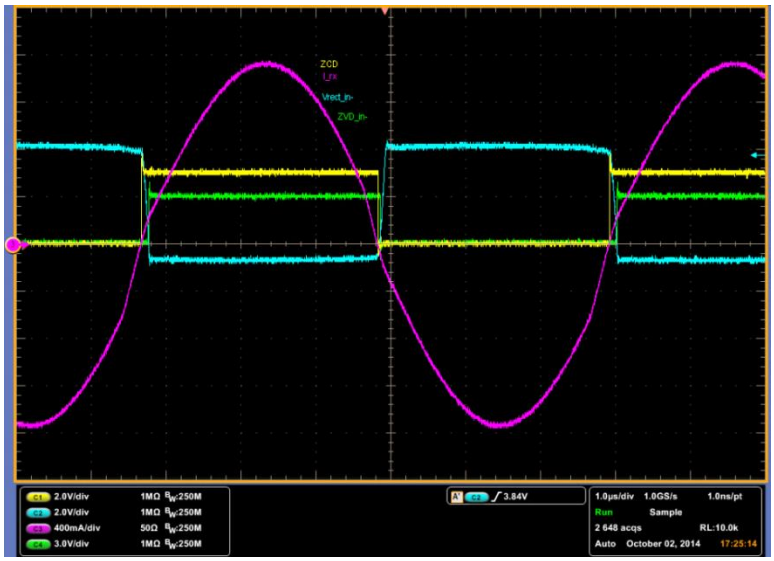


Fig. 103: Coil current (violet), rectifier input voltage referred to ground (blue), ZCD (yellow), ZVD (green)

5.2.5. Rectifier Output Voltage sensing

As for the transmitter current coil sensing a verification of the rectifier output voltage sensing has been done [Fig. 104] when 2 V are applied at the ADC input. The serial data conversion is toggling 1 bit which is not more than 16 mV.

Fig. 104: Rectifier output voltage ADC sensing. Serial ADC clock (yellow), chip select (blue), serial data (green)

With an ADC resolution of 16'1 mV and based on the results obtained output voltage value is given by:

$$\text{ADC\_output (V)} = res.* (2^7) = 2'063\ V \quad \textbf{(24)}$$

5.2.6. Clamping Control verification

Here the clamping control activation is shown for a specific range of voltage protection with hysteresis set with the FPGA (V_{TH} = 5'5 V, V_{TL} = 4 V). Fig. 105 is plotting the activation of the clamping signal once the output voltage reaches the high hysteresis voltage. This signal is turning on both NMOS transistors [Fig. 72] which clamps the rectifier input voltage when the input capacitors are connected to ground. Both NMOS transistors are remaining on till the rectifier output voltage reaches the low hysteresis voltage.

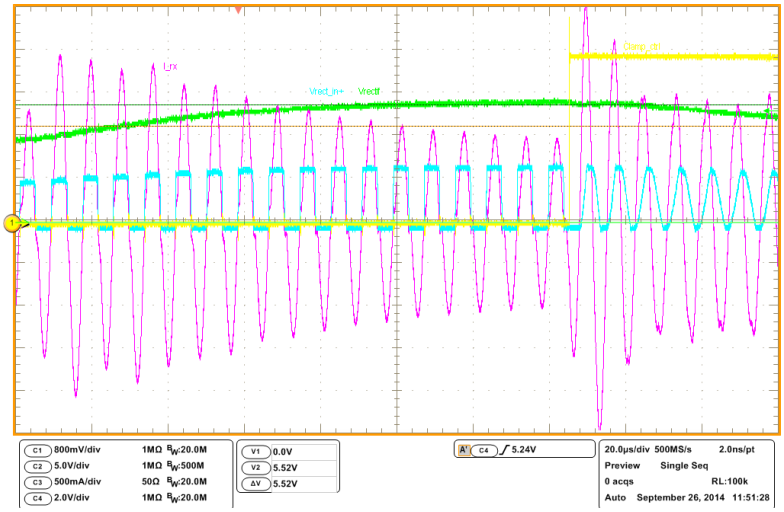


Fig. 105: Rectifier output voltage (C4 - green), rectifier input voltage referenced to ground (C2 - blue), clamping signal control (C1 - yellow), receiver coil current (C3 - violet)

5.3. Experimental WPT results

5.3.1. Passive Rectifier Test – Low Power

In the final product a certain load will be connected at the receiver output, most probably a DC-DC converter, which will adapt the output voltage to the convenient voltage. Therefore, a certain current-voltage will be required for the second stage. The main idea behind this test is to know how much DC power it is possible to transfer and on the other hand to get the DC

output voltage levels for different frequencies and coil distances. The target output power, defined by WPC, is to achieve 5 W.

In this measurement [Fig. 106] the 4 NMOS switches of the rectifier are driven passively, i.e. emulating the bridge diode, so there is no switching activity and gate switches are grounded. A control of the transmitter half bridge it is done sweeping the frequency from the 205 kHz to close to the resonant frequency. Input voltage is 19 V and the load current is also sweep from 25 mA up to 1 A. Distance between the transmitter coil (without magnet) and the receiver coils (with magnet) is fixed to 2 mm. In Fig. 107, the plot is showing the output power which the WPT system can give together with its efficiency for different operating frequencies. WPT efficiency is measured based on the input power give to the transmitter vs the output power which provides the receiver.

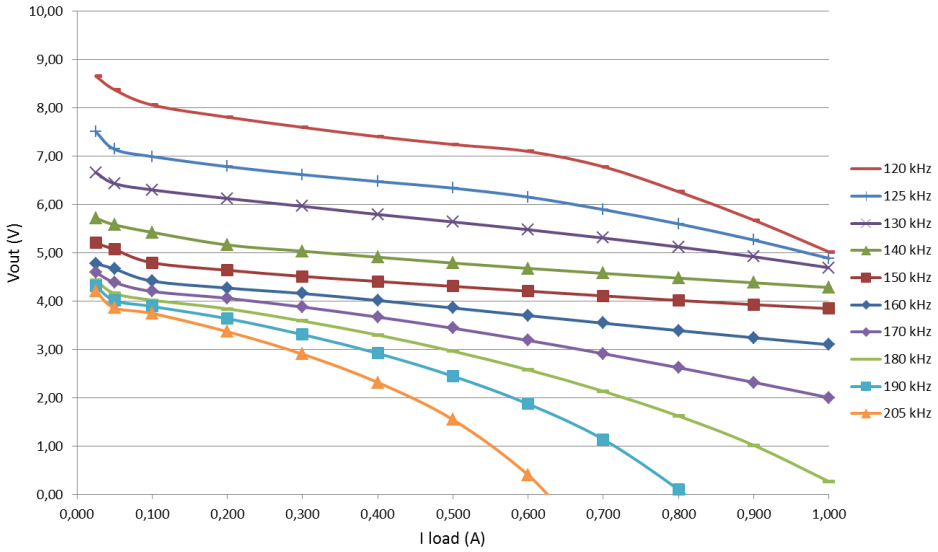


Fig. 106: Output rectifier voltage without rectifier control . D_{coil}[4] = 2 mm

[4] D_{coil}: stands for the coil separation distance

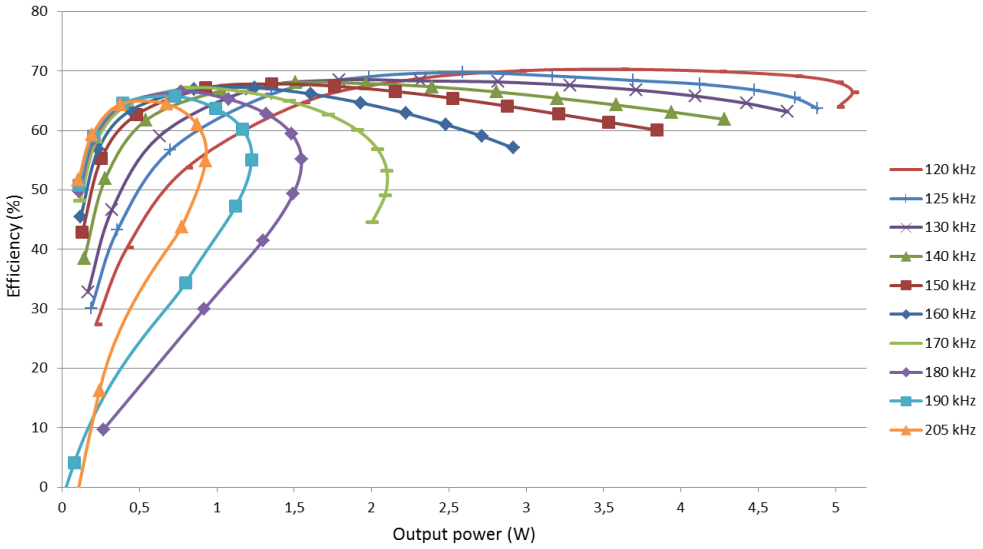


Fig. 107: WPT efficiency without rectifier control . D_{coil} = 2 mm

For the measurements a current source meter was used as a load. At high frequencies it is draining more current than what the system can give, that is why the output voltage goes to 0 and so as the efficiency. 5 W were achieved with an operating frequency of 120 kHz. Viewing plot [Fig. 107] the efficiency is much higher for low loads at higher frequencies; having as an example an output power demand of 400 mW approx., at 125 kHz the efficiency is just 40 % whereas with an operating frequency of 205 kHz the efficiency rises up to 65 %. On the other hand for high loads, frequencies close to resonance give higher efficiency. If a control it is implemented to obtain the optimum operating frequency higher efficiencies can be achieved for all loads.

These low efficiencies which are obtained are due to the losses of the diodes. Fig. 108 shows the measurement of the quasi square voltage waveform of the rectifier input and the rectifier output voltage. As it can be seen there a reduction of the output voltage due to the diodes voltage drops.

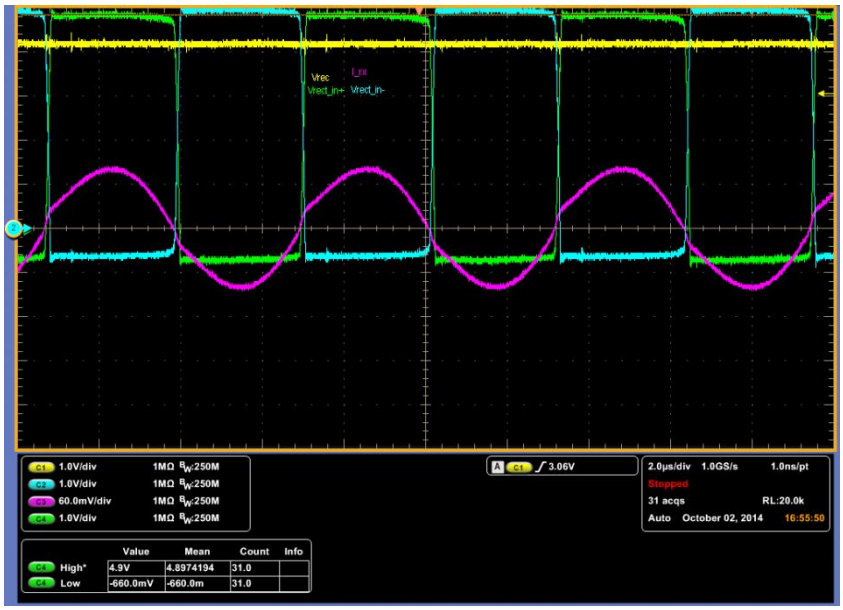


Fig. 108: Rectifier input signals (blue and green), rectifier output voltage (yellow), coil current (violet)

5.3.2. Passive Rectifier Test - Medium Power

This test pretends to reproduce the passive rectifier measurement with the same input parameters, but with the full bridge configuration in the transmitter to achieve higher output power with higher efficiencies. A comparison between low power and medium power is shown in Fig. 110 and Fig. 109 for coil separation distances, 2 and 5 mm respectively.

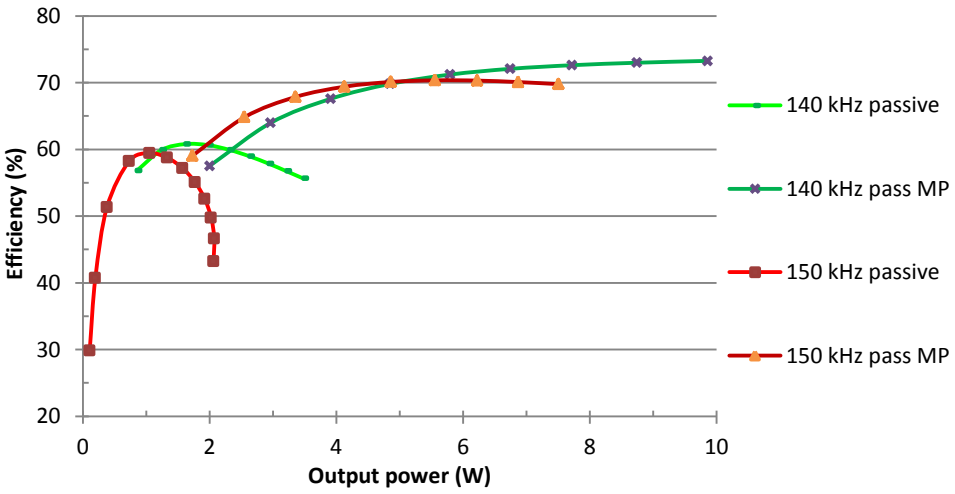


Fig. 109: WPT efficiency comparison between LP and MP without rectifier control . D_{coil} = 5 mm

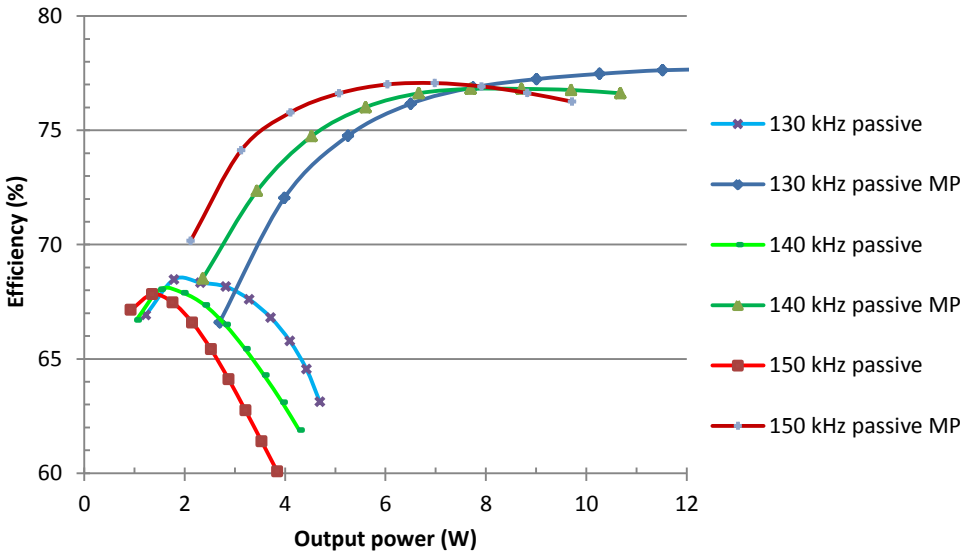


Fig. 110: WPT efficiency comparison between LP and MP without rectifier control . D_{coil} = 2 mm

5.3.3. Semi-Active Rectifier with Zero Crossing Current detection

In semi-active rectifier the low side switches are controlled by the information of the zero crossing receiver current where the upper NMOS transistors are switched off, i.e. leaving the body diodes to self-driven. Comparing to passive rectifier measurement better efficiency results are obtained [Fig. 111].

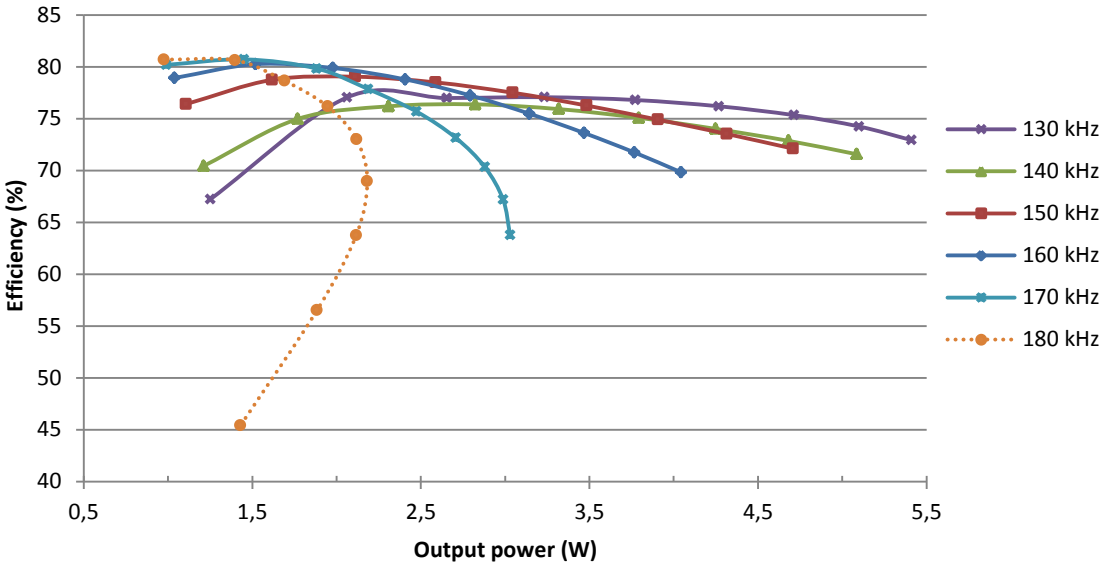


Fig. 111: WPT efficiency with the semi-active rectifier control . D_{coil} = 2 mm

5.3.4. Active Rectifier with Zero Crossing Current detection

When the full bridge is driven by the either the information by ZCD or ZVD even much higher voltages and efficiency can be achieved. Active rectifier has been achieved by ZCD and ZVD. Behaviours were similar but as already have been mentioned in some articles in state of art, problems with start-up appears with the ZVD. On simple way to solve this problem is to perform a passive start-up till the rectifier input voltage reaches a certain operative voltage level for the comparator.

Fig. 112 shows the effect of the synchronous rectification, since the rectifier output voltage levels is equal to the rectifier input voltage. Also no voltage drop is visible because of the diodes.

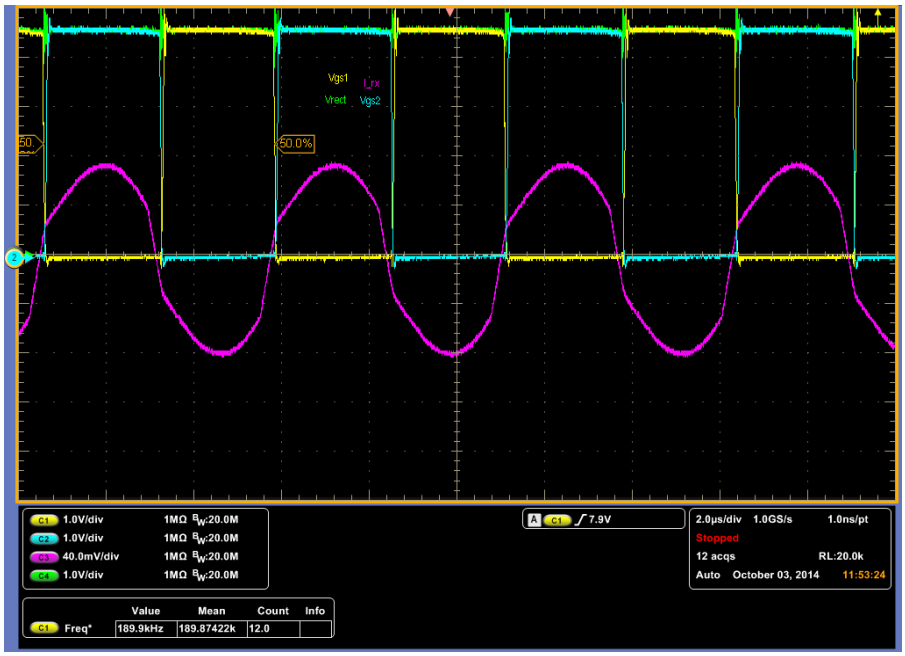


Fig. 112: Rectifier input signals (blue and yellow), rectifier output voltage (green), coil current (violet)

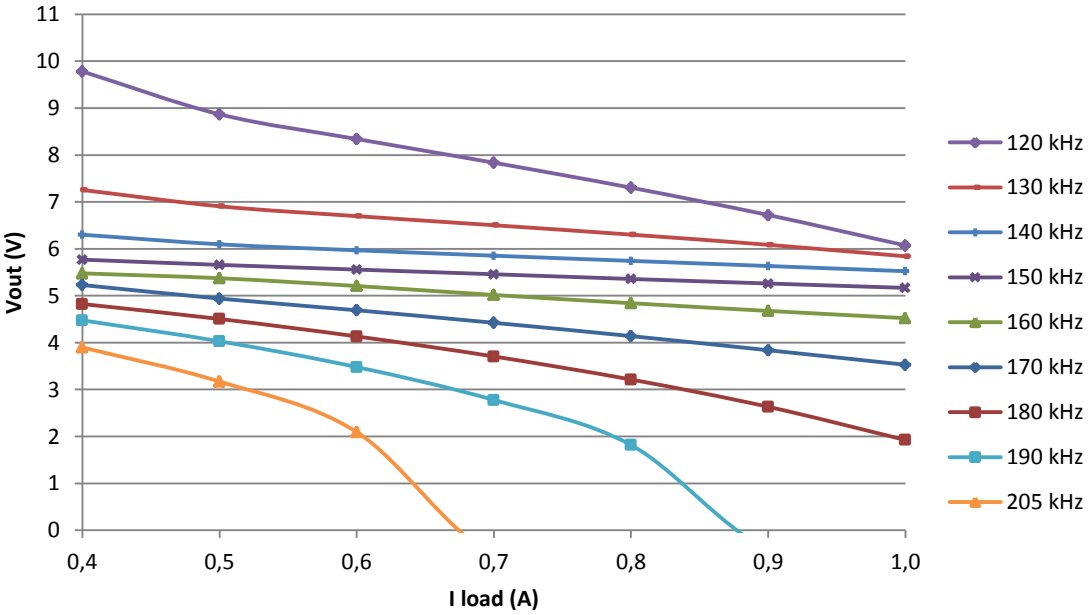


Fig. 113: Output rectifier voltage with the active rectifier control . D_{coil} = 2 mm

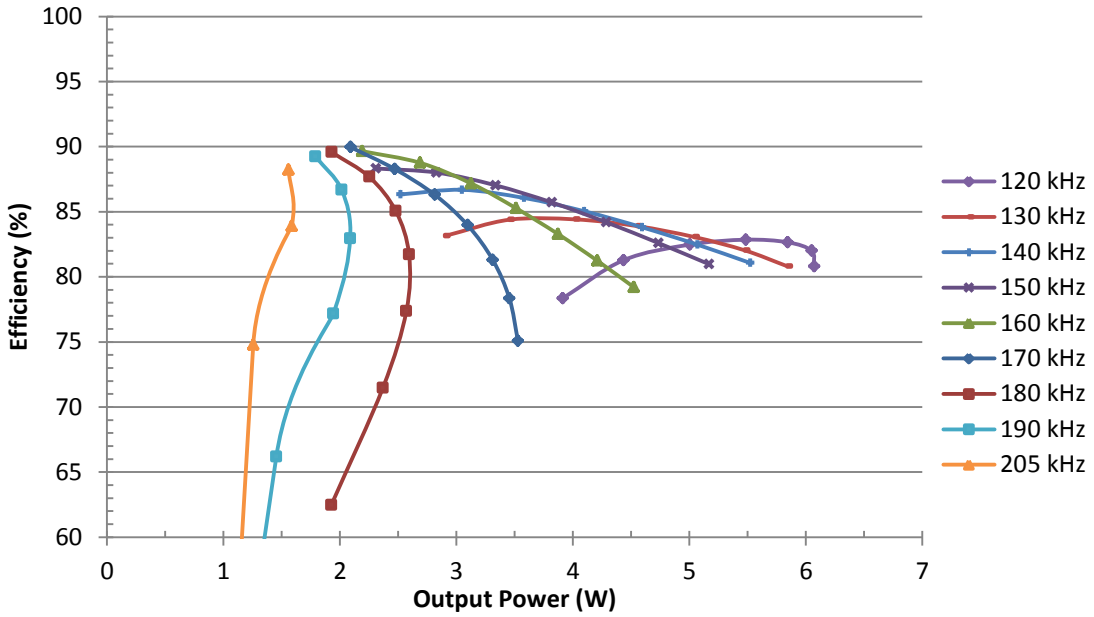


Fig. 114: WPT efficiency with the active rectifier control . D_{coil} = 2 mm

Fig. 115 is plotting an efficiency comparison with several the methods used and representing the big improvement of the synchronous rectification.

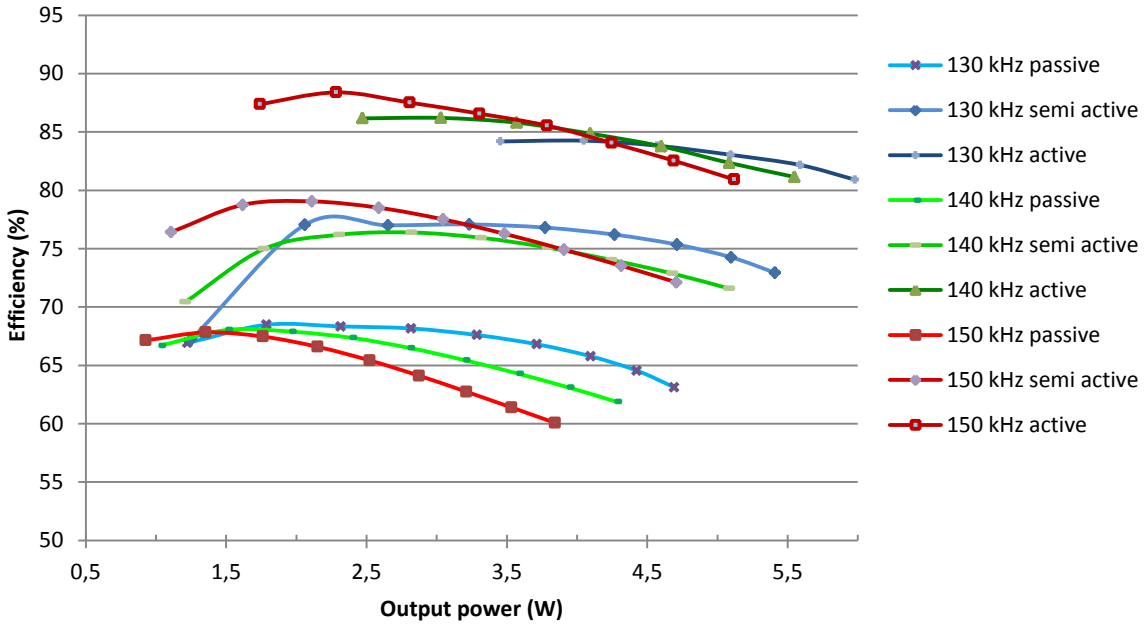


Fig. 115: WPT efficiency comparison between the rectifier controls . D_{coil} = 2 mm

Efficiency measurements to distances closer to the application (5 mm) are plotted in Fig. 116.

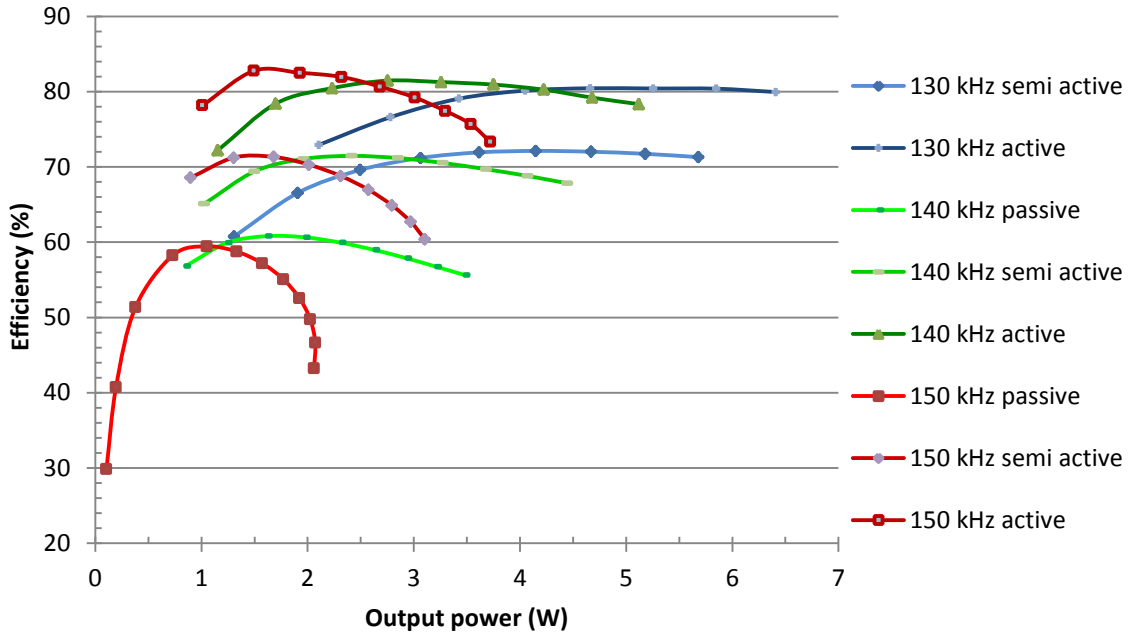


Fig. 116: WPT efficiency comparison between the rectifier controls . D_{coil} = 5 mm

5.3.5. ZVD and ZCD issue: more zero-crossing in the same cycle

For low loads and for frequencies close to the resonance, the current starts to behave not in a sinusoidal wave anymore and double, triple zero-crossing start to appear, see issue in Fig. 117 and Fig. 118. Two ways can be implemented to overdue this problem: switch to passive mode, but this would increase power losses, or the way which has been performed which is use a digital filter to skip these not desired detections. Fig. 118 is showing the rectifier gate switches commutation which is not affected by the double zero-crossing.

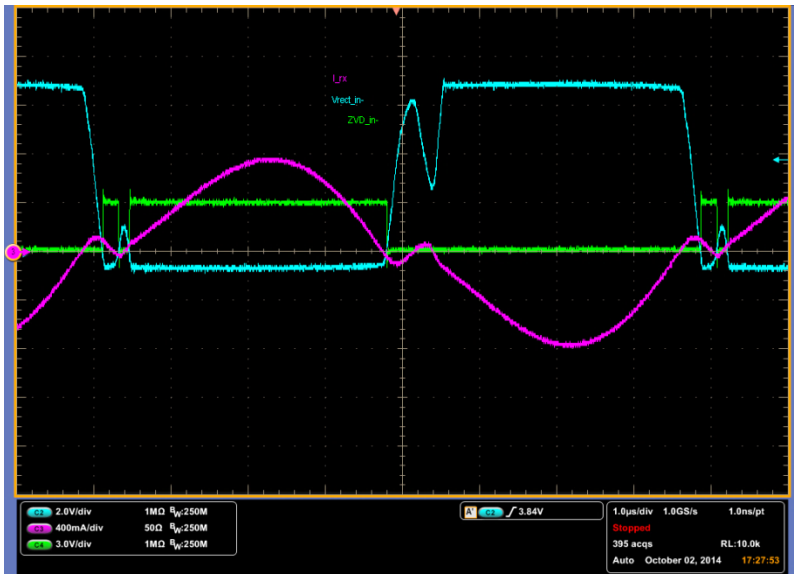


Fig. 117: Zero double crossing voltage with an operating frequency of 125 kHz and 400 mA load. Passive rectifier

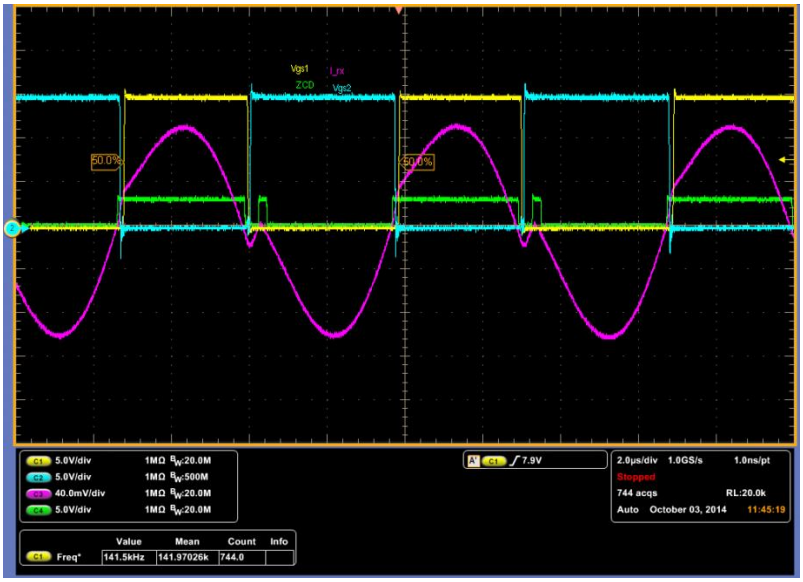


Fig. 118: Zero double crossing current with an operating frequency of 140 kHz and 400 mA load. Active rectifier

5.3.6. Stages efficiency measurements

The efficiency measurement of the WPT system implemented has been divided in stages to understand where the main power losses are present. The whole efficiency is mainly depending on [Fig. 119] and defined by (25):

- DC to AC power conversion ($\eta_{dc\text{-}ac}$): affected by the design of the half/full bridge.
- Link + the resonant circuit ($\eta_{link+res.}$): affected by the distance between the coils and the parasitic resistances of the resonant circuit.
- Rectifier ($\eta_{rectifier}$): affected by the design structure and control. It is the stage intended to reduce power losses.

$$\eta_{system} = \eta_{dc\text{-}ac} * \eta_{link} * \eta_{rectifier} \quad (25)$$

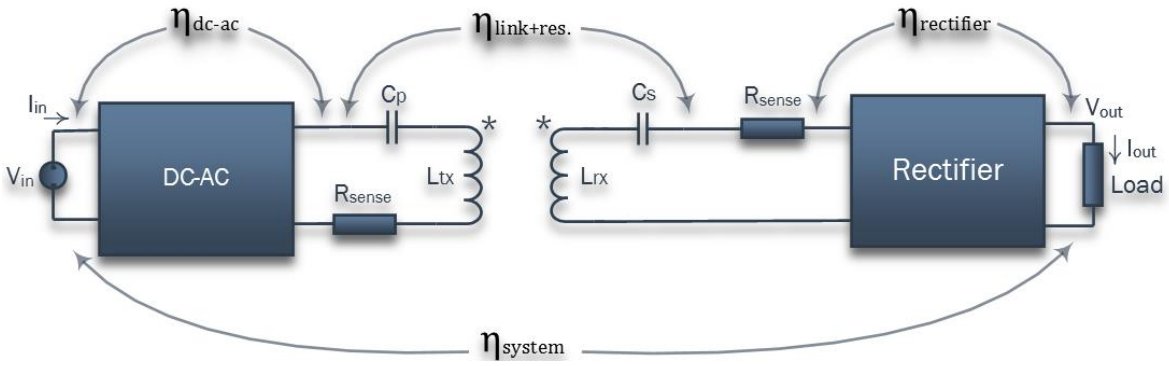


Fig. 119: WPT stages efficiencies

Table 8 shows the results of an efficiency measurement using a passive rectifier structure, where the operating frequency is 160 kHz and the distance between coils is 1 mm. Current load is set to 400 mA and input voltage is 19 V. Comparing to Table 9 where the rectifier it is controlled, the efficiency measurement of the WPT system having the same input parameters is 22 % lower. This important efficiency difference is only affected, as it can be seen in Table 10 and Table 11, because of the rectifier.

Freq.	160 kHz		Passive rectifier			
Coil distance	1 mm					
Vin: 19 V	Iin	130 mA	Pin	2,47 W	WPT Efficiency	68,5 %
I_{out} (load): 400 mA	Vout	4,24 V	Pout	1,69 W		

Table 8: WPT efficiency result when passive rectifier it is employed.

Freq.	160 kHz			Active rectifier		
Distance	1 mm					
Vin: 19 V	Iin	130 mA	Pin	2,47 W	WPT Efficiency	90,5 %
I_{out} (load) : 400 mA	Vout	5,63 V	Pout	2,25 W		

Table 9: WPT efficiency result when active rectifier it is employed.

P_{in}	$\eta_{dc\text{-}ac}$	$P_{dc\text{-}ac}$	$\eta_{link+res}$	$P_{in\_rectifier}$	$\eta_{rectifier}$	P_{out}
2,47 W	96,4 %	2,38 W	95 %	2,26 W	**74,9 %**	1,69 W

Table 10: Efficiency stage results using the passive rectifier

P_{in}	$\eta_{dc\text{-}ac}$	$P_{dc\text{-}ac}$	$\eta_{link+res}$	$P_{in\_rectifier}$	$\eta_{rectifier}$	P_{out}
2,47 W	96,4 %	2,38 W	95 %	2,26 W	**98,3 %**	2,25 W

Table 11: Efficiency stage results using the active rectifier

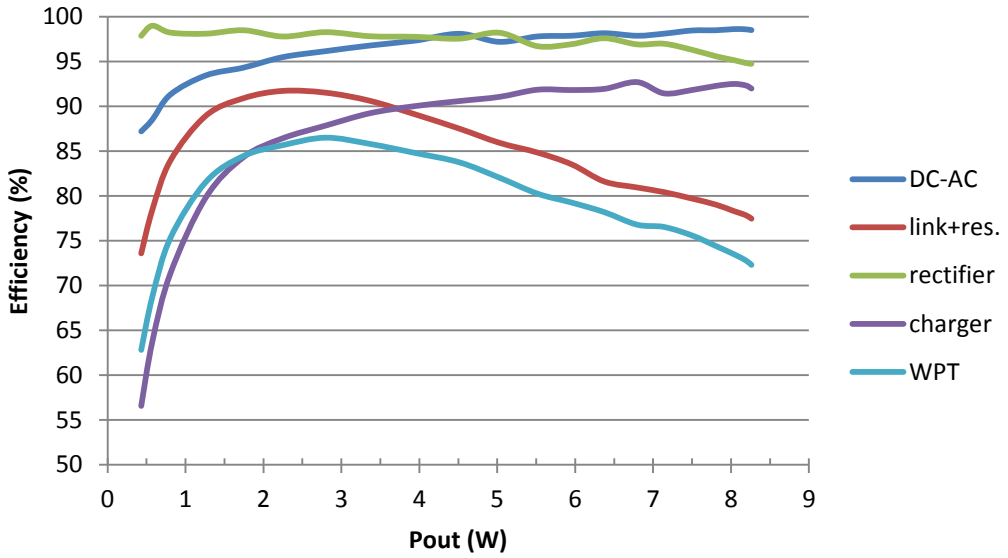


Fig. 120: WPT efficiency stages with an operating frequency of 140 kHz

5.3.7. Connection of a DC-DC charger as a load

A DC-DC charger has been connected to the output as a load to test the behavior of the whole system. The system was able to transfer and charge 5 W of power with efficiencies up to 76 % [see Fig. 121].

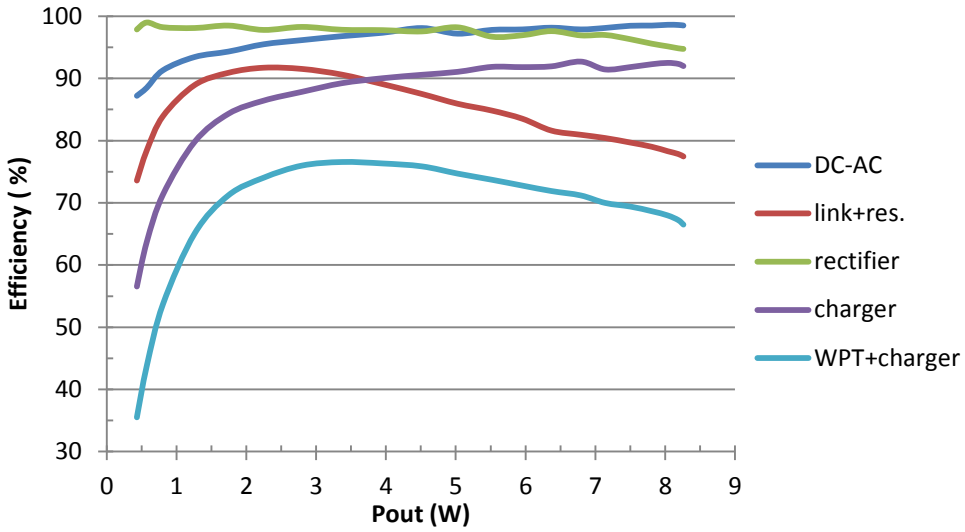


Fig. 121: WPT together with a charger efficiency for an operating frequency of 140 kHz

5.3.8. WPT prototype efficiency comparison with other prototypes

The efficiency results obtained with the WPT prototype implemented are compared with the results extract from [16]. Fig. 122 shows the efficiency of the researched prototype with an operating frequency of 150 kHz. Taking the defined low output power of the Qi standard, 5 W, the system is having efficiencies up to 75 % using a full-synchronous rectifier.

The proposed prototype in this project is showing higher efficiencies for an output power of 5 W, up to 80 % [Fig. 118], with a coupling factor of 0'65. However, if the power loses for the external components (MOSFET drivers, comparators, FPGA) is considered, see table [Table 12] then the efficiency is scaled down almost to 75 %,

	I_{DD} (mA)	V_{DD} (V)	Number	Power (mW)
TX Driver	2	12	2	48
RX Driver	3	18	2	108
IA	2	30	1	60
Comparator Vcc	15	3,3	1	49,5
Comparator -Vcc	8	-3,3	1	26,4
FPGA	30	5	1	150
TOTAL				**441,9**

Table 12: External components power losses

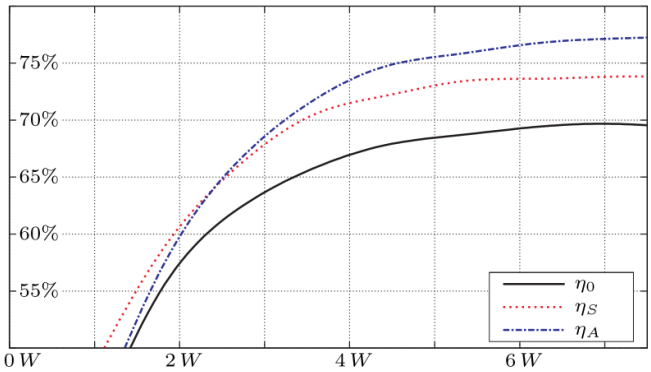


Fig. 122: Efficiency measurements. η_o is the efficiency with a passive rectifier, η_s is the efficiency with a semi-active rectifier, η_a is the efficiency with the proposed synchronous rectifier in [16]

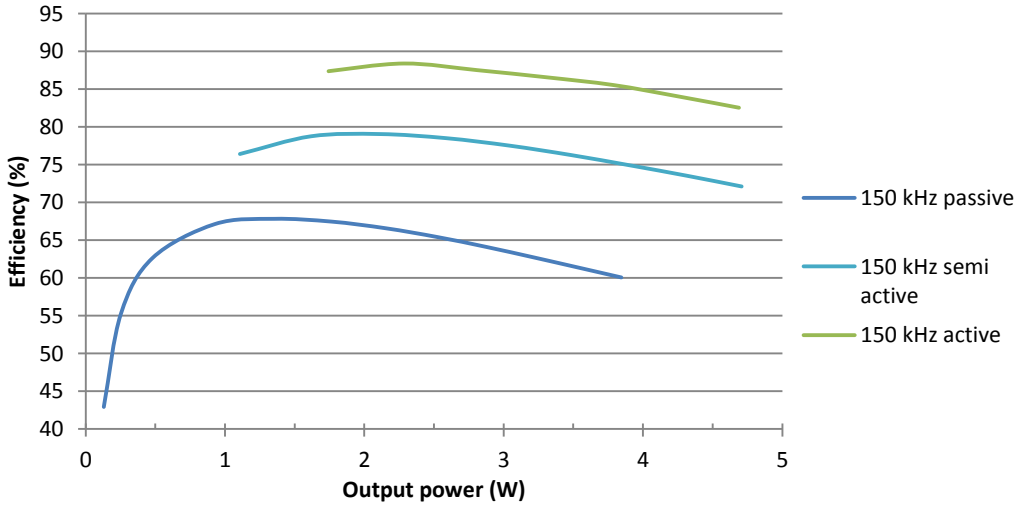


Fig. 123: WPT efficiency vs output power with a coil separation distance of 2 mm

6. CHAPTER VIII: Conclusion

The wireless transfer of energy is considered one of the most attractive new technologies and does have its place in future. Although this technology is still not widely applied for high level of electric power and large distance, there are signs that the research in this direction is intensive and has never stopped.

In this prototype implemented wireless power transfer was achieved via resonant inductive coupling between the transmitting and receiving coils in the near field (few mm). The WPT prototype implemented is able to transfer 5 W of power with efficiencies of 83 % and even higher efficiencies (> 90 %) for low output power [1 - 2 W]. An experimental measurement has been done connecting a DC-DC converter operating as a charger at the output and the system was able to charge a battery with efficiencies up to 75 %.

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8. Appendix

8.1. Transmitter and Receiver PCB problems, redesign and improvements

A PCB redesign of the boards designed (see appendix 8.4 and 8.5) has been done to solve/improve problems that have been found, view Table 13.

Issue	PCB	Change
Add input capacitor for the bridge	Tx	33 uF, 25 V
MAX15019B/A (U_1 and U_2) drivers get damage and inoperative after some time of use.	Tx	Driver HIP2100 IBZ (necessary level shifter)
Add reference voltage (1,65 V) for the AD8421 amplifier to shift the output voltage.	Tx	AD8603 buffer
For better performance a differential ADC can be used (U_3).	Tx	Not need to set a ref. voltage for the AD8421
NMOS clamping transistors connected otherwise (drain – source)	Rx	Powerful NMOS (PMV60EN)
Remove voltage dividers of the ZVD and ZCD circuitry. Bad operation.	Rx	R_1, R_5, R_2, R_6, R_{11}, R_{12}, R_{13}, R_{14}
Add capacitor to the input of the ADC to smooth the signal.	Rx	100 nF, 10 V
MAX4427 (U_5 and U_6) drivers get damage and inoperative after some time of use.	Rx	EL7202 (driving signals only up to 15 V)
Input ADC voltage divider	Rx	R_{27}=30 kΩ, R_{27}=7,5 kΩ
-3.3 V linear voltage regulator resistors	Rx	R_{37}=240 Ω, R_{38}=390 Ω
10 V linear voltage regulator resistors	Rx	R_{35}=1,1 kΩ, R_{36}=160 Ω
Not necessary 18 V linear voltage regulator	Rx	remove
ADC decoupling capacitor	Rx	C_{19}=1 uF
Resistors for 20 mV comparator hysteresis	Rx	R_3, R_4, R_{18}, R_{19} =160 Ω

Table 13: PCB's issues and improvements

8.2. VHDL code

8.2.1. Transmitter Power Conversion VHDL

```
----------------------------------------------------------------------------------
-
-- Engineer: Marc Martín Canellas
--
-- Create Date:    27/04/2014
-- Design Name:
-- Module Name:    PWM_HBridge - Behavioral
-- Project Name:   Wireless charging system
-- Description:
    -- Low and high side half bridge switches PWM control. Frequency configurable
using external push button from 100 kHz up to 205 kHz (10 kHz steps).
    -- Dead time set to 50 ns
----------------------------------------------------------------------------------

-- Libraries --
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- I/O Definition --
entity PWM_HBridge is
    Port (nReset          : in  std_logic; -- External push button reset
          clk_60MHz       : in  std_logic; -- External 60 MHz clock oscillator
          freq_push_button : in  std_logic; -- Freq. selector (Pull up input)
          current_tx_sample: out std_logic; -- Monitors the current sampling
          Hside_out       : out std_logic; -- High side switch control
          Lside_out       : out std_logic) -- Low side switch control
;
end PWM_HBridge;


architecture Behavioral of PWM_HBridge is

-- Signal declaration
-----------------------------------------------------------------

-- 60 MHz clock rising edge counter for the Hside control
signal cnt_clk_hs            : integer range 0 to 305 := 0;
-- 60 MHz clock rising edge counter for the Lside control
signal cnt_clk_ls            : integer range 0 to 305 := 0;
signal count_clock           : integer range 0 to 305 := 0;
signal Hside                 : std_logic;
signal Lside                 : std_logic;
signal freq_push_button_d    : std_logic;
signal freq_push_button_d2   : std_logic;

-- Type of state machine --
    -- One state for each frequency control
type state_type is (s_205kHz, s_190kHz, s_180kHz, s_170kHz, s_160kHz, s_150kHz,
s_140kHz, s_130kHz, s_120kHz, s_110kHz, s_100kHz);
signal freq_state: state_type;
-----------------------------------------------------------------
```

```
begin

process(clk_60MHz)
      begin
         if (clk_60MHz'event and clk_60MHz = '1') then
                cnt_clk_ls <= cnt_clk_ls + 1;
                cnt_clk_hs <= cnt_clk_hs + 1;

                -- external signal synchronization with the clock
                freq_push_button_d <= freq_push_button;
                freq_push_button_d2 <= freq_push_button_d;

                -- Reset --
                    -- Lside = GND, Hside = High
                    -- Initial frequency = 180 kHz
                    -- Dead time set to: 50 ns
                if(nReset = '0') then
                -- Set dead time and change duty cycle
                    cnt_clk_ls <= 3; -- 3*60_Clk = 50 ns
-- 6*60_Clk = 100 ns: dead time + increase low logic time (reduce duty cycle)
                    cnt_clk_hs <= 6;
                    Lside <= '0';
                    Hside <= '1';
                    freq_state <= s_180kHz;
                    count_clock <= 169;
                    freq_push_button_d <= '1';
                    freq_push_button_d2 <= '1';

                -- High side switch PWM
                elsif(cnt_clk_hs = count_clock) then
                    Hside <= not(Hside);
                    if(Hside = '0') then
                            cnt_clk_hs <= 6;
                        else
                            cnt_clk_hs <= 0;
                        end if;

                -- Low side switch PWM
                elsif(cnt_clk_ls = count_clock) then
                    Lside <= not(Lside);
                        if(Lside = '0') then
                            cnt_clk_ls <= 6;
                        else
                            cnt_clk_ls <= 0;
                        end if;

                -- falling edge detection -> change operating frequency
                elsif((freq_push_button_d2 and not(freq_push_button)) = '1')
then
        -- Define initial values for the switches after pressing the push button
                    Lside <= '0';
                    Hside <= '1';

                    -- Set dead time and change duty cycle
                    cnt_clk_ls <= 3;
                    cnt_clk_hs <= 6;

                    -- when frequency push button is pressed -> change of state:
```

```
                    -- change of operating frequency and update clock counter
                    case freq_state is
-- Count_clock = (60_Clk/freq_sel.)/2 + deadtime - 1{Count_clock init. value = 0}
                        when s_205kHz => count_clock <= 160;
                                         freq_state <= s_190kHz;
                        when s_190kHz => count_clock <= 169;
                                         freq_state <= s_180kHz;
                        when s_180kHz => count_clock <= 178;
                                         freq_state <= s_170kHz;
                        when s_170kHz => count_clock <= 190;
                                         freq_state <= s_160kHz;
                        when s_160kHz => count_clock <= 202;
                                            freq_state <= s_150kHz;
                        when s_150kHz => count_clock <= 216;
                                         freq_state <= s_140kHz;

                        when s_140kHz => count_clock <= 233;
                                         freq_state <= s_130kHz;

                        when s_130kHz => count_clock <= 252;
                                         freq_state <= s_120kHz;
                        when s_120kHz => count_clock <= 275;
                                         freq_state <= s_110kHz;
                        when s_110kHz => count_clock <= 302;
                                         freq_state <= s_100kHz;
                        when s_100kHz => count_clock <= 148;
                                         freq_state <= s_205kHz;
                        when others =>  count_clock <= 169;
                                         freq_state <= s_180kHz;
                    end case;
                end if;
        end if;
       end process;

Lside_out <= Lside;
Hside_out <= Hside;

-- start current ADC sampling -> sense I amplitude
current_tx_sample <= '1' when (cnt_clk_hs =  15 and Hside = '0') else '0';
end Behavioral;
```

8.2.2. Transmitter Coil Current ADC control VHDL

```
----------------------------------------------------------------------------------
-
-- Engineer: Marc Martín Canellas
--
-- Create Date:    20/05/2014
-- Design Name:
-- Module Name:    Curr_tx_ADC
-- Project Name:   Wireless charging system
-- Description:
    -- ADC control interface(ADCS7477 - 10 bit, 3 MSPS, serial communication) for
sensing the transmitter coil current
    -- Implementation of a 30 MHz Clock for the ADC.
    -- Data sampling
    -- Store the serial data conversion from the ADC in a 10 bit vector
    -- Include an end of conversion signal once the data vector is ready.
----------------------------------------------------------------------------------
-
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
    -- libraries for the shift left bit operator (shl)
use ieee.std_logic_arith.all;
use ieee.std_logic_unsigned.all;

-- I/O Define
entity Curr_tx_ADC is
    port(nReset           : in  std_logic; -- External push button reset
    clk_60MHz             : in  std_logic; -- External 60 MHz clock oscillator
    sdata_iADC            : in  std_logic; -- Serial data conversion from the ADC
    initiate_sample       : in  std_logic; -- Enable conversion signal
    sclk_iADC             : out std_logic; -- ADC 30 MHz clock
    ncs_iADC              : out std_logic; -- ADC chip select
    -- ADC data conversion vector
    iADC_data             : out std_logic_vector(9 downto 0);
    sample_ready_iADC     : out std_logic; -- ADC data conversion ready
-- Debugging pins
    out_bit9_iADC         : out std_logic;
    out_bit8_iADC         : out std_logic;
    out_bit7_iADC         : out std_logic;
    out_bit6_iADC         : out std_logic;
    out_bit5_iADC         : out std_logic;
    out_bit4_iADC         : out std_logic;
    out_bit3_iADC         : out std_logic;
    out_bit2_iADC         : out std_logic
        );
end Curr_tx_ADC;

architecture Behavioral of Curr_tx_ADC is

-- Signal declaration
-----------------------------------------------------------------
type machine is (initiation, conversion, eoc);
signal state                  : machine;
signal sclk_iADC_aux          : std_logic; -- sclk_iADC auxiliary clock signal
-- ADC auxiliar data storage
signal data_aux               : std_logic_vector(9 downto 0);
-- rising + falling edge ADC clock signal counter
```

```
signal cnt_sclk_iADC          : std_logic_vector(5 downto 0);
signal enable_sample          : std_logic;
-------------------------------------------------------------------

begin
-- Conversion
-------------------------------------------------------------------
process(clk_60MHz)
 begin
  if (clk_60MHz'event and clk_60MHz = '1') then

    -- Reset --
        -- Data conversion vector reset
        -- state -> beginning of conversion
     if(nReset = '0') then
        data_aux <= (others => '0');
        state <= initiation;
        enable_sample <= '0';

     elsif(initiate_sample = '1') then
        enable_sample <= '1';

     elsif(enable_sample = '1') then
         case state is
  -- initiation state: Chip select = high; conversion process begin on the
falling edge of ncs_iADC
           when initiation =>  if(sclk_iADC_aux = '0') then  -- to guaranty the
setup time after falling edge of ncs_iADC
                                        state <= conversion;
                                        data_aux <= (others => '0');
                                end if;

  -- conversion state: after 2 rise + 2 fall. edge of sclk_iADC, serial data
conversion coming from the ADC can be taken
            when conversion => if(cnt_sclk_iADC = "010110") then
                                        state <= eoc; -- system goes at the end
of conversion after catching the 10 bit data conversion

                               elsif(cnt_sclk_iADC > "000010" and sclk_iADC_aux =
'0') then -- data it is taken when sclk_iADC = low
                                        data_aux <= data_aux + sdata_iADC;

                               elsif(cnt_sclk_iADC > "000010" and sclk_iADC_aux =
'1') then -- data is shifted and stored when sclk_iADC = high
                                        data_aux <= shl(data_aux,"1");
                               end if;

              -- eoc(end of conversion):  Chip select = low
             when eoc => if(cnt_sclk_iADC = "100100") then -- -- necessary to
wait between conversions: tquiet > 63 ns 2*(sclk_iADC)
                                    state <= initiation;
                                    enable_sample <= '0';
                          end if;

            when others => null;
           end case;
             end if;
```

```
    end if;
-------------------------------------------------------------------------------
end process;

iADC_DATA <= data_aux;
-- data is ready at the end of conversion
sample_ready_iADC <= '1' when state = eoc else '0';
ncs_iADC <= '1' when state = initiation else '0'; -- chip select


-- Divider clock structure from 60 MHz to - 30 MHz (sclk_iADC)
-------------------------------------------------------------------------------
process(clk_60MHz)
      begin
         if (clk_60MHz'event and clk_60MHz = '1') then
                sclk_iADC_aux <= not(sclk_iADC_aux);

                if (nReset = '0') then
                    cnt_sclk_iADC <= (others => '0');
                    sclk_iADC_aux <= '1';

                elsif(state = initiation) then
                    cnt_sclk_iADC <= (others => '0');

                else
                    cnt_sclk_iADC <= cnt_sclk_iADC + '1';
                end if;
            end if;
      end process;
sclk_iADC <= sclk_iADC_aux;
-------------------------------------------------------------------------------


-- Structure for verification & debugging
-------------------------------------------------------------------------------
process(clk_60MHz)
      begin
         if (clk_60MHz'event and clk_60MHz = '1') then
                if(nreset = '0') then
                    out_bit9_iADC <= '0';
                    out_bit8_iADC <= '0';
                    out_bit7_iADC <= '0';
                    out_bit6_iADC <= '0';
                    out_bit5_iADC <= '0';
                    out_bit4_iADC <= '0';
                    out_bit3_iADC <= '0';
                    out_bit2_iADC <= '0';

                elsif(state = eoc) then
                    out_bit9_iADC <= data_aux(9);
                    out_bit8_iADC <= data_aux(8);
                    out_bit7_iADC <= data_aux(7);
                    out_bit6_iADC <= data_aux(6);
                    out_bit5_iADC <= data_aux(5);
                    out_bit4_iADC <= data_aux(4);
                    out_bit3_iADC <= data_aux(3);
                    out_bit2_iADC <= data_aux(2);
```

```
                end if;
            end if;
    end process;

end Behavioral;
```

8.2.3. Rectifier Output Voltage ADC control VHDL

```
----------------------------------------------------------------------------------
-
-- Engineer: Marc Martín Canellas
--
-- Create Date:    18/05/2014
-- Design Name:
-- Module Name:    Vrectif_ADC
-- Project Name:   Wireless charging system
-- Description:
    -- ADC control interface(ADCS7477 - 10 bit, 1 MSPS, serial communication) for
sensing the rectifier voltage.
    -- Implementation of a 10 MHz Clock for the ADC.
    -- Store the serial data conversion from the ADC in a 10 bit vector
    -- Include an end of conversion signal once the data vector is ready.
----------------------------------------------------------------------------------
-

-- Libraries --
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
    -- libraries for the shift left bit operator (shl)
use ieee.std_logic_arith.all;
use ieee.std_logic_unsigned.all;

-- I/O Define
entity Vrectif_ADC is
    port(nReset      : in  std_logic; -- External push button reset
      clk_60MHz      : in  std_logic; -- External 60 MHz clock oscillator
      sdata_vADC     : in  std_logic; -- Serial data conversion from the ADC
      sclk_vADC      : out std_logic; -- ADC 10 MHz clock
      ncs_vADC       : out std_logic; -- ADC chip select
-- ADC data conversion vector
      DATA_vADC      : out std_logic_vector(9 downto 0);
      sample_ready_vADC : out std_logic;  -- ADC data conversion ready
-- Debugging pins
      out_bit9_vADC  : out std_logic;
        out_bit8_vADC        : out std_logic;
        out_bit7_vADC        : out std_logic;
        out_bit6_vADC        : out std_logic;
        out_bit5_vADC        : out std_logic;
        out_bit4_vADC        : out std_logic;
        out_bit3_vADC        : out std_logic;
        out_bit2_vADC        : out std_logic
        );
end Vrectif_ADC;

architecture Behavioral of Vrectif_ADC is
```

```
-- Signals declaration
-----------------------------------------------------------------
type machine is (initiation, conversion, eoc);
signal state                        : machine;
signal sclk_vADC_aux      : std_logic;  -- sclk_vADC auxiliary clock signal
signal data_aux           : std_logic_vector(9 downto 0);
-- rising + falling edge ADC clock signal counter
signal cnt_sclk_vADC      : std_logic_vector(5 downto 0);
-- rising edge 60_Clk counter
signal cnt_clk            : integer range 0 to 2 := 0;
signal sclk_vADC_pre      : std_logic;
signal sclk_vADC_post     : std_logic;
signal sclk_vADC_rising_edge  : std_logic;
signal sclk_vADC_falling_edge : std_logic;
-----------------------------------------------------------------

begin
-- Falling/rising edge sclk_vADC detector
-----------------------------------------------
process(clk_60MHz)
      begin
         if (clk_60MHz'event and clk_60MHz = '1') then
            sclk_vADC_pre <= sclk_vADC_aux;
            sclk_vADC_post <= sclk_vADC_pre;
         end if;
end process;
sclk_vADC_falling_edge<= sclk_vADC_post and not(sclk_vADC_pre);
sclk_vADC_rising_edge <= sclk_vADC_pre and not(sclk_vADC_post);
-----------------------------------------------

-- Conversion
-----------------------------------------------------------------------
process(clk_60MHz)
   begin
     if (clk_60MHz'event and clk_60MHz = '1') then

             -- Reset --
                 -- Data conversion vector reset
                 -- state -> beggining of conversion
        if(nReset = '0') then
          data_aux <= (others => '0');
          state <= initiation;

          else
           case state is
             -- initiation state: Chip select = high; Conversion process begin on
the falling edge of ncs_vADC
             --  necessary to wait between conversions: tquiet > 50 ns
(sclk_vADC)
            when initiation => if(sclk_vADC_rising_edge = '1') then
                                state <= conversion;
                                -- data conversion reset
                                data_aux <= (others => '0');
                              end if;

             -- conversion state: Chip select = low
```

```
            -- after 3 rise + 3 fall. edge of sclk_vADC, serial data conversion
coming from the ADC can be taken
           when conversion => if (cnt_sclk_vADC > "000110" and
sclk_vADC_falling_edge= '1') then
                              data_aux <= data_aux + sdata_vADC; -- at the
sclk_vADC falling edge data it is taken

                            elsif( cnt_sclk_vADC > "000110" and
sclk_vADC_rising_edge = '1') then
                              data_aux <= shl(data_aux,"1");      -- at the
sclk_vADC rising edge data is shifted and stored

                                        -- system goes at the end of conversion
after catching the 10 bit data conversion
                            elsif(cnt_sclk_vADC = "011010") then
                                          state <= eoc;
                            end if;

            -- eoc(end of conversion):  Chip select = low
                when eoc =>  if(cnt_sclk_vADC >= "100000" and
sclk_vADC_rising_edge = '1' ) then
                                     state <= initiation;
                                end if;

           when others => null;
         end case;
           end if;
-------------------------------------------------------------------------------
    end if;
end process;

DATA_vADC <= data_aux;

-- data is ready at the end of conversion
sample_ready_vADC <= '1' when state = eoc else '0';
ncs_vADC <= '1' when state = initiation else '0'; -- chip select


-- Divider clock structure from 60 MHz to - 10 MHz (sclk_vADC)
-------------------------------------------------------------------------------
process(clk_60MHz)
      begin
         if (clk_60MHz'event and clk_60MHz = '1') then
            cnt_clk <= cnt_clk + 1;

                if (nReset = '0') then
                    cnt_clk <= 0;
                    cnt_sclk_vADC <= (others => '0');
                    sclk_vADC_aux <= '1';

            -- cnt_clk = 2 -> ( 60MHz_clock/sclk_vADC )/2 - 1. "-1" because
"cnt_clk initial_value = 0"
                elsif(cnt_clk = 2) then
                    sclk_vADC_aux <= not(sclk_vADC_aux);
                    cnt_clk <= 0;
```

```
                    -- reset of sclk_vADC counter once the conversion is ready
to start
                    if(state = initiation) then
                        cnt_sclk_vADC <= (others => '0');
                    else
                        cnt_sclk_vADC <= cnt_sclk_vADC + '1';
                    end if;
                end if;
            end if;
      end process;
sclk_vADC <= sclk_vADC_aux;
-------------------------------------------------------------------------------


-- Structure for verification & debugging
-------------------------------------------------------------------------------
process(clk_60MHz)
      begin
         if (clk_60MHz'event and clk_60MHz = '1') then
                if(nreset = '0') then
                    out_bit9_vADC <= '0';
                    out_bit8_vADC <= '0';
                    out_bit7_vADC <= '0';
                    out_bit6_vADC <= '0';
                    out_bit5_vADC <= '0';
                    out_bit4_vADC <= '0';
                    out_bit3_vADC <= '0';
                    out_bit2_vADC <= '0';

                elsif(state = eoc) then
                    out_bit9_vADC <= data_aux(9);
                    out_bit8_vADC <= data_aux(8);
                    out_bit7_vADC <= data_aux(7);
                    out_bit6_vADC <= data_aux(6);
                    out_bit5_vADC <= data_aux(5);
                    out_bit4_vADC <= data_aux(4);
                    out_bit3_vADC <= data_aux(3);
                    out_bit2_vADC <= data_aux(2);

                end if;
            end if;
    end process;
-------------------------------------------------------------------------------

end Behavioral;
```

8.2.4. ZCD Active rectifier VHDL

```
----------------------------------------------------------------------------------
-
-- Engineer: Marc Martín Canellas
--
-- Create Date:    9/05/2014
-- Design Name:
-- Module Name:    ActRectifier
-- Project Name:   Wireless charging system
-- Description:
    -- Rectifier switching control depending on the ZCD signal (zero crossing
current detection)
    -- Dead time set to 66,67 ns
    -- Possibility tu turn on/off the rectifier control with an external switch
----------------------------------------------------------------------------------
-

-- Libraries
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Define I/O
entity ActRectifier is
    Port ( nReset         : in  STD_LOGIC; -- External push button reset
           clk_60MHz      : in  STD_LOGIC; -- External 60 MHz clock oscillator
           ZCD            : in STD_LOGIC;  -- Zero crossing current signal
        -- External switch to turn on/off active rectification ctrl
           ActRect_off    : in STD_LOGIC;
        -- Rectifier switches: SW1 & SW2 high side; SW3 & SW4 low side
           SW1_out        : out  STD_LOGIC;
           SW2_out        : out  STD_LOGIC;
           SW3_out        : out  STD_LOGIC;
           SW4_out        : out  STD_LOGIC
            );
end ActRectifier;


architecture Behavioral of ActRectifier is

-- Signal declaration
-------------------------------------------------------------------
    -- Auxiliary rectifier signals switches: SW1 & SW2 high side; SW3 & SW4 low
side
signal SW1                : std_logic;
signal SW2                : std_logic;
signal SW3                : std_logic;
signal SW4                : std_logic;
signal ZCD_d     : std_logic; -- zero crossing current detection delayed
signal ZCD_d2    : std_logic; -- zero crossing current detection 2 Tclk delayed
signal ZCD_d3    : std_logic; -- zero crossing current detection 3 Tclk delayed
-- 60 MHz clock counter: 16,667 * 300 = 5000 us (max half period)
signal cnt_clk   : integer range 0 to 300 := 0;
signal cnt_SW3   : integer range 0 to 300 := 0;
signal cnt_SW4   : integer range 0 to 300 := 0;
signal timer_SW2 : integer range 0 to 300 := 0;
signal timer_SW1 : integer range 0 to 300 := 0;
```

```
-- Type of state machine.
type state_type is (SW4_ON, SW3_ON, dead_time1, dead_time2, initial);
signal SW_state: state_type;

constant Tclk_DeadTime : integer := 4;  -- 16,67 ns * 4 = 66,67 ns
-- cnt_clk > 59 : ZCD signal filtering (1 MHz)  ; cnt_clk > 99 (600 kHz)
constant Tclk_Filter : integer := 59;
constant Tclk_Filter_high : integer := 299;    -- 299 = 5 us ->  4.5 us, 269
constant Tclk_SW4vsSW1_delay : integer := 3;
constant Tclk_SW3vsSW2_delay : integer := 3;
-------------------------------------------------------------------------

begin
process(clk_60MHz)
      begin
         if (clk_60MHz'event and clk_60MHz = '1') then
                cnt_clk <= cnt_clk + 1;

                -- signal synchronization to avoid metastability
                ZCD_d3 <= ZCD_d2;
                ZCD_d2 <= ZCD_d;
                ZCD_d <= ZCD;

                -- Reset --
                    -- All switches -> OFF
                    -- Switching control off
                    -- After enable active rect. control -> SW2 -> ON
                    -- ZCD filtering signal OFF
                if(nReset = '0') then
                    SW_state <= initial;
                    cnt_clk <= 59;           -- ZCD filter off
                    SW3 <= '0';
                    SW4 <= '0';
                    cnt_clk <= 0;
                    ZCD_d2 <= ZCD;
                    ZCD_d <= ZCD;
                    ZCD_d3 <= ZCD;
                    cnt_SW3 <= 0;
                    cnt_SW4 <= 0;
                    timer_SW2 <= 0;
                    timer_SW1 <= 0;


                elsif (ActRect_off = '0') then
                -- active rectification is enabled
                    case SW_state is
                    -- check current direction to decide which rectifier
switches should turn on
                        when initial => SW4 <= '0';
                                        SW3 <= '0';

                                        if(ZCD_d = '1') then
                                            SW_state <= SW4_ON;

                                        else
                                            SW_state <= SW3_ON;
                                        end if;
```

```
                    -- SW3 together with SW2 is turned on
                        when SW3_ON => SW4 <= '0';
                                       SW3 <= '1';
                                       cnt_SW3 <= cnt_SW3 + 1;

                                       -- ZC rising edge detection, ZCD
signal filtering (1 MHz)  ; cnt_clk > 99 (600 kHz)
                                       if( ((ZCD_d and not(ZCD_d2)) = '1')
and  cnt_clk > Tclk_Filter) then
                                            SW_state <= dead_time1;
                                            cnt_clk <= 0;
                                            timer_SW2 <= cnt_SW3 -
Tclk_SW3vsSW2_delay;

                                       elsif(cnt_clk > Tclk_Filter_high)
then
                                            SW_state <= dead_time1;

                                       else
                                            SW_state <= SW3_ON;
                                       end if;


                        when dead_time1 =>   SW4 <= '0';
                                             SW3 <= '0';
                                             cnt_SW3 <= 0;

                                             if(cnt_clk >=
Tclk_DeadTime) then
                                                  SW_state <= SW4_ON;
                                                  cnt_clk <= 0;
                                             end if;

                        when SW4_ON => SW4 <= '1';
                                       SW3 <= '0';
                                       cnt_SW4 <= cnt_SW4 +1;

                                       -- falling edge
                                       if( ((ZCD_d2 and not(ZCD_d)) = '1')
and  cnt_clk > Tclk_Filter) then
                                            SW_state <= dead_time2;
                                            cnt_clk <= 0;
                                            timer_SW1 <= cnt_SW4 -
Tclk_SW4vsSW1_delay;

                                       elsif(cnt_clk > Tclk_Filter_high)
then
                                            SW_state <= dead_time2;

                                       else
                                            SW_state <= SW4_ON;
                                       end if;

                        when dead_time2 =>   SW4 <= '0';
                                             SW3 <= '0';
                                             cnt_SW4 <= 0;
```

```
                                                    if(cnt_clk >=
Tclk_DeadTime) then
                                                        SW_state <= SW3_ON;
                                                        cnt_clk <= 0;
                                                    end if;

                        when others => SW_state <= SW3_ON;
                                                   cnt_clk <= 0;
                    end case;

            -- active rectification is disabled
                else
                    SW_state <= initial;
                    SW3 <= '0';
                    SW4 <= '0';
                end if;
        end if;
end process;

SW2 <= SW3;
SW1 <= SW4;

SW1_out <= SW1;
SW2_out <= SW2;

SW3_out <= SW3;
SW4_out <= SW4;

  end Behavioral;
```

8.2.5. ZVD Active rectifier VHDL

```
  ----------------------------------------------------------------------------
---
  -- Engineer: Marc Martín Canellas
  --
  -- Create Date:    9/05/2014
  -- Design Name:
  -- Module Name:    ActRectifier
  -- Project Name:   Wireless charging system
  -- Description:
    -- Rectifier switching control depending on the ZVD_in+ signal (zero crossing
current detection)
    -- Dead time set to 100 ns
    -- Possibility tu turn on/off the rectifier control with an external push
button
  ----------------------------------------------------------------------------
---

  -- Libraries
  library IEEE;
  use IEEE.STD_LOGIC_1164.ALL;

  -- Define I/O
  entity ActRectifier is
      Port ( nReset      : in  STD_LOGIC; -- External push button reset
             clk_60MHz   : in  STD_LOGIC; -- External 60 MHz clock oscillator
               ZVD_in_p       : in STD_LOGIC;  -- Zero voltage detection signal
               ZVD_in_n       : in STD_LOGIC;  -- Zero voltage detection signal
           -- External push button to turn on/off active rectification
             ActRect_off  : in STD_LOGIC;
               SW1_out        : out  STD_LOGIC;-- rectifier switches: SW1 & SW4
        connected together
             SW2_out          : out  STD_LOGIC;-- SW2 & SW3 connected together
               SW3_out        : out  STD_LOGIC;
               SW4_out        : out  STD_LOGIC
               );
  end ActRectifier;


  architecture Behavioral of ActRectifier is

  -- Signal declaration
  ----------------------------------------------------------------
  signal SW1              : std_logic;
  signal SW2              : std_logic;
  signal SW3              : std_logic;
  signal SW4              : std_logic;
  signal ZVD_in_p_d  : std_logic; -- zero crossing current detection delayed
  -- zero crossing current detection 2 Tclk delayed
  signal ZVD_in_p_d2 : std_logic;
  -- zero crossing current detection 3 Tclk delayed
  signal ZVD_in_p_d3 : std_logic;
  -- zero crossing current detection delayed
  signal ZVD_in_n_d  : std_logic;
```

```
  -- zero crossing current detection 2 Tclk delayed
  signal ZVD_in_n_d2 : std_logic;
  -- zero crossing current detection 3 Tclk delayed
  signal ZVD_in_n_d3 : std_logic;
  signal enable      : std_logic;                          --       enable/disable
active rectification signal
  --signal cnt_clk       : integer range 0 to 300 := 0;    --    60    MHz    clock
counter: 16,667 * 300 = 5000 us (max period/2)
  signal cnt_clk         : integer range 0 to 1000 := 0;
  signal cnt_SW3         : integer range 0 to 300 := 0;
  signal cnt_SW4         : integer range 0 to 300 := 0;
  signal timer_SW2       : integer range 0 to 300 := 0;
  signal timer_SW1       : integer range 0 to 300 := 0;
  -- Type of state machine.
  type state_type is (SW4_ON, SW3_ON, dead_time1, dead_time2, initial);
  signal SW_state: state_type;

  constant Tclk_DeadTime : integer := 4;  -- 16,67 ns * 4 = 66,67 ns
  -- cnt_clk > 59 : ZVD_in+ signal filtering (1 MHz)  ; cnt_clk > 99 (600 kHz)
  constant Tclk_Filter : integer := 59;
  constant Tclk_SW4vsSW1_delay : integer := 5;
  constant Tclk_SW3vsSW2_delay : integer := 5;
  ------------------------------------------------------------------------

  begin
  process(clk_60MHz)
        begin
           if (clk_60MHz'event and clk_60MHz = '1') then
                 cnt_clk <= cnt_clk + 1;

                 -- signal synchronization to avoid metastability
                 ZVD_in_p_d3 <= ZVD_in_p_d2;
                 ZVD_in_p_d2 <= ZVD_in_p_d;
                 ZVD_in_p_d <= ZVD_in_p;

                ZVD_in_n_d3 <= ZVD_in_n_d2;
                 ZVD_in_n_d2 <= ZVD_in_n_d;
                 ZVD_in_n_d <= ZVD_in_n;

                 -- Reset --
                     -- All switches -> OFF
                     -- Switching control off
                     -- After enable active rect. control -> SW2 -> ON
                     -- ZVD_in+ filtering signal OFF
                 if(nReset = '0') then
                     SW_state <= initial;
                     cnt_clk <= 59;            -- ZVD_in+ filter off
                     SW3 <= '0';
                     SW4 <= '0';
                     cnt_clk <= 0;
                     ZVD_in_p_d2 <= ZVD_in_p;
                     ZVD_in_p_d <= ZVD_in_p;
                     ZVD_in_p_d3 <= ZVD_in_p;

                     ZVD_in_n_d2 <= ZVD_in_n;
                     ZVD_in_n_d <= ZVD_in_n;
                     ZVD_in_n_d3 <= ZVD_in_n;
                     cnt_SW3 <= 0;
```

```
                    cnt_SW4 <= 0;
                    timer_SW2 <= 0;
                    timer_SW1 <= 0;


                -- active rectification is enabled
                elsif (ActRect_off = '0') then
                --else
                    case SW_state is
                        when initial => SW4 <= '0';
                                        SW3 <= '0';
                                         if(ZVD_in_p_d = '1') then
                                            SW_state <= SW3_ON;
                                         else
                                            SW_state <= SW4_ON;
                                         end if;

                        when SW3_ON => SW4 <= '0';
                                        SW3 <= '1';
                                        cnt_SW3 <= cnt_SW3 + 1;
                                        -- cnt_clk > 59 : ZVD_in+ signal
filtering (1 MHz)  ; cnt_clk > 99 (600 kHz)
                                        -- ZVD_in+ falling edge detection -
> dead time
                                        if(        ((ZVD_in_p_d2        and
not(ZVD_in_p_d)) = '1') and  cnt_clk > Tclk_Filter) then
                                        -- risin_edge
                                        --if(        ((ZVD_in_p_d        and
not(ZVD_in_p_d2)) = '1') and  cnt_clk > Tclk_Filter) then
                                            SW_state <= dead_time1;
                                            cnt_clk <= 0;
                                            timer_SW2    <=    cnt_SW3    -
Tclk_SW3vsSW2_delay;
                                        else
                                            SW_state <= SW3_ON;
                                        end if;

                        when dead_time1 => SW4 <= '0';
                                            SW3 <= '0';
                                            cnt_SW3 <= 0;
                                            if(cnt_clk   >=   Tclk_DeadTime)
then
                                                SW_state <= SW4_ON;
                                                cnt_clk <= 0;
                                            end if;

                        when SW4_ON => SW4 <= '1';
                                        SW3 <= '0';
                                        cnt_SW4 <= cnt_SW4 +1;
                                        -- rising edge ZVD_in+ detection
                                        --if(        ((ZVD_in_n_d        and
not(ZVD_in_n_d2)) = '1') and  cnt_clk > Tclk_Filter) then
                                        -- falling edge
                                        if(        ((ZVD_in_n_d2        and
not(ZVD_in_n_d)) = '1') and  cnt_clk > Tclk_Filter) then
                                            SW_state <= dead_time2;
                                            cnt_clk <= 0;
```

```
                                                timer_SW1    <=    cnt_SW4    -
Tclk_SW4vsSW1_delay;
                                            else
                                                SW_state <= SW4_ON;
                                            end if;

                        when dead_time2 => SW4 <= '0';
                                                SW3 <= '0';
                                                cnt_SW4 <= 0;
                                                if(cnt_clk   >=   Tclk_DeadTime)
then
                                                    SW_state <= SW3_ON;
                                                    cnt_clk <= 0;
                                                end if;
                        when others => SW_state <= initial;
                                            cnt_clk <= 0;
                    end case;

                    -- active rectification is disabled
                else
                    SW_state <= initial;
                    SW3 <= '0';
                    SW4 <= '0';
                end if;
        end if;
    end process;

    SW2 <= SW3;
    SW1 <= SW4;

    SW1_out <= SW1;
    SW2_out <= SW2;

    SW3_out <= SW3;
    SW4_out <= SW4;

    end Behavioral;
```

8.3. Datasheets

8.3.1. iADC timing specifications

Symbol	Parameter	Conditions	Typical	Limits	Units
$t_{CONVERT}$			16 x t_{SCLK}		
t_{QUIET}	(Note 5)			**50**	ns (min)
t_1	Minimum $\overline{CS}$ Pulse Width			**10**	ns (min)
t_2	$\overline{CS}$ to SCLK Setup Time			**10**	ns (min)
t_3	Delay from $\overline{CS}$ Until SDATA TRI-STATE® Disabled (Note 6)			**20**	ns (max)
t_4	Data Access Time after SCLK Falling Edge(Note 7)	V_{DD} = +2.7 to +3.6		**40**	ns (max)
		V_{DD} = +4.75 to +5.25		**20**	ns (max)
t_5	SCLK Low Pulse Width			**0.4 x t_{SCLK}**	ns (min)
t_6	SCLK High Pulse Width			**0.4 x t_{SCLK}**	ns (min)
t_7	SCLK to Data Valid Hold Time	V_{DD} = +2.7 to +3.6		**7**	ns (min)
		V_{DD} = +4.75 to +5.25		**5**	ns (min)
t_8	SCLK Falling Edge to SDATA High Impedance (Note 8)	V_{DD} = +2.7 to +3.6		**25** **6**	ns (max) ns (min)
		V_{DD} = +4.75 to +5.25		**25** **5**	ns (max) ns (min)
$t_{POWER-UP}$	Power-Up Time from Full Power-Down		1		µs

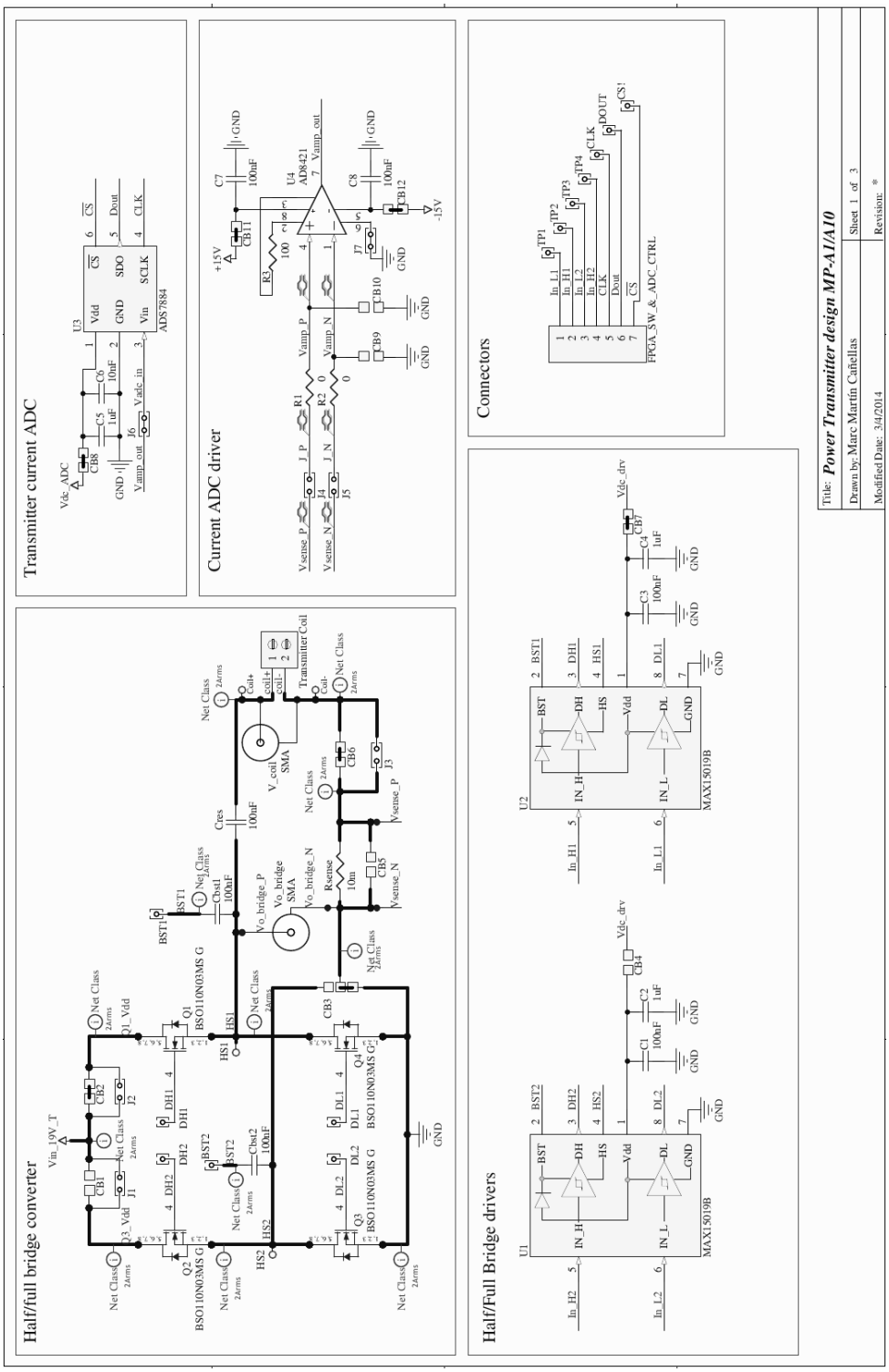
Fig. 124: ADCS7477 ADC timing specifications (V_{DD} = +2.7 V to 5.25 V, fsclk = 20 MHz)

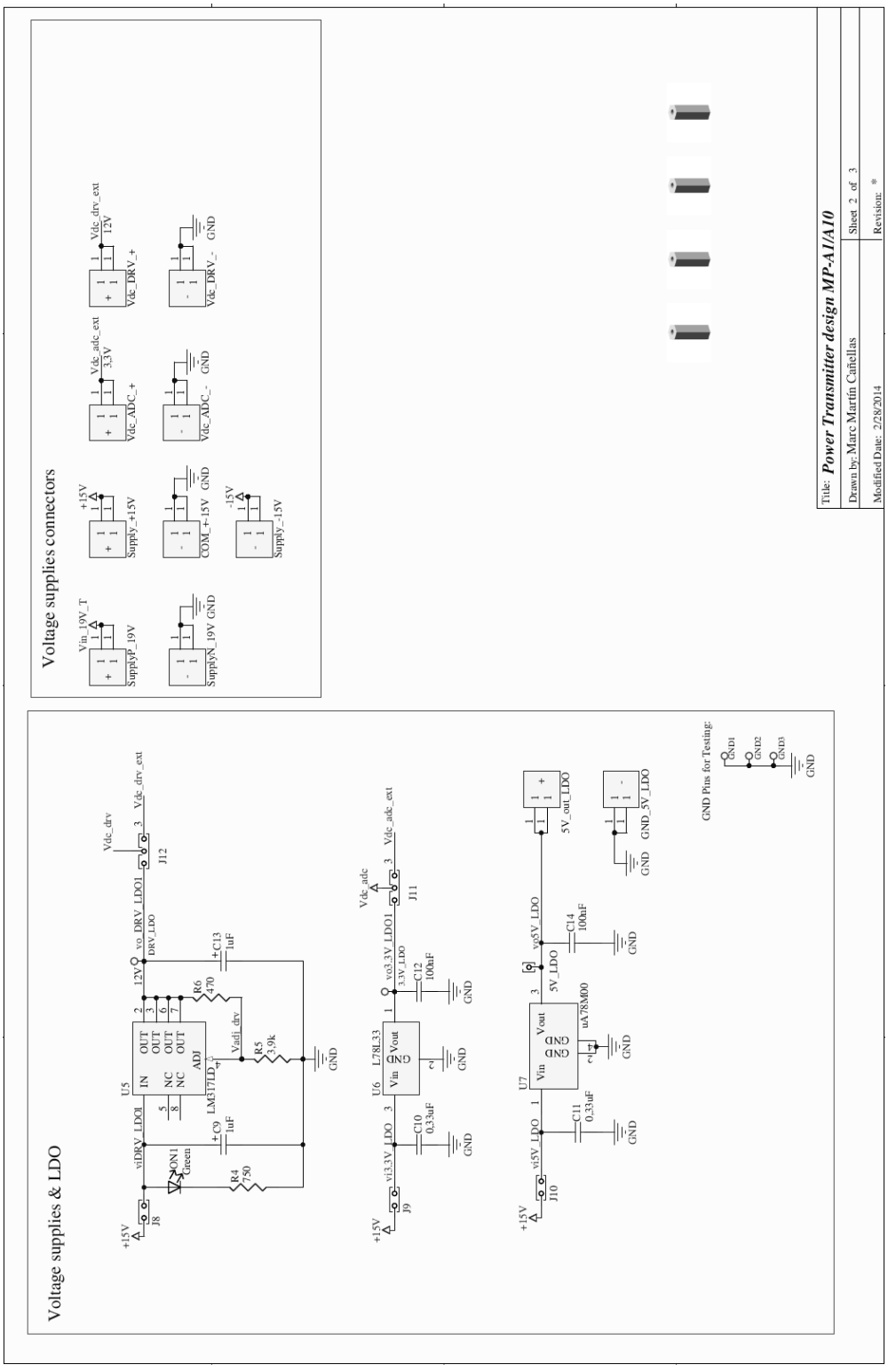
8.3.2. vADC timing specifications

PARAMETER			TEST CONDITIONS[1]	MIN	TYP	MAX	UNIT
t_{conv}	Conversion time	ADS7884	V_{DD} = 3 V			11.5 × t_{SCLK}	ns
			V_{DD} = 5 V			11.5 × t_{SCLK}	
		ADS7885	V_{DD} = 3 V			9.5 × t_{SCLK}	
			V_{DD} = 5 V			9.5 × t_{SCLK}	
t_{acq}	Aquisition time		V_{DD} = 3 V	62.5			ns
			V_{DD} = 5 V	52			
t_q	Minimum quiet time needed from bus 3-state to start of next conversion		V_{DD} = 3 V	10			ns
			V_{DD} = 5 V	10			
t_{d1}	Delay time, $\overline{CS}$ low to first data (0) out		V_{DD} = 3 V		9	15	ns
			V_{DD} = 5 V		8	11	
t_{su1}	Setup time, $\overline{CS}$ low to SCLK low		V_{DD} = 3 V	7			ns
			V_{DD} = 5 V	5			
t_{d2}	Delay time, SCLK falling to SDO		V_{DD} = 3 V		11	20	ns
			V_{DD} = 5 V		9	12	
t_{h1}	Hold time, SCLK falling to data valid[2]		V_{DD} < 3 V	5.5			ns
			V_{DD} > 5 V	4			
t_{d3}	Delay time, 16th SCLK falling edge to SDO 3-state		V_{DD} = 3 V		9	15	ns
			V_{DD} = 5 V		8	11	
t_{w1}	Pulse duration, $\overline{CS}$		V_{DD} = 3 V	10			ns
			V_{DD} = 5 V	10			
t_{d4}	Delay time, $\overline{CS}$ high to SDO 3-state,		V_{DD} = 3 V		9	15	ns
			V_{DD} = 5 V		8	11	
t_{wH}	Pulse duration, SCLK high		V_{DD} = 3 V	0.45 × t_{SCLK}			ns
			V_{DD} = 5 V	0.45 × t_{SCLK}			
t_{wL}	Pulse duration, SCLK low		V_{DD} = 3 V	0.45 × t_{SCLK}			ns
			V_{DD} = 5 V	0.45 × t_{SCLK}			
	Frequency, SCLK		V_{DD} = 3 V			40	MHz
			V_{DD} = 5 V			48	
t_{d5}	Delay time, second falling edge of clock and $\overline{CS}$ to enter in powerdown (use min spec not to accidently enter in powerdown) Figure 3		V_{DD} = 3 V	–2		4	ns
			V_{DD} = 5 V	–2		3	

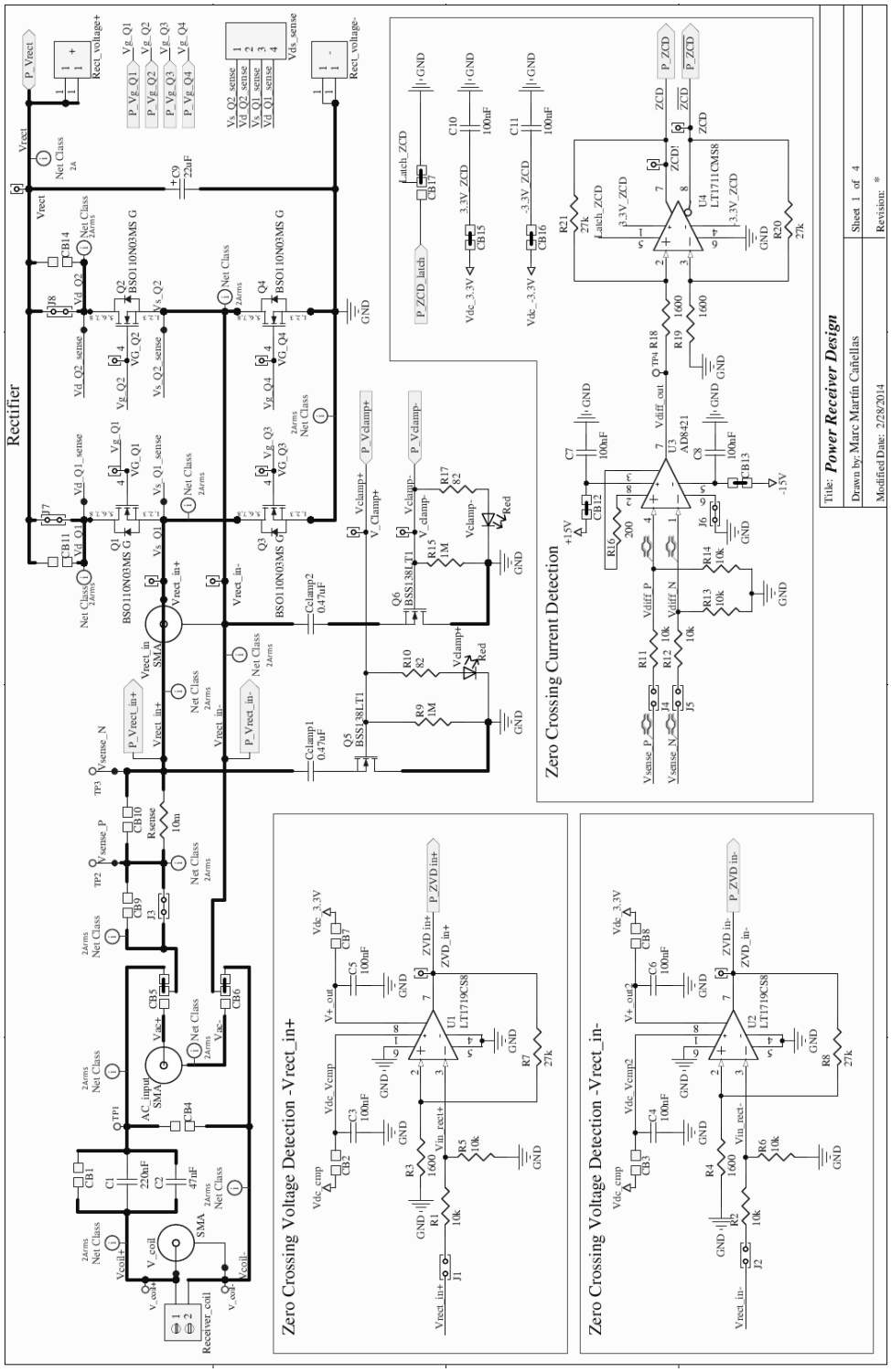
Fig. 125: ADS7884 ADC timing specifications (V_{DD} = +2.5 V to 5.5 V)

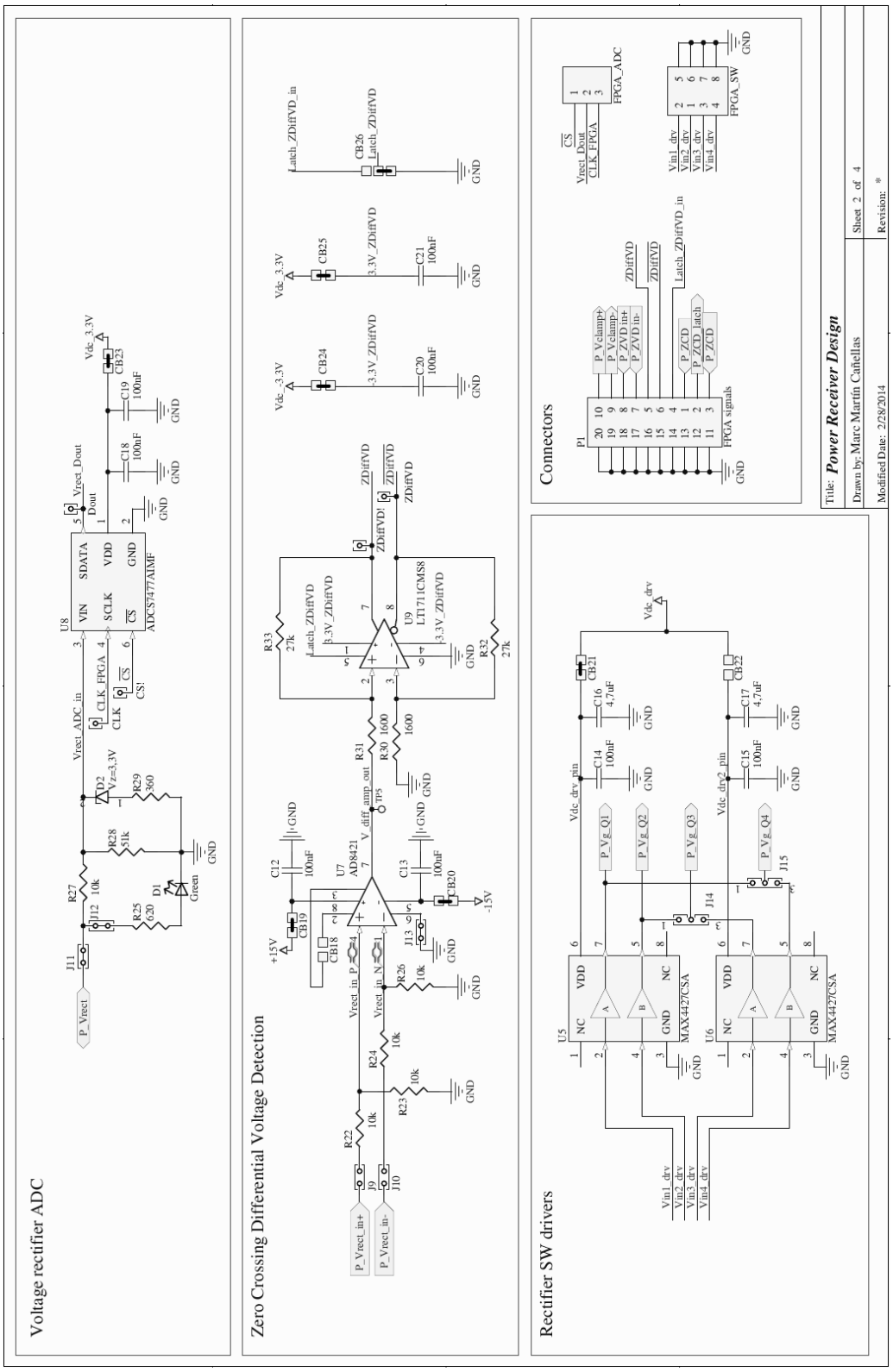
8.4. Power Transmitter schematic

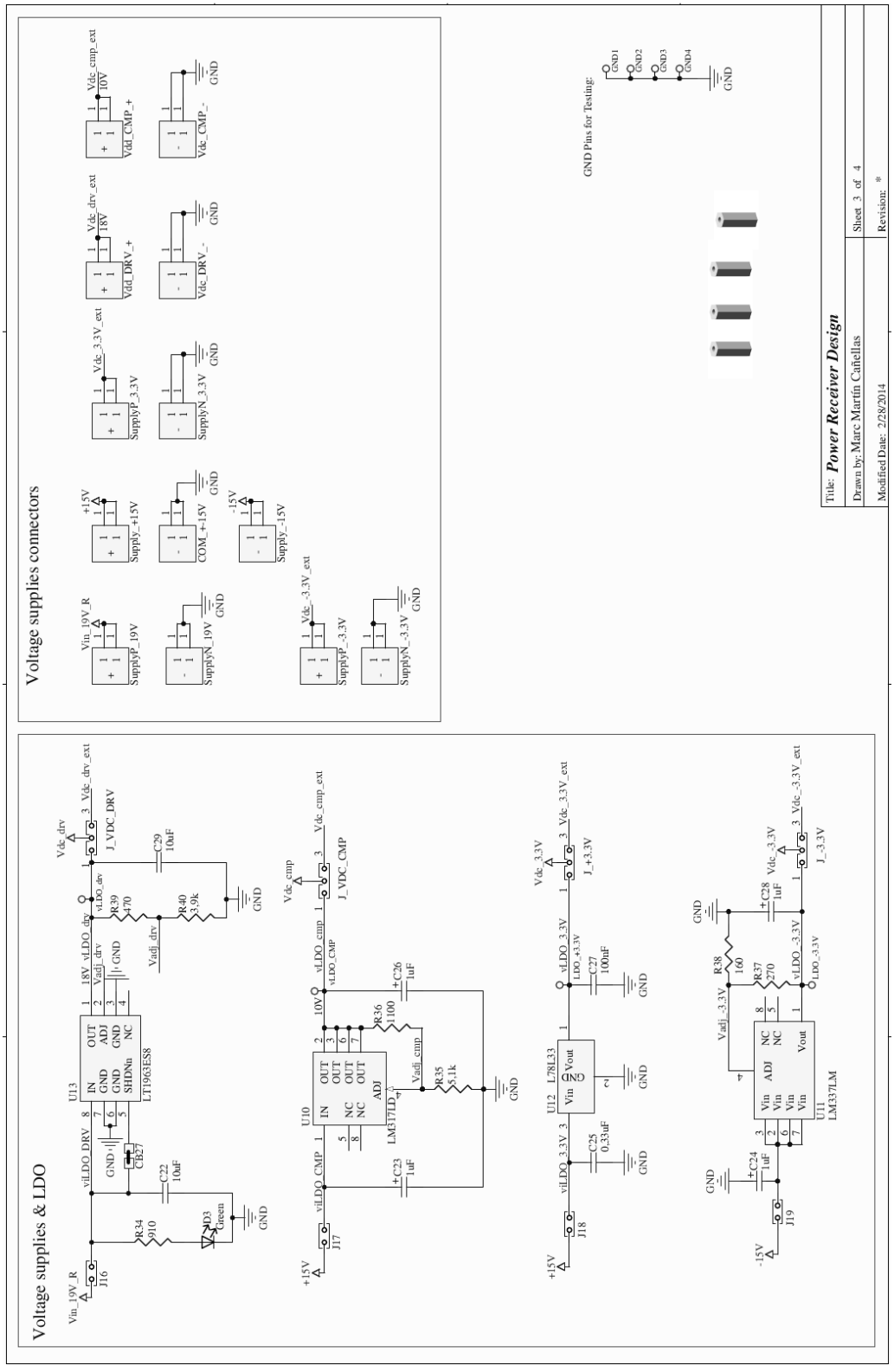



Voltage supplies connectors
Vin_19V_T
SupplyP_19V
SupplyN_19V
GND
+15V
Supply_+15V
COM_+15V
GND
-15V
Supply_-15V
Vdc_adc_ext
3.3V
Vdc_ADC_+
Vdc_ADC_-
GND
Vdc_drv_ext
12V
Vdc_DRV_+
Vdc_DRV_-
GND
Voltage supplies & LDO
Vdc_drv
Vdc_drv_ext
J12
vo_DRV_LDO1
DRV_LDO
12V
U5
LM317LD
IN
OUT
NC
ADJ
vi15V_LDO1
J8
+15V
ON1
Green
R4
750
R6
470
C13
1uF
C9
1uF
Vadj_drv
R5
3.9k
GND
Vdc_adc
Vdc_adc_ext
J11
vo3.3V_LDO1
3.3V_LDO
U6
L78L33
Vin
GND
Vout
vi3.3V_LDO
J9
C10
0.33uF
C12
100nF
U7
uA78M00
vo5V_LDO1
5V_LDO
vi5V_LDO
J10
C11
0.33uF
C14
100nF
5V_out_LDO
GND_5V_LDO
GND Pins for Testing:
GND1
GND2
GND3
Title: Power Transmitter design MP-A1/A10
Drawn by: Marc Martín Cañellas
Sheet 2 of 3
Modified Date: 2/28/2014
Revision: *

8.5. Power Receiver schematic




Voltage rectifier ADC
Zero Crossing Differential Voltage Detection
Rectifier SW drivers
Connectors
Title: Power Receiver Design
Drawn by: Marc Martín Cañellas
Sheet 2 of 4
Modified Date: 2/28/2014
Revision: *


Voltage supplies & LDO
Voltage supplies connectors
Vin_19V_R
SupplyP_19V
SupplyN_19V
COM_+15V
Supply_+15V
Supply_-15V
Vdc_3.3V_ext
SupplyP_3.3V
SupplyN_3.3V
Vdc_drv_ext
Vdd_DRV_+
Vdc_DRV_-
Vdc_cmp_ext
Vdd_CMP_+
Vdc_CMP_-
GND Pins for Testing:
GND1
GND2
GND3
GND4
Title: Power Receiver Design
Drawn by: Marc Martín Cañellas
Sheet 3 of 4
Modified Date: 2/28/2014
Revision: *
LT1963ES8
LM337LM
LM317LD
L78L33
J_VDC_DRV
J_VDC_CMP
J_+3.3V
J_-3.3V

9. Annex

9.1. FPGA pinout

Signal	Type I/O	Vhdl Name	Length	WPT board label	FPGA board pin	FPGA pin board name	Characteristics
System clock	Input	Clk	1 bit	-	A8	osci_60MHz	60 MHz
System reset	Input	Reset	1 bit	- R1	RESET_PWR_DOWN_N	Pullup pin	
Curr Tx ADC block (ADS7884)							
Serial data ADC	Input	sdata_iadc	1 bit	Dout	H13	WDOG_SERVE	
ADC Serial clock	Output	sclk_iadc	1 bit	CLK G1	RESET_ALL_N	30 MHz	
ADC chip select	Output	ncs_iadc	1 bit	CS!	G16	MON_1	
Parallel data ADC conversion	internal	iadc_data	10 bits	- -			
Enable_sample	internal	initiate_sample	1 bit	-	-		
PWM tx block							
Frequency selector	Input	Freq_selection	1 bit	-	L1	SW1_FPGA	Pull up pin
Q1 Low side gate	Output	DL1_PWM	1 bit	In_L1 D15	PMU_CTRL_2		
Q4 Low side gate	Output	DH1_PWM	1 bit	In_H1	F15	PMU_CTRL_1	
Q2 Low side gate	Output	DL2_PWM	1 bit	In_L2 E3	SSC_RST_N		
Q3 Low side gate	Output	DH2_PWM	1 bit	In_H2	H4	SPI_MRST	
Active rectifier							
SW1 rectifier	Output	SW1_out	1 bit	Vin1_drv	P2	RTC_ALARM	
SW2 rectifier	Output	SW2_out	1 bit	Vin2_drv L14	PMU_ISO		
SW3 rectifier	Output	SW3_out	1 bit	Vin3_drv	M15	PMU_CTRL_0	
SW4 rectifier	Output	SW4_out	1 bit	Vin4_drv	L16	MON_2	
ZCD	Input	ZCD	1 bit	ZCD	C16	INTERRUPT	
ZCD!	Input	not used	1 bit	ZCD!	C1	OSCI_26MHZ	
ZDiffVD!	Input	not used	1 bit	ZDiffVD!	E14	PMU_CTRL_3	
ZDiffVD	Input	not used	1 bit	ZDiffVD	H6	TRIG_A	
ZVD_in-	Input	ZVD_inn	1 bit	ZVD_in-	G3	SPI_MTSR	
ZVD_in+	Input	ZVD_inp	1 bit	ZVD_in+	G14	PMU_REG_RESET_N	
V_Clamp-	Output	Vclamp_sw6	1 bit	V_Clamp-	K4	SSC_ERR	
V_Clamp+	Output	Vclamp_sw5	1 bit	V_Clamp+	M3	SPI_CLK	
Turn on/off active	Input	ActRect_off	1 bit	-	L4	SW4_FPGA	Pull up pin
Vrectif. ADC block							
Sclk	Output	sclk_vadc	1 bit	Sclk	N1	RESET_BB_REQ_N	10 MHz
Sdata	Input	sdata_vadc	1 bit	Sdata	N16	MON_3	
CS!	Output	ncs_vadc	1 bit	CS!	R15	MON_4	
Parallel data ADC conversion	internal	DATA_vADC	10 bits	- -			

9.2. PCBs Layout

Characteristics of the boards:

- Material used: FR4 1.55mm 35µm Cu
- Surface: HAL leadfree
- Solder resist: Top and bottom green.
- Size: Transmitter (127 mm x 117 mm), Receiver(98 mm x 79 mm)

Track width and via sizes are based on the following specifications [31] and [32].

Since this is not a final product and its purpose it's more as an experimental prototype for testing and measuring, components has been carefully chosen to be more manageable and easily solder and unsolder keeping the performance. Apart from this, having a reasonable size of components allows to have a better accessibility to each point and better rework. Therefore SOIC Package and 0805 components has been priority selected every time that was possible.

9.2.1. Transmitter PCB layout

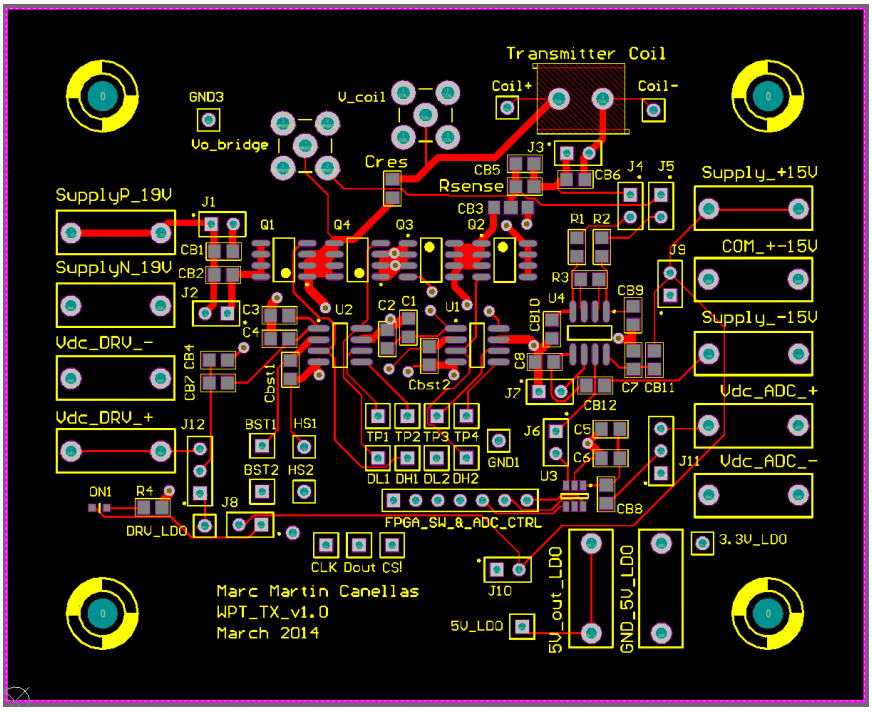


Fig. 126: Transmitter PCB Board Layout (top layer)

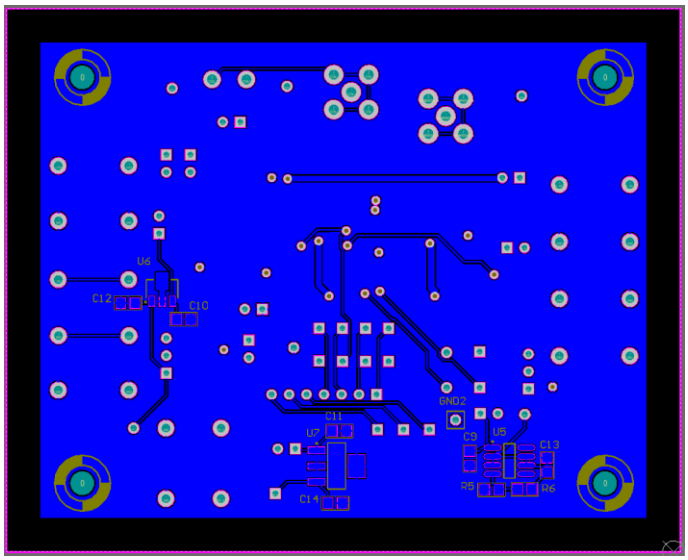


Fig. 127: Transmitter PCB Board Layout (bottom layer)

9.2.2. Receiver PCB layout

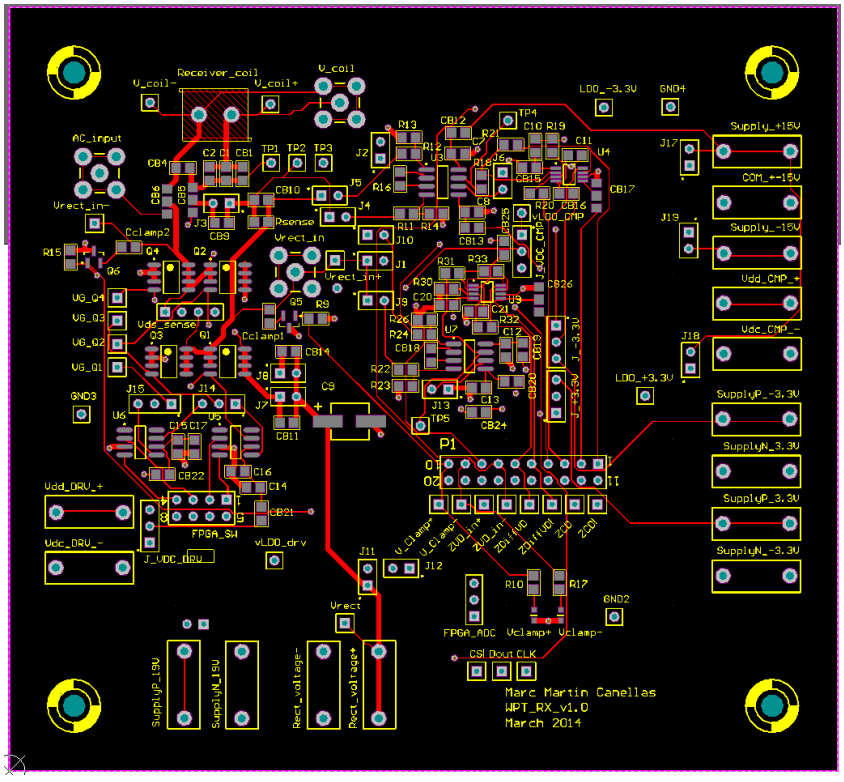


Fig. 128: Receiver top layer layout

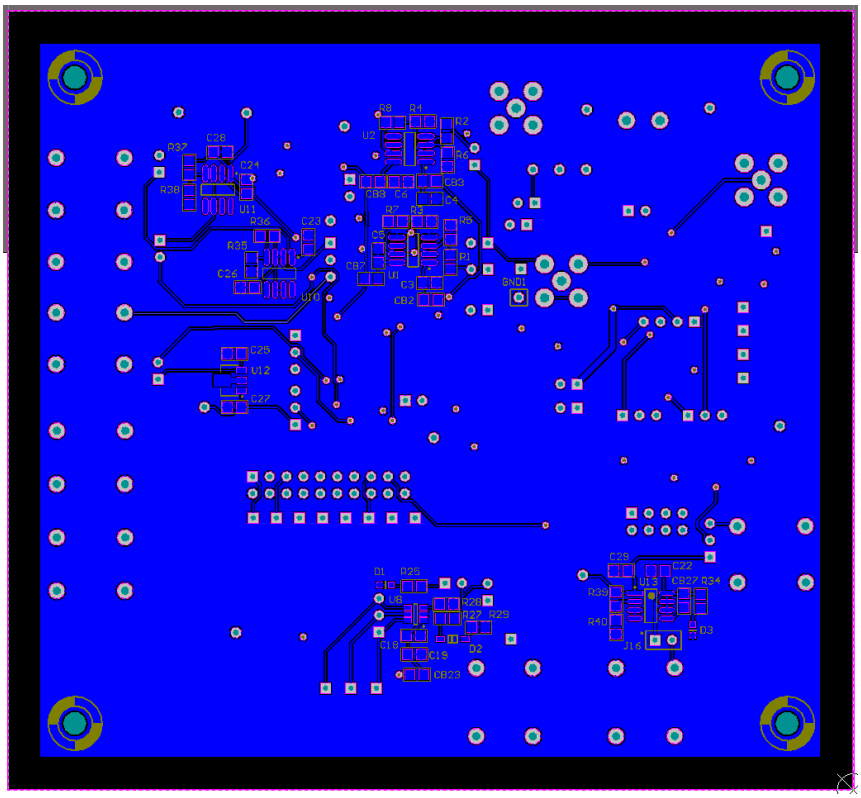


Fig. 129: Receiver PCB Board Layout (bottom layer)