Master in Photonics

MASTER THESIS WORK

ETCHING TECHNIQUES FOR THINNING SILICON WAFERS FOR ULTRA THIN HIGH EFFICIENCY IBC SOLAR CELLS

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Etching techniques for thinning silicon wafer for ultra thin High Efficiency Interdigitated back contact solar cells

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Abstract. High efficiency Interdigitated back contact (IBC) solar cells help reduce the area of solar panels needed to supply sufficient amount of energy for household consumption. We believe that a properly passivated IBC cell with the aid of light trapping schemes can maintain an efficiency of 20% even with thickness under 20μm. In this work, photolithography and etching techniques are used for deep etching of crystalline Silicon (c-Si) wafer to a thickness less than 20 μm. Tetramethylammoniumhydroxide (TMAH) wet anisotropic etching and plasma based Reactive ion etching (RIE) are used with SPR 220-7.0 and SU-8 photoresists. SiO₂ is used as making layer for TMAH etching. TMAH etch of a 4-inch c-Si wafer is done at a temperature of 80°C for 8 hours. RIE of a quarter of a 4-inch c-Si wafer is done for 3 hours using SF₆ as reactive gas. A baseline photolithography process flow for SU-8 photoresist deposition was developed. The etch rates of TMAH etch techniques fall within the range of 0.3 – 0.45 μm/min and etch rates for Reactive ion etching fall within the range of 1.2 – 1.8 μm/min. The Reactive ion etching shows capability of achieving smaller thickness sizes with greater advantages than the TMAH etching technique.

Keywords: IBC solar cells, Masked Etching, Photolithography, Reactive-ion etch, and TMAH Etching.

1. INTRODUCTION

Energy is believed to be the number one problem humanity faces in the next fifty years [1]. By estimation, solar energy shows potential of supplying in an hour, the amount of energy to meet the total energy demand of the world in a year [2]. A major challenge that the Photovoltaic industry faces is the generation of sufficient amount of energy at a cost competitive to that of fossil fuels. This factor depends on the need for high efficiency PV devices and a reduced manufacturing cost [3]. Higher efficiency solar cells have been reported to give efficiencies greater than 20% on a scale higher than the commercially available solar cells using crystalline silicon material. One of these types of PV cells is the Interdigitated Back Contact Solar cell [4].

IBC solar cells are cells with both p+ contacts and n+ emitters on the rear side of the cell which prevents shading losses. The metallization follows an interdigitated patterning. The IBC cell at UPC is processed by surface passivation of Aluminium oxide/amorphous Silicon Carbide (Al₂O₃/a-SiCₓ) for p+ contact, phosphorus-doped silicon carbide stack/Hydrogenated amorphous Silicon Carbide (SiCₓ/a-Si:H) for the n+ contact and a-SiCₓ as the back reflector. The contacts are created by laser processing and finally Aluminium metallization to complete the fabrication process [5]. The advantages of this type of cell are: (a) there are no metal shadow losses in the front side (b) resistive losses due to the fingers and busbar can be very low, and (c) there is easier cell interconnection [5, 6]. IBCs are introduced to increase conversion efficiency of crystalline silicon solar cells greater than 20%. With this high efficiency, the size of panels 6.5m² of traditional cells can be reduced to 4.8m² or less to meet the total family average annual energy demand. The major goal is to develop procedures that facilitate large scale production [6].

IBC solar cells allow further reduction of cell thickness. Light trapping schemes in crystalline silicon cells such as anti-reflection coatings, random texturing and others have helped in increasing absorption
of carriers, the total internal reflections and also the percentage of light absorbed, thereby maintaining high efficiency with need for much less materials [7]. So a very thin layer of silicon performs better than very thick films of very quality material. We believe that a well passivated IBC solar cell through these schemes can achieve efficiency up to 20% even with thickness under 20μm. In order to achieve this and experimentally demonstrate this idea, we try to develop reliable procedures to deeply etch silicon wafers to a thickness less than 20μm. Technology trends have been widely used to etch silicon wafers. Anisotropic wet etching has been an extensive used technique for microstructure fabrication on silicon wafers because of its compatibility and is cheaper to implement. Tetramethylammoniumhydroxide (TMAH) is used as the anisotropic etchant in this work. Recent developments introduce dry etching, more especially the plasma-based technique known as Reactive Ion Etching. RIE involves a combination of physical mechanism (ion bombardment) and chemical mechanism (chemical reaction of etchant gases) to produce a more anisotropic etch profile [8].

This paper presents the use of the RIE technique to thin Silicon wafers to a final thickness less than 20 microns. This was achieved by using SU-8 photoresist, a high contrast negative epoxy based photoresist as masking layer. A study was carried out on the behavior of this type of Photoresist at film deposition thickness of 40 microns and 120 microns. A baseline photolithography process was developed using SU-8 photoresist. The outcome of using SU-8 and RIE method was compared to the popular anisotropic wet chemical etching in terms of the etch profile and most especially the etch rates. The understanding of this concept is useful for future applications in the fabrication of ultra thin IBC solar cells.

2. EXPERIMENT
Crystalline Silicon wafer (4 inches) with 100nm thin layer of SiO$_2$ on both sides was pre-treated with acetone and isopropyl solutions, and then rinsed and dried with water and N$_2$ respectively. Thin film deposition on the wafer was done using a Megaposit 220-7.0 SPR positive photoresist. This positive photoresist is removed from areas where there is no masking and UV irradiation reaches, making it softer to be removed. The opposite is the case for the negative photoresist. These behaviours are portrayed in Figure 1.

![Figure 1](image_url)

Figure 1. Response of (a) SPR positive and (b) SU-8 negative photoresists to UV irradiation

The wafer with SPR is baked in an oven for 15mins at a temperature of 105°C and cooled for a few minutes before exposing to UV irradiation to create windows on the surface of the substrate. A hold time of 45 minutes before developing using Megaposit Developer MF24A% to remove the SPR from the windows created for etching. A thin layer of SiO$_2$ on the silicon surface is etched in Ammonium Flouride etching mixture solution with SPR as masking for the SiO$_2$. SPR is removed from the surface and RCA standard clean steps are performed on this sample to remove organic residues from the surface. This is done in a solution of 5 parts of deionized water (H$_2$O), 1 part of aqueous NH$_4$OH (29% by weight of NH$_3$) and 1 part of aqueous H$_2$O$_2$ (Hydrogen peroxide, 30%) at a temperature of 70°C for a period of 10mins. The wafer is washed and dried with H$_2$O and N$_2$. The substrate is inserted in a
commercial concentration of TMAH at an etching temperature of 80°C for 8 hours in order to etch the windows on one side (front side) of the wafer. The 8 hours time duration is divided into smaller times to check the etch rates. The process flow of the SPR deposition and TMAH etching is shown in figure 2. This process was repeated on a wafer with SPR 7.0 on both sides to mask the SiO$_2$ on the rear side during SiO$_2$ etch.

![Figure 2. SPR Photolithography and TMAH Process Flow](image)

Another wafer is divided into four parts and each quarter is used to perform an SU-8 deposition to show a repeated process. The SU-8 photoresist is chemically and thermally stable with excellent imaging characteristics. 40 microns film thickness is deposited on the substrate and baked for 7 minutes on a hot plate. UV irradiation is exposed to the sample to form an image. The photoresist remains on the area where there is no masking as shown in figure 1(b). A post exposure bake is done before developing with an SU-8 developer for 7 minutes, and then cleaned with isopropyl solution for 10 seconds. The substrate is rinsed and dried with water and N$_2$. This process is done for a thickness of 120 microns on a full wafer with different parameters. The parameters used to perform SU-8 deposition and photolithography for 40 and 120 microns are summarized in table 1. The process flow for SU-8 deposition is shown in figure 3.

**Table 1. Photolithography parameters for 40 and 120 microns SU-8 deposition**

<table>
<thead>
<tr>
<th>Parameters</th>
<th>40μm</th>
<th>120μm</th>
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<tbody>
<tr>
<td><strong>Spin Coating</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Spin Speed 1$^{st}$ Cycle</td>
<td>500rpm</td>
<td>500rpm</td>
</tr>
<tr>
<td>2$^{nd}$ Cycle</td>
<td>4000rpm</td>
<td>1500rpm</td>
</tr>
<tr>
<td>Acceleration 1$^{st}$ Cycle</td>
<td>100 rpm/sec</td>
<td>100 rpm/sec</td>
</tr>
<tr>
<td>2$^{nd}$ Cycle</td>
<td>300 rpm/sec</td>
<td>300 rpm/sec</td>
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<tr>
<td><strong>Soft Bake</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bake Temperature</td>
<td>95°C</td>
<td>95°C</td>
</tr>
<tr>
<td>Bake Time (Duration)</td>
<td>7mins</td>
<td>22mins</td>
</tr>
<tr>
<td><strong>Alignment and UV Exposure</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Exposure Power</td>
<td>270 mJ/cm$^2$</td>
<td>270 mJ/cm$^2$</td>
</tr>
<tr>
<td>Number of Cycles</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>Exposure Time per cycle (Total)</td>
<td>20s (40s)</td>
<td>20s (40s)</td>
</tr>
<tr>
<td><strong>Post Exposure Bake</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bake Temperature</td>
<td>95°C</td>
<td>95°C</td>
</tr>
<tr>
<td>Bake Time (Duration)</td>
<td>7mins</td>
<td>11mins</td>
</tr>
<tr>
<td><strong>Development</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Development Time</td>
<td>7mins</td>
<td>11mins</td>
</tr>
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</table>

![Figure 3. Photolithography and RIE process Flow for SU-8 deposition](image)
RIE was used to etch (100) oriented crystalline silicon wafer in order to determine the etch rates and characterize this etching process. RIE system consists of a cylindrical vacuum chamber with a combination of a parallel plate reactor powered by a 13.56MHz radio frequency (RF) generator. The wafer is placed on a cooled surface (20°C) power electrode of the parallel plate reactor and negative DC bias generated in the electrode where the substrate was placed, exposing the wafer to the bombardment of positive ions. Sulfur Hexafluoride (SF₆) is the reactive gas used and are fed into the chamber. SF₆, which is used for silicon etching experiences dissociation as a result of gas discharge, thereby generating fluorine ions used for etching. In this work, the RIE was divided into two steps: (1) Conditioning chamber step (SF₆ test on dummy substrate) (2) Process Chamber (SF₆ on substrate). The etch conditions depend on the process parameters including the pressure, gas flows, RF power and summarized in table 2.

<table>
<thead>
<tr>
<th>Table 2. RIE parameters for c-Si etching</th>
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</thead>
<tbody>
<tr>
<td><strong>Parameter</strong></td>
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<tr>
<td>Gases</td>
</tr>
<tr>
<td>Pressure</td>
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<td>Power</td>
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<td>ICP</td>
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<tr>
<td>Temperature</td>
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Etch was done for 3 hours duration in steps of 1 hour to calculate the etch rates per hour. The remaining photoresist was removed with 1-methyl-2-pyrrolidone at a temperature of 120°C on the hot plate and SU-8 deposition is done on the wafer after each hour of RIE because SU-8 becomes hard and parts of it remove from the surface of the wafer after RIE. The etch depth for each hour is measured by profilometry.

Compatibility tests were carried out on two sets of wafers with (a) the SU-8 on the front surface and the SPR on the rear side. (b) SU-8 and SPR on the same side (Front surface). The first case was to check if both photoresists are compatible for realization of the IBC fabrication. The oven at a temperature of 105°C for SPR on the rear side and 95°C for the SU-8 on the front side. The first case shows compatibility for IBC process. The second case was done to make the SU-8 remain on the surface of the wafer after the reactive-ion etch. This case is not compatible because of the different responses of these two types of photoresists to UV irradiation and different photomasks.

3. RESULTS AND DISCUSSION
3.1 SPR Photoresist and TMAH Etching
A perfect anisotropic profile after performing the lithography with the SPR 220-7.0 photoresist is shown in figure 4.

![Surface profile of SPR 7.0 deposition](image)

Figure 4. Surface profile of SPR 7.0 deposition

The case of the photoresist on one side of the sample, after 2 hours of TMAH etch, an etch depth of 46.6μm was obtained as shown in Figure 5 (a). After an extra 2 hour etch, the etch depth obtained was
an extra 48.1μm making a total of 95μm etch after 4 hours as shown in figure 5 (b). After another 4 hours of TMAH etching, a total of 8 hours of etch. The final etch depth was 193.2 microns as shown in figure 5 (c). The TMAH etch profile of silicon wafer has a tapered anisotropic etch profile forming a V-shape by the (111) oriented sidewalls as shown in figure 6.

![Figure 5. Surface profile of etched wafer for (a) 2 hours (b) 4 hours (c) 8 hours TMAH etching](image)

![Figure 6. Tapered Anisotropic Etch profile of TMAH etch showing crystallographic orientations and undercutting effects.](image)

The etch rates are calculated as Etch Depth/Etch time (in μm/min). The etch rates for 2 hours, extra 2 hours and finally 4 hours were 0.39, 0.40 and 0.41μm/min respectively. These values are plotted in figure 7.

![Figure 7. Etch rates of TMAH etching](image)

Same experiment with SPR 7.0 on both sides of the wafer is done to evaluate repeatability and reliability of the process. After 4 hours 45 minutes of TMAH etch, the etch depth was 100.8μm as shown in figure 8 (a). After an extra 3 hour 15minutes of etch making a total of 8 hours, the etch depth was 175.3μm as seen in figure 8 (b).
The same etch profile was observed as the first case. The etch rates for 4 hours 45 mins and 3 hours 15 minutes were 0.35μm/min and 0.37μm/min. These etch rates fall within the range of wet anisotropic etching, which is between 0.1 to 1 μm/min [9]. The etch rates of (100) Silicon wafer can be improved by decreasing the concentration and increasing etching temperature [10, 11].

Some problems were identified using TMAH etching techniques. After more than 4 hours of etch and exceeding a wafer thickness of 200 microns, pinholes were observed in the etched region using an optical microscope. Optical microscope images showing pinhole detection and calculation of its size are shown in figure 9.

The pinhole at a closer zoom appears like a vertex point as seen in fig 9 (b) and contributes severely in reducing the cell yield strength and eventually leads to breakage [9, 11, 12]. This is a huge defect when fabricating high efficiency IBC solar cells. Larger pinholes and even breakage along the (110) crystallographic plane of the c-Si wafer were observed in the second experiment of TMAH etching, as shown in figure 9 (c). It is necessary to check these defects before the wafer is introduced into further cell processing to avoid panel efficiency reduction.

Another problem noticed with the TMAH wet etching technique was the case of undercutting, whereby some etches undercut the masking layer and form cavities beneath, forming sloping sidewalls [13] as shown in figure 6. 1μm of undercutting was observed for every 10μm of TMAH etch. Although this defect is more common with the isotropic etch (CP4 Etch, also called HNA – HF: Nitric: Acetic Etch).

### 3.2 SU-8 Photoresist and Reactive ion etching

The surface profile after performing the deposition and lithography with the SU-8 photoresist for 40 microns thickness and 120 microns thickness is shown in figure 10 (a) and (b) respectively.
For the case of 120μm, after one hour of RIE and removal of SU-8 from the surface of the wafer, the etch depth was 39microns. This yields an etch rate of 0.65μm/min (i.e. 39microns/60mins), which is even less than 1 μm/min. This is shown in figure 11.

This indicates a limited etch as a result of using a full wafer and also the crinkled surface caused by a hard contact on the 120 microns deposition during alignment for UV exposure. The chamber clamp experiences problem holding the wafer. As a result of this, during the RIE, flux of Helium gas was released inside the process chamber in excess, thereby mixing with the etchant gases leading to a reduction in the etch rate. A smaller SU-8 deposition of 40 microns on a quarter wafer was used to perform the same experiment to avoid the previous problems. After one hour of RIE of 40 microns deposited wafer, the etch depth was 105.6 microns after taking an average of two sides as shown in figure 12.

After another one hour, the etch depth was 184.9 microns after taking an average of measurements on two sides of the etched window cavity as shown in figure 13. After the third hour of etch, the wafer was completely etched and a depth of 10 microns into a supporting substrate used for placing the initial substrate in the RIE chamber. The surface profile was measured on two sides to determine the
entire thickness of the wafer, the etch profile is shown in figure 14 (a), and then measuring the etch depth of the supporting wafer as shown in figure 14 (b).

Figure 13. Surface profiles of two sides of etched 40μm deposited wafer after 2 hours of RIE

Figure 14. (a) Surface profiles of total wafer thickness (b) Surface profile of extra 10μm etch into supporting substrate.

The value of the etch depth of the second wafer was added to the entire thickness of the initial wafer and subtracting the previous etch after two hours, to determine the etch rates of the third hour. This value is depicted in equation 1.

$$X = (A + \delta) - B$$

Where A is the total thickness of the initial wafer, B is the etch depth after 2 hours and \(\delta\) is the extra etch into the second wafer and X is the etch depth for the third hour. The value of the third etch after calculation using equation 1 was 85.7 microns \([(260.6 + 10) - 184.9]\). This means a total etch of 270.6 microns after three hours of Reactive ion etching. The etch rates were calculated as 1.76μm/min, 1.32 μm/min and 1.43 μm/min for the first hour, second hour and third hour respectively. These values were plotted as etch depth as a function of the etch time shown in figure 15.
The etch rates fall within the range of 1.3 to 1.8 μm/min, with an average etch time of 1.5 μm/min. This means approximately 90 microns of etch for each hour, that is 3 to 5 times the etch rates of TMAH wet etching. The reason for faster etch rates is because of the synergy between the physical and chemical mechanisms occurring during Reactive ion etching [8]. This effect is shown in figure 16. The high energy collisions from ionization helps to dissociate etchant gases into more reactive nature resulting in a faster etch process [14]. Reactive ion etching has other advantages like higher aspect ratio, this means more visible etch profiles with a rougher surface [15]. There is little or no undercutting when using this technique and after a deep etch, pinholes are not observed.

Some challenges with RIE were also noticed, this relates more to the photoresist. As seen in the case of 120 μm deposition of SU-8, limited etch rates were observed on a full wafer because of problems with the chamber clamp. In most cases, the photoresist was partially or completely removed from the surface of the substrate. Another case was observation of cracks on the SU-8 photoresist, making it more difficult to remove with 1-methyl-2-pyrrolidone. This increased the removal time from 1 – 2 hours to 3 – 5 hours. The etched surface is rougher than the TMAH etched surface.

4. CONCLUSION

The article develops reliable procedures to deeply etch silicon wafers to a thickness less than 20μm for fabricated IBC solar cells. A baseline photolithography process using SU-8 photoresist was developed. A study on the behavior of this type of photoresist and an influence of masked photolithography and etching was carried out. SU-8 photoresist is proven to be made harder by UV irradiation. It has higher aspect ratio imaging characteristics. Different thickness studies were carried out on this type of photoresist, 40μm and 120μm depositions.
Etching techniques, TMAH wet anisotropic etching and Reactive ion etching for silicon wafer reduction to ultra thin size have been investigated. The etch rates of RIE technique proved to be 3 to 5 times faster than the etch rates of TMAH with less disadvantages such as pinholes and cracks along the crystallographic planes. This indicates less breakage and better potential cell yield. The reactive ion etching proves capable of achieving smaller feature sized microstructures and good for future applications like the ultra thin interdigitated back contact solar cells.

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References