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Engineer (Electronic)

June 2014

Final Year Project

Engineer (Electronic)

Design of CMOS Active Inductors and their use in tuned narrowband and wideband-extension Low Noise Amplifier
Final Year Project

MEMÒRY

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Convocatòria: June 2014

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ABSTRACT

The evolution of CMOS technology has allowed the integration of communication systems on a single chip. A Low-Noise Amplifier (LNA) is the first block in an integrated receiver and its design is critical for the system performance. On-chip spiral inductors are key components in LNA's running at GHz frequency range. They are the performance limiting components of LNA's, and have the added problems of rigidity and also do not scale well with CMOS (i.e. consume a large amount of area, which increases the chip cost). Their quality factor (Q) is limited by the resistive losses in the spiral coil and by substrate losses. This project deals with replacing the area-consuming, lossy spiral inductors by gyrator-based CMOS active inductors. The project starts with the simulation of some reference spiral inductors to find their main characteristics (inductance value, quality factor at different frequencies and self-resonant frequency). Next, several CMOS active inductors are designed with the target to achieve similar or improved performance compared to the reference ones. Several topologies are tested, and the designed is optimized after predictions of simple models. Finally, both active and passive inductors are then used in two test amplifiers: a tuned narrowband amplifiers and a wideband – extension amplifier. Their performance is compared in terms of input and output matching, gain, isolation, noise figure and linearity. Frequency tuning capability is tested in the active inductors, which would provide an interesting flexibility in future communication receivers.

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1)Introduction

1.1)CMOS Integration

The evolution of CMOS microelectronic technology over the years has allowed integration of communication systems on a single chip. Scaling of transistors over the years, a case of Moore's law has resulted in a decrease in channel length. The following figure illustrates the decrease of transistor´s channel length over the years:

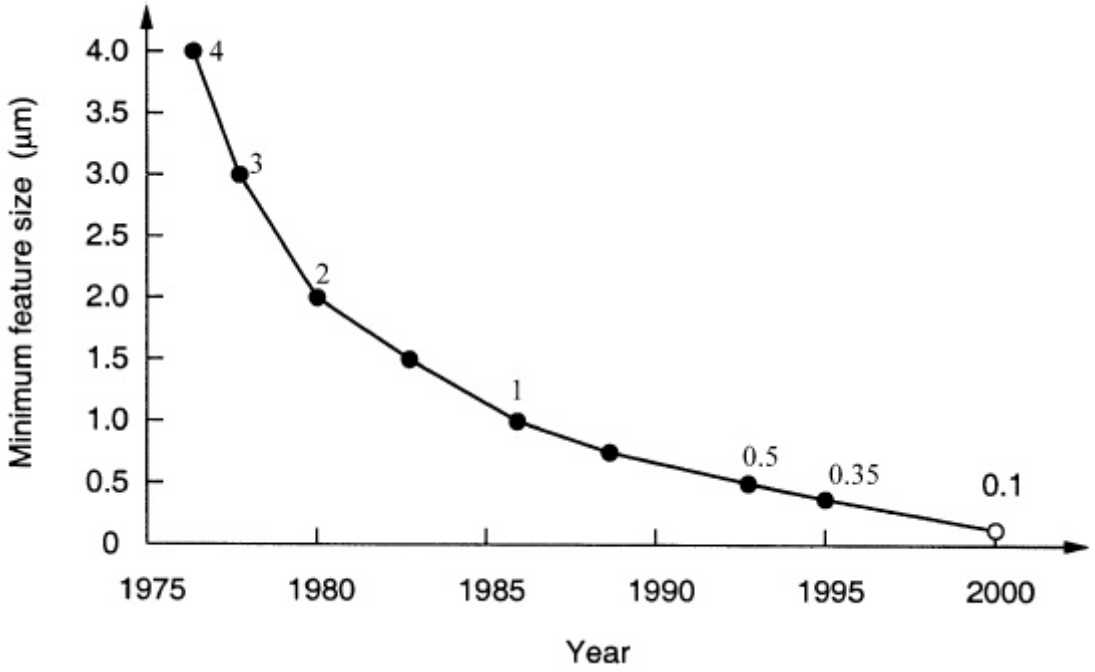


Fig. 1.1: CMOS integration

Channel length is taken as the reference geometrical parameter in a CMOS technology node. All geometrical dimensions in a circuit are considered to be scaled according to the channel length. Therefore, the decrease in channel length has led to integration of more and more transistors on a single chip and has also led to the decrease in the area of chip, which also has reduced the cost. In digital devices, the minimum channel length has gone upto 20nm, but in analog devices, the minimum channel length has gone upto 45nm. In general, this decrease is component size has allowed the integration of more circuitry -and more functionality- in a single chip. Today, complex communication systems, including radiofrequency transmitters and receivers, digital processing, processors and mamories, can be produced in a single silicon die.

1.2)RF Receiver Architecture

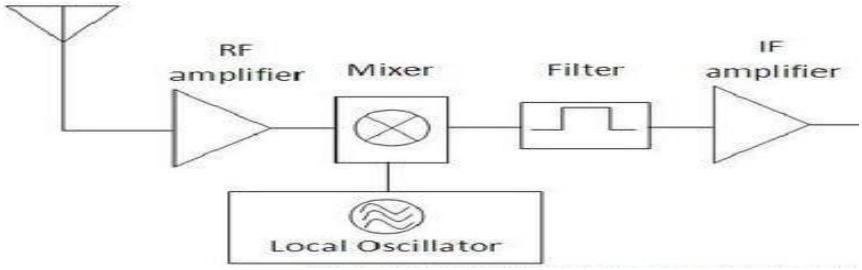


Fig. 1.2: RF Receiver Architecture

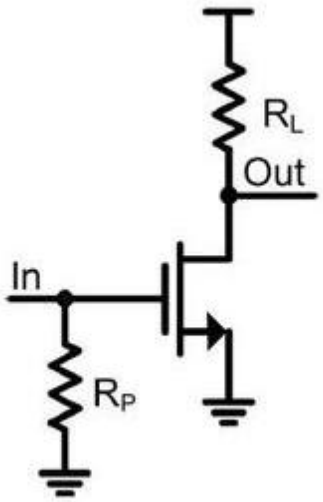
A typical communication system includes of a transmitter front-end and a receiver front-end. A signal is sent from the transmitter, travels from centimeters to thousands of miles -depending on the communication standard and has noise corrupting the signal.The purpose of a radio receiver is to take this observed RF signal and convert it into baseband symbols understandable by the demodulator. Low noise amplifier (LNA) is typically the first stage of a receiver. Its performance greatly affects the overall receiver performance. It plays a critical role in determining the overall system noise figure of the receiver. Overall noise figure of a cascaded system can be given by:

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + ...$$

As seen from the above equation, gain of the first stage is very critical, and making it very large can render the noise figure of subsequent stages useless, thus not affect the overall noise figure. The main function of an LNA is to provide this sufficient gain to reduce the noise of subsequent stages.

1.3)Low Noise Amplifier(LNA)

A low noise amplifier has several common goals – providing a low noise figure, sufficient gain and a good matching at the input – here it is a 50Ω matching. A good input match is even more critical when a preselect filter precedes the LNA because such filters are often sensitive to the quality of their terminating impedances.
We first focus on the requirement of providing a stable input impedance of 50Ω. The architectures satisfying this condition can be given as follows:



R_p=50Ω

Fig. 1.3: Parallel resistance termination

(a) **Parallel resistive termination**: We can use a resistive termination of 50Ω to match the LNA to the input resistance of 50Ω. This provides a perfect input matching, but gives a higher noise figure due to the presence of resistor. Hence this topology is commonly avoided as an LNA in an RF receiver.

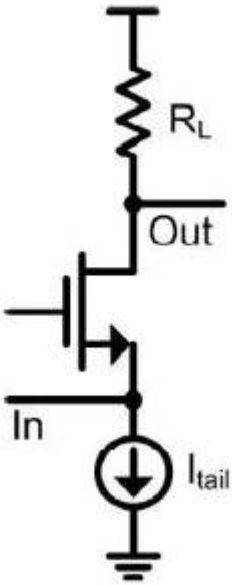


Fig. 1.4: Common gate LNA

(b) **Common – gate LNA:** Using LNA in common gate fashion, as this eliminates the use of resistor. By using this method, the input signal sees the transistor channel from source to drain, which provides the real part of the input impedance. The input impedance of the common-gate topology is thus the inverse of the transistor transconductance i.e. $1/g_m$. Hence we have to make g_m=20mS. Although the common-gate topology generally provides better noise figure than the parallel resistance topology, the noise performance of the amplifier cannot be optimized as the transconductance of the input transistor is fixed with a value inverse to the source resistance in order to provide input impedance matching.

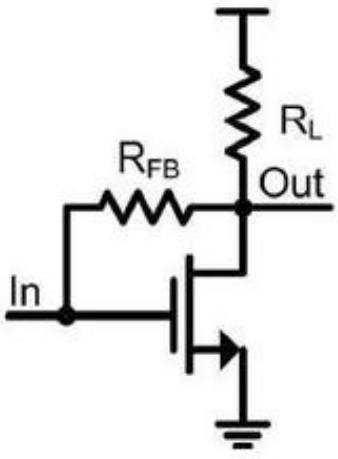


Fig. 1.5: Resistive Feedback

(c) **Resistive feedback:** It is based on using a feedback resistor located between the drain and the gate of the amplifying device. By placing this resistor, the input impedance presents a real part that can be used for impedance matching. As compared to performing input impedance matching by using a parallel resistance, the signal is not attenuated at the input and therefore provides a better noise figure. Nevertheless, the feedback resistor adds thermal noise which, depending on the required value of the resistor to provide input impedance matching, may become a dominant factor in the total noise generated by the amplifier. When using resistive feedback, reverse isolation is degraded even when using a cascode topology, therefore it is important to ensure that the circuit is stable within the desired frequency range.

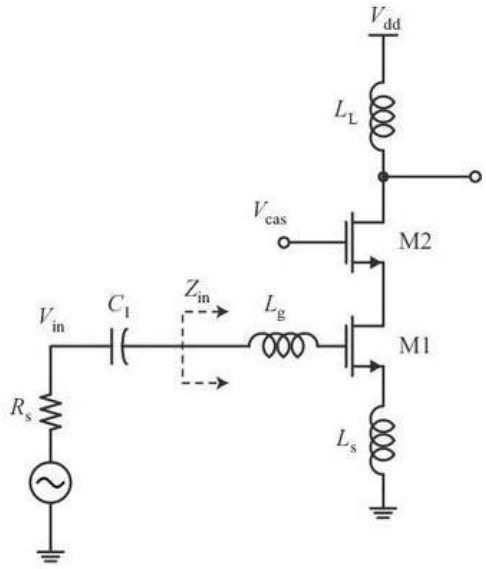


Fig. 1.6: Inductive Degenerated tuned LNA

(d) **Inductive Degeneration:** In this architecture, input matching is provided by inductive termination. There are no resistive elements in the signal path. Hence this provides the best noise performance than the previous architectures. Also the cascode structure provides isolation of the output port from the input port.

$$Z_{in} = \frac{1}{j\omega C_{gs}} + L_s\omega_T + j\omega_s\left(L_g + L_s\right)$$

where

$$\omega_T = \frac{g_m}{C_{gs}}$$

Hence making Z_{in}=50Ω we get the required input matching without using a resistor. Also the amplifier resonates at a frequency of

$$\omega_0 = \frac{1}{\sqrt{C_{gs}\left(L_g + L_s\right)}}$$

We can fix the resonant frequency and have a freedom of choosing L_g and L_s, to get the correct termination and resonant frequency. Besides the inductors at the gate (Lg) and source (Ls), the load inductor (Ll) is designed to resonate with the load capacitance at the desired carrier frequency, thus providing maximum gain.

Note this topology provides optimum NF characteristics, but is inherently narrowband. Whenever a wideband amplification is desired, some of the other topologies is used (preferably common-gate or resistive-feedback), and commonly some inductive bandwidth-extension circuit is added at the output net in order to extend the RF response.

1.4) Inductors in CMOS technology

CMOS technology is essentially a planar process, i.e. different layers are laid on the surface of the silicon chip, thus producing the IC structure. Fig. 1.7 shows an ideal cross-section of a CMOS IC.

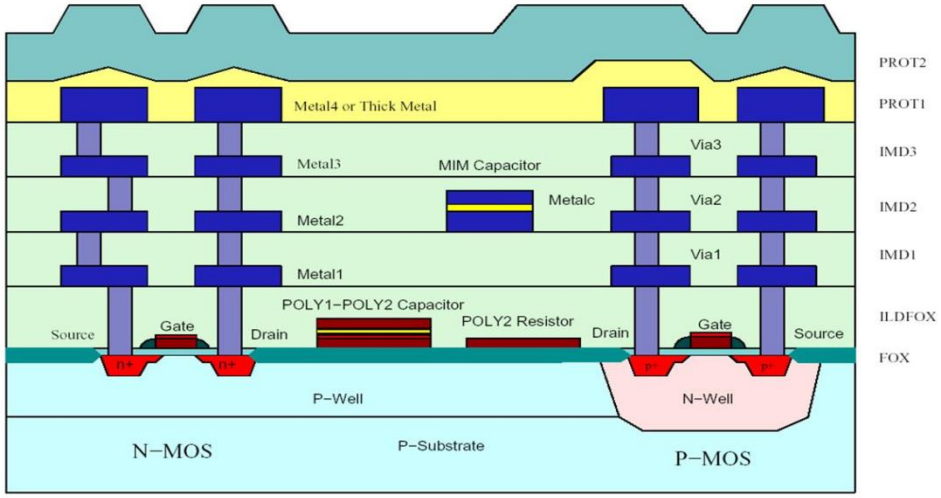


Fig. 1.7: CMOS IC cross-section

Implementing passive components, and particularly inductors, in such manufacturing process is quite inconvenient, and their performance is typically limited by important losses and parasitics. In the case of inductors, they are commonly implemented as spirals using the top metallization layer, if possible especially thick. Fig. 1.8 shows the typical layout of a spiral inductor.

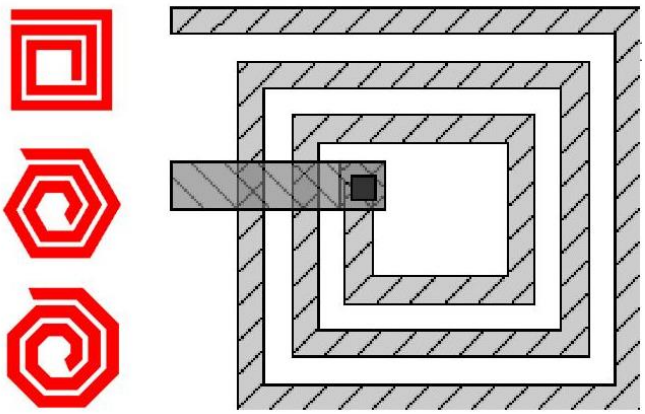


Fig 1.8: Typical Layout of a spiral inductor

Inductance is increased as the diameter and number of turns increases, and inductances in the order to 0.3 nH - 30 nH can be obtained. The price paid is silicon area (inductors are the most area-consuming component in the circuit), cost (because of the area consumed), and losses due to different mechanisms (resistive losses, eddy currents, skin effects).

1.5)Objectives.

Although spiral inductors are the common implementation approach in ICs, it is possible to design active circuits, using the gyrator concept, that show an inductor impedance from some input terminal. These active-inductor circuits would save area and add easy tunability of the inductance value. Note the trend in RF communication systems today is towards more tunability and reconfigurability, after paradigms such and the multi-standard receivers and software-defined radio (SDR). Therefore, tunability of inductances is a desirable feature, which is not possible in conventional passive inductors.

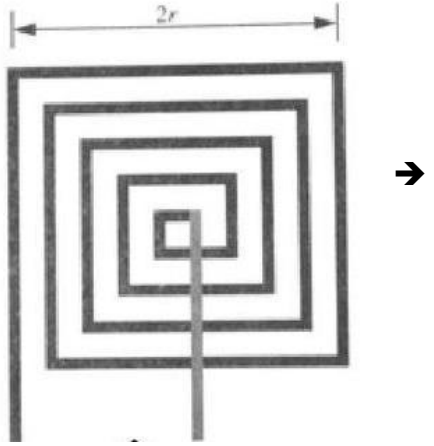
Several circuit topologies have been proposed in the past to implement active inductors based on gyrators. This worth has as a objective to compare their figures of merit in a given technology and determine the most promising in terms of losses (Q factor) and frequency response. Once this is achieved, it is proposed to demonstrate their suitability to be used in both wideband and narrowband LNAs, comparing the circuit performance when conventional spirals are replaced by active inductors, and showing the tunability allowed.

2)Implementation and figures of merit of integrated inductors

2.1)Spiral inductors

Spiral inductors are important, performance limiting components in LNA´s. The quality factor (Q) of the inductors is limited by the resistive losses in the spiral coil and by the substrate losses. There are three major loss mechanisms that degrade the quality factor of on-chip inductors: the energy loss due to the series resistance of the spiral itself, the electric coupling between the spiral and the substrate, and the magnetically induced eddy currents.

A typical layout and model for a spiral inductor can be shown as given in Fig. 2.1 and Fig. 2.2 respectively,



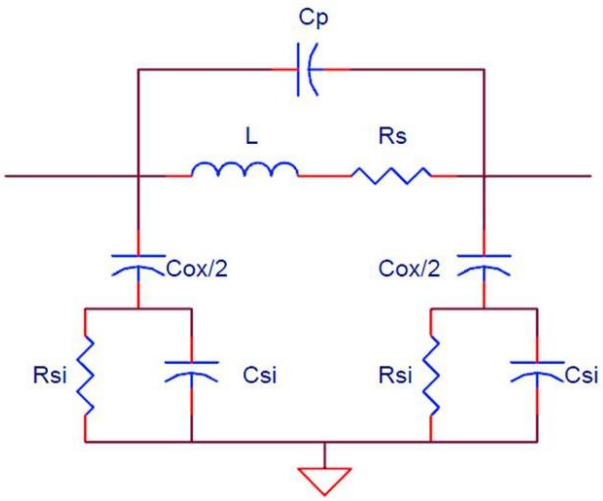


Fig 2.1: Typical layout of a spiral inductor

Fig 2.2:Typical model of spiral inductor

Paramters of layout of spiral inductor	Paramters of model of spiral inductor
L: total length of the wire	L_S: series inductance
W: width of the wire	R_S: series resistance
ω: angular frequency	C_p: parallel capacitance
t: thickness of the wire	$C_{ox1,2}$: oxide capacitances
σ: conductivity of the metal	$C_{s1,2}$: substrate capacitances
δ: skin depth	$R_{s1,2}$: substrate resistances
n: number of loops	

Ideally, we would like to have only L (i.e. only inductance), but we have more elements. Relating parameters of the layout to the model we get:

$$R_s \approx \frac{L}{W.\sigma.\delta\left(1-e^{-t/\delta}\right)}, \delta = \sqrt{\frac{2}{\omega\mu_0\sigma}}$$

$$C_p \approx n.W^2.\frac{\varepsilon_{ox}}{t_{ox}}$$

$$C_{ox} = W.L.\frac{\varepsilon_{ox}}{t_{ox}}$$

Now, assuming a ground (GND) connection, we get a parallel equivalent model as shown in Fig. 2.3, to the model of spiral inductor (given in Fig. 2.2):

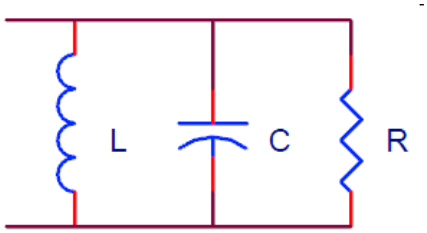


Fig. 2.3: Parallel equivalent model of spiral inductor

$$Y = \frac{1}{R_p} + j\omega C + \frac{1}{j\omega L} = \frac{1}{R_p} + j\left(\omega C - \frac{1}{\omega L}\right)$$

2.1.1)Figures of merit of the inductors

The figures of merit of characterization of inductors are the Q factor, inductance value and the self resonant frequency. They can be derived from the measurement of the admittance seen from the two port

By definition,

$$Q = -\frac{\mathrm{Im}\{Y11\}}{\mathrm{Re}\{Y11\}} = -R_p\left(\omega C - \frac{1}{\omega L}\right) \approx \frac{R_p}{\omega L}$$

$$L \approx -\frac{1}{\omega}\frac{1}{\mathrm{Im}\{Y11\}}$$

$$f_{SR} \approx \mathrm{Im}\{Y11\} = 0$$

Fig. 2.4 shows a graphical representation of the three figures of merit of the spiral inductor:

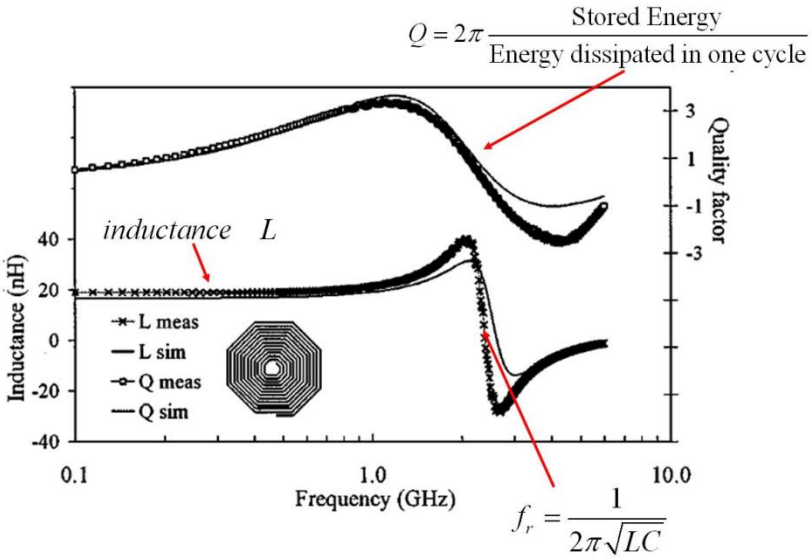


Fig. 2.4: Three figures of merit of spiral inductor

2.1.1.1)Quality factor

The inductor quality factor is directly related to many circuit figures of merit (in LNAs, VCOs, etc), and is thus a critical parameter in the design. Higher the quality factor, better the performance. Hence in this case, increasing the parallel resistance increases the quality factor.

2.1.1.2)Inductance frequency range

A spiral inductor is inductive only in a certain frequency range, i.e. till the self-resonant frequency.

2.1.2) Simulation of spiral inductors

We have selected a 0.35 µm process to implement our circuits. This relatively old process is considered representative of other more advanced technologies, and considered suitable of a vehicle for proof-of-concepts. In particular, we have used the 0,35 µm process from Austra MicroSystems, which is a technology traditionally used at the Department of Electronic Engineering. This technology includes, in its design kit, libraries of spiral inductors for design of RF circuits. The technology offers several versions: C35, which is CMOS-only, and S35, which includes bipolar transistor and high-Q spiral inductors.

We have selected some representative inductors from the library to obtain their characteristics and check they match the expected values that appear in the documentation provided by the manufacturer. We have created a test circuit to make simulations and obtain their characteristics (Q factor, inductance and self resonant frequency).

The spiral inductors used are the following:

- SP014S300D (using C35 process)
- SP090S155D (using C35 process)
- SP011S200T (using S35 process)
- SP100S250T (using S35 process)

We do an s – parameter analysis, to get the Y parameters and characterize the spiral inductor according to the formulae given before. The schematic is given by:

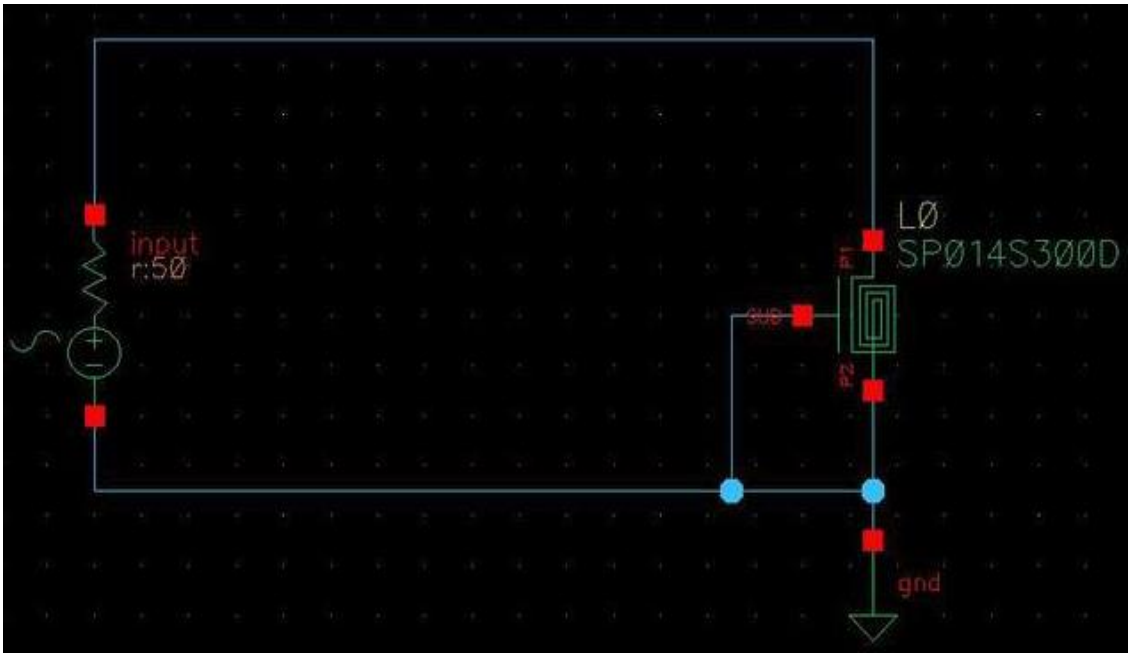


Fig. 2.5: schematic for simulation for spiral inductors

We make the following observations:

Table 2.1: Spiral Inductor simulation

SP014S300D(C35)				
f	Re{Y11}	Im{Y11}	Q	L
1GHz	0.032	-0,113	3.53	1.408nH
2.5GHz	0.00732	-0,0463	6.33	1.374nH
5GHz	0.00369	-0,0224	6.07	1.421nH
f(self resonant)	24.8 GHz			

SP090S155D(C35)				
f	Re{Y11}	Im{Y11}	Q	L
1GHz	0.007246	-0,0125	1.73	12.73nH
2.5GHz	0.00171	-0,0058	3.39	10.97nH
5GHz	0.000856	-0,00174	2.03	18.29nH
f(self resonant)	9.25 GHz			
SP011S200T(S35)				
f	Re{Y11}	Im{Y11}	Q	L
1GHz	0.0375	-0,151	4.03	1.05nH
2.5GHz	0.00658	-0,06	9.12	1.06nH
5GHz	0.00256	-0,031	12.11	1.026nH
f(self resonant)	41.5 GHz			
SP100S250T(S35)				
f	Re{Y11}	Im{Y11}	Q	L
1GHz	0.00284	-0,0147	5.18	10.83nH
2.5GHz	0.00076	-0,00505	6.65	12.61nH
5GHz	0.000706	-0,000976	1.38	32.61nH
f(self resonant)	6.21 GHz			

Conclusion:

Note in the last inductor that the L (inductance) value increases at 5 GHz since the self-resonant frequency is comparable. Nevertheless, we focus or target on the 2.4 GHz frequency, since this is the carrier frequency used in many wireless LAN communication standards. The spiral inductors were characterized and at the point of interest of 2.4 GHz the following conclusions were made:

SP014S300D (C35) – 1.37 nH (with Q of 6.33 at 2.4 GHz)

SP090S155D (C35) – 10.97 nH (with Q of 3.39 at 2.4 GHz)

SP011S200T (S35) – 1.06 nH (with Q of 9.12 at 2.4 GHz)

SP100S250T (S35) – 12.61 nH (with Q of 6.65 at 2.4 GHz)

These values match the values provided by the manufacturer in the documentation. As a conclusion, we have validated the schematic and characterization procedure, and we have obtained the characteristics of small inductors (1 nH range) and large ones (10 nH range).

2.2)Active Inductors:

The following figure (Fig. 2.6) shows a general scheme of a lossy, single ended gyrator active inductor. The circuit can be modelled by the equivalent circuits in the right:

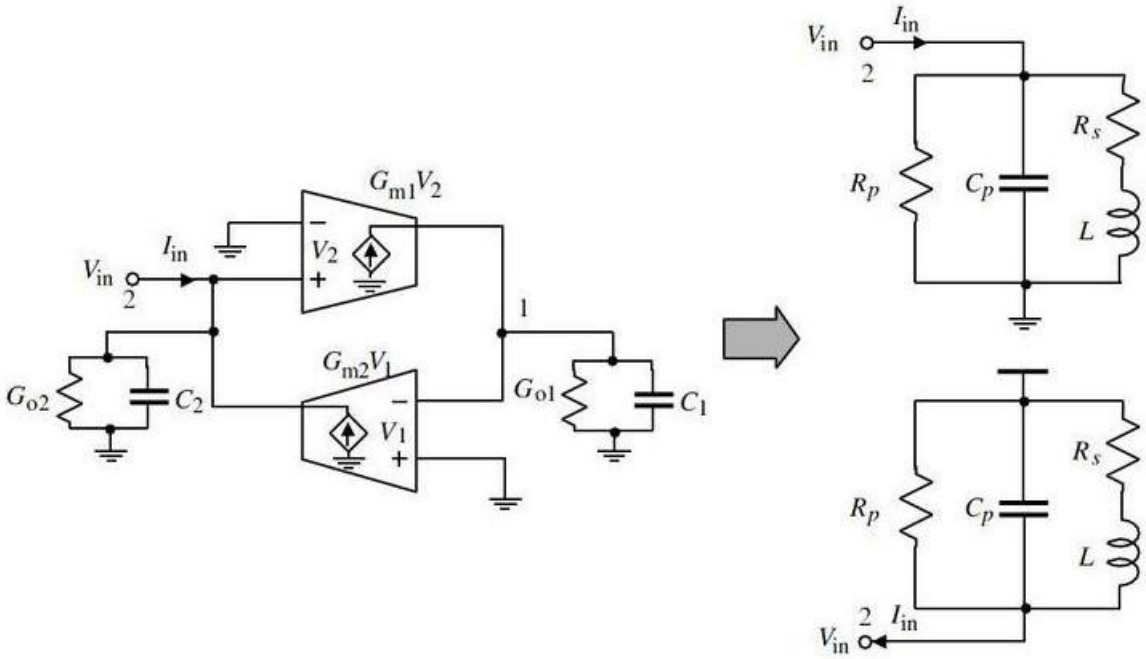


Fig 2.6: general scheme of active inductor and its equivalent circuit

A gyrator consists of two back-to-back connected transconductors. When one port of the gyrator is connected to a capacitor, as shown in Fig.2.1, the network is called the gyrator-C network. When the input or output impedances of the gyrator – C networks are finite (and not zero), the system is called lossy. Consider the gyrator-C network shown in Fig.2.4 where G_{01} and G_{02} denote the total conductances at nodes 1 and 2, respectively. Note G_{01} is due to the finite output impedance of transconductor 1 and the finite input impedance of transconductor 2.

Using KCL at nodes 1 and 2:

$$(sC_1 + G_{01})V_1 - G_{m1}V_2 = 0 - node(1)$$

$$-I_{in} + (sC_2 + G_{02})V_2 - G_{m2}(-V_1) = 0 - node(2)$$

The admittance looking into port 2 of the gyrator-C network is obtained from

$$Y = \frac{I_{in}}{V_2}$$

$$\Rightarrow Y = sC_2 + G_{02} + \frac{1}{s\left(\frac{C_1}{G_{m1}G_{m2}}\right) + \frac{G_{01}}{G_{m1}G_{m2}}}$$

Hence from the above equation can be represented by the RLC network shown in Fig. with its parameters given by:

$$R_p = \frac{1}{G_{02}}$$

$$C_p = C_2$$

$$R_s = \frac{G_{01}}{G_{m1}G_{m2}}$$

$$L = \frac{C_1}{G_{m1}G_{m2}}$$

The gyrator-C network behaves as a lossy inductor with its parasitic parallel resistance R_p, parallel capacitance C_p, and series resistance R_s. R_p should be maximized while R_s should be minimized to low the ohmic loss. The finite input and output impedances of the transconductors of the gyrator-C network, however, have no effect on the inductance of the active inductor. The resonant frequency of this active inductor is given by

$$\omega_0 = \frac{1}{\sqrt{LC_p}} = \sqrt{\frac{G_{m1}G_{m2}}{C_1C_2}}$$

2.2.1)Figures of merit of active inductors

2.2.1.1) Inductive Frequency range

A lossy gyrator – C active inductor exhibits inductive characteristics only in a certain frequency range. This frequency range can be obtained by examining the impedance of the RLC equivalent circuit of the lossy active inductor:

$$Z = \left(\frac{R_s}{\omega L}\right) \frac{s\frac{L}{R_s} + 1}{s^2 + s\left(\frac{1}{R_p C_p} + \frac{R_s}{L}\right) + \frac{R_p + R_s}{R_p C_p L}}$$

When complex conjugate poles are encountered, the pole resonant frequency of Z is given by

$$\omega_p = \sqrt{\frac{R_p + R_s}{R_p C_p L}}$$

Because $R_p >> R_s$, the above relation is simplified to

$$\omega_p \approx \frac{1}{\sqrt{LC_p}} = \omega_0$$

where ω_0 is the self – resonant frequency of the active inductor. Also observe that Z has a zero at frequency

$$\omega_z = \frac{R_s}{L}$$

It is evident that the gyrator-C network is resistive when $\omega < \omega_z$, inductive when $\omega_z < \omega < \omega_0$, and capacitive when $\omega > \omega_0$. The frequency range in which the gyrator-C network is inductive is lower-bounded by ω_z and upper-bounded by ω_0. Also observed is that R_p has no effect on the frequency range of the active inductor. R_s, however, affects the lower bound of the frequency range over which the gyrator-C network is inductive. The upper bound of the frequency range is set by the self resonant frequency of the active inductor, which is set by the cut-off frequency of the transconductors constituting the active inductor. For a given inductance L, to maximize the frequency range, both R_s and C_p should be minimized.

2.2.1.2)Inductance Tunability

Many applications, such as filters, voltage or current controlled oscillators, and phase-locked loops, require the inductance of active inductors be tunable with a large inductance tuning range. It is seen that the inductance of gyrator-C active inductors can be tuned by either changing the load capacitance or varying the transconductances of the transconductors constituting the active inductors. Capacitance tuning in standard CMOS technologies is usually done by using varactors. Adding varactors means adding a non-linear element in the circuit and this degrades the linearity of the active inductor to a large extent and hence we will avoid this technique. Hence this leaves us with the option of changing the transconductance. We can change it by changing the bias voltage of the transistors and hence get a good tuning range of inductance.

2.2.1.3) Quality factor

The quality factor Q of an inductor quantifies the ratio of the net magnetic energy stored in the inductor to its ohmic loss in one oscillation cycle. For spiral inductors, the quality factor of these inductors is independent of the voltage / current of the inductors. This property, however, does not hold for active inductors as the inductance of these inductors depends upon the transconductances of the transconductors constituting the active inductors and the load capacitance.

For a linear inductor, the complex power of the active inductor is obtained from:

$P(j\omega)=I(j\omega)V^*(j\omega)=Re[Z]|I(j\omega)|^2 + jIm[Z]|I(j\omega)|^2$, (2.1)

where Re[Z] and Im[Z] are the resistance and inductive reactance of the inductor, respectively.

The first term in (2.1) quantifies the net energy loss arising from the parasitic resistances of the inductor, whereas the second term measures the magnetic energy stored in the inductor. In this case becomes:

$$Q = \frac{\mathrm{Im}[Z]}{\mathrm{Re}[Z]}$$

This provides the most convenient way to find the quality factor of the active inductor.

The quality factor of a lossy gyrator-C active inductor can be derived as:

$$Q = \left(\frac{\omega L}{R_s}\right)\frac{R_p}{R_p + R_s\left[1+\left(\frac{\omega L}{R_s}\right)^2\right]}\left[1-\frac{R_s{}^2 C_p}{L}-\omega^2 L C_p\right]$$

$$R_p >> R_s$$

$$Q \approx \left(\frac{\omega L}{R_s}\right)\frac{R_p}{R_p + \frac{(\omega L)^2}{R_s}} \approx \left(\frac{\omega L}{R_s}\right)\frac{R_p R_s}{(\omega L)^2} \approx \frac{R_p}{\omega L}$$

$$R_s >> R_p$$

$$Q \approx \frac{\omega L}{R_s}$$

Hence we have to decrease the series resistance and increase the parallel resistance, for a given value of inductance to get a good quality factor.

3)Simulation of active inductors

3.1)Basic Active Inductor

With the spiral inductor characterized, we proceed to characterize the active inductor to get similar or improved performance compared to the passive inductors characterized in the previous chapter. As seen in Fig. 2.6, a basic topology for an active inductor can be obtained if transconductors are implemented in its simple way, i.e. with single transistors. We replace the transconductors with transistors as they are based on the model of a transconductor.

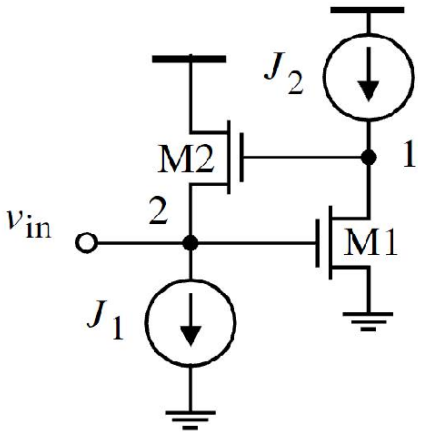


Fig 3.1: Basic Active inductor

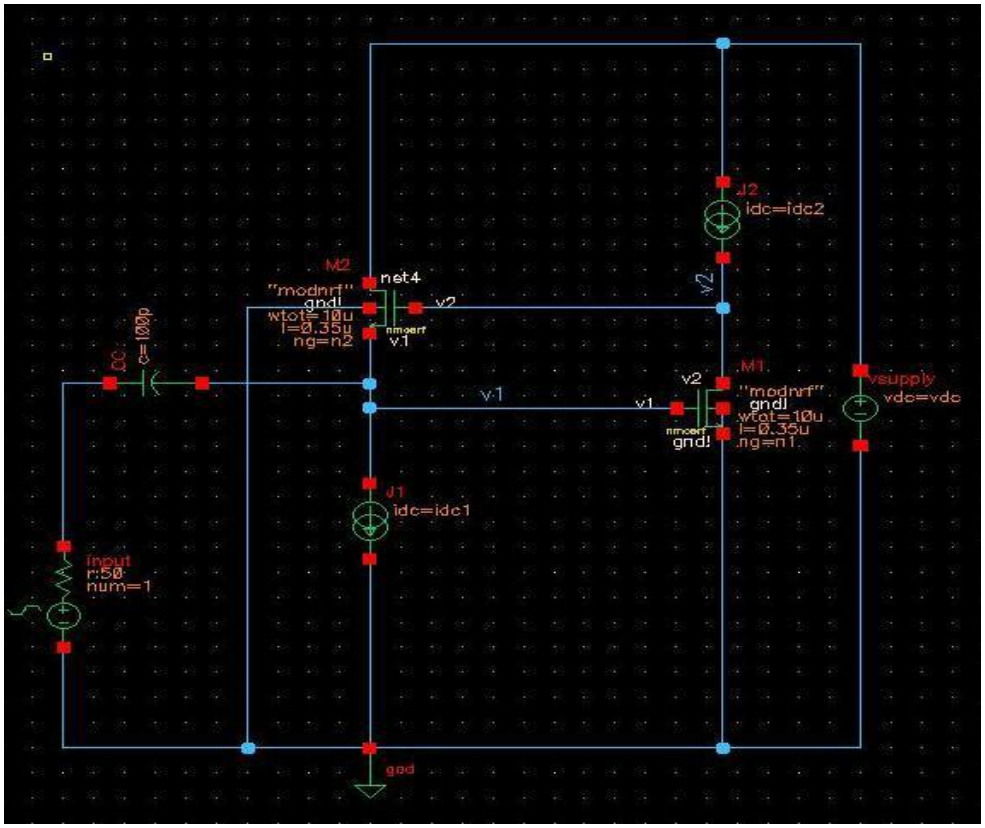


Fig. 3.2: Schematic: Basic Active Inductor

In Fig. 3.1 and Fig. 3.2, we see the implementation and schematic of the basic active inductor, respectively. Here we use transistor (M1) as the main transconductor and a transistor (M2) in feedback. Current source J1 biases the transistor (M2) and current source J2 biases the transistor (M1). We use a power supply voltage of 3.3 V, which is the nominal coltage for this 0.35 um technology. The input port is having an amplitude of 0.1mV and 50 Ω source resistance. It is a very low resistance and creates problems for dc biasing of transistor (M2). Hence, we have to use a coupling capacitor of 100pF to get a to get DC blocking, which enables the current source J1 to properly bias the transistor (M2) and get the desired results.

Modelling as a parallel equivalent model:

$$C_p = C_{gs1}$$

$$R_p = \frac{1}{g_{m2}}$$

$$L = \frac{C_{gs2}}{g_{m1} g_{m2}}$$

$$R_s = \frac{g_{01}}{g_{m1} g_{m2}}$$

$$\omega_0 = \sqrt{\frac{C_{gs1} C_{gs2}}{g_{m1} g_{m2}}}$$

Changing the above parameters, we can change the characteristics of the active inductor. We can change it either by changing the bias current or the widths of the transistors.

Keeping the widths of transistors (M1 and M2) to be at a minimum of W1=W2=10µm.Taking an arbitrary value of current J2 (here J2=500µA), we change the current J1 to change the parameters as given in the below table:

Table 3.1: Active inductor simulation - 1

J2=500uA				
J1	1uA	2uA	10uA	20uA
gm1 (in mA/V)	1.755	1.757	1.761	1.762
gm2 (in mA/V)	0,035	0,052	0,226	0,399
Cgs1(in fF)	12.702	12,69	12,67	12,66
Cgs2 (infF)	7.424	7.886	10,26	11,3
J1	100uA	200uA	500uA	1mA
gm1 (in mA/V)	1.766	1.776	1.778	17.886
gm2 (in mA/V)	1.091	1.405	1.779	2.075
Cgs1(in fF)	12,64	12.625	12,58	12,55
Cgs2 (infF)	12,23	12,28	12,31	12,36

J1				
100uA				
f	Re{Y11}	Im{Y11}	Q	L(in nH)
1GHz	0,00427	-0,0108	2,529	14.74
2.4GHz	0,00186	-0,00438	2,355	15.14
5GHz	0,00149	-0,00153	1,026	20.8
f(self resonant)	8.68 GHz			
J1				
200uA				
f	Re{Y11}	Im{Y11}	Q	L(in nH)
1GHz	0,005226	-0,0139	2,659	11,45
2.4GHz	0,002159	-0,00575	2,663	11,53
5GHz	0,001675	-0,002192	1,308	14,52
f(self resonant)	9.92 GHz			

J1				
500uA				
f	Re{Y11}	Im{Y11}	Q	L(in nH)
1GHz	0,006846	-0,0179	2,615	8,89
2.4GHz	0,002517	-0,00742	2,948	8,94
5GHz	0,00189	-0,00299	1,582	10,64
f(self resonant)	11.24 GHz			
J1				
1mA				
f	Re{Y11}	Im{Y11}	Q	L(in nH)
1GHz	0,0078	-0,02097	2,688	7,59
2.4GHz	0,00286	-0,00872	3,048	7,605
5GHz	0,002079	-0,00367	1,765	8,67
f(self resonant)	12.27 GHz			

The following conclusions can be extracted from the above numerical observations:

- Increase in J1 leads to increase in g_{m2} and C_{gs2}.
- Increase in g_{m2} decreases $R_{p.}$
- Decrease in C_{gs2}/g_{m2} decreases L (inductance).

Hence, decrease in parallel resistance (R_p) and inductance (L) does not change the Q factor much, but for the same Q, we get different values of L (where L decreases as current J1 increases).

Now, keeping the value of J1=500µA, we change the current J2 to change the parameters as given in the table below:

Table 3.2:Simulation of active inductors - 2

J1=500uA				
J2	1uA	2uA	10uA	20uA
gm1(in mA/V)	0,0348	0,0572	0,2241	0,3912
gm2(in mA/V)	1.821	1.806	1.802	1.801
Cgs1(in fF)	8,22	8,69	10,91	11,81
Cgs2(in fF)	12,35	12,34	12,33	12.329
J2	100uA	200uA	500uA	1mA
gm1(in mA/V)	1.075	1.392	1.778	2.096
gm2(in mA/V)	1.792	1.789	1.781	1.763
Cgs1(in fF)	12.576	12.603	12.589	12.569
Cgs2(in fF)	12.318	12,31	12.307	12.329

J2				
100uA				
f	Re{Y11}	Im{Y11}	Q	L(in nH)
1GHz	0,00286	-0,0116	4,055	13.72
2.4GHz	0,00175	-0,00451	2,577	14.7
5GHz	0,00161	-0,00155	0,963	20.54
f(self resonant)	8.65 GHz			
200uA				
f	Re{Y11}	Im{Y11}	Q	L(in nH)
1GHz	0,0039	-0,0146	3,74	10.9
2.4GHz	0,00201	-0,00582	2,895	11.39
5GHz	0,00172	-0,00222	1,291	14.34
f(self resonant)	9.83 GHz			
500uA				
f	Re{Y11}	Im{Y11}	Q	L(in nH)
1GHz	0,0063	-0,01796	2,85	8.86
2.4GHz	0,00252	-0,0074	2,936	8.96
5GHz	0,00189	-0,00299	1,582	10.64
f(self resonant)	11.18 GHz			
1mA				
f	Re{Y11}	Im{Y11}	Q	L(in nH)
1GHz	0,0094	-0,0194	2,064	8.2
2.4GHz	0,00314	-0,00856	2,726	7.75
5GHz	0,00208	-0,00362	1,74	8.79
f(self resonant)	12.33 GHz			

The following conclusions can be extracted from the above numerical observations:

- Increase in J2 leads to increase in g_{m1} and C_{gs1}.
- Increase in g_{m1} leads to decrease in the series resistance (R_s) and also the inductance (L).

Hence decrease in both series resistance (R_s) and inductance (L), does not change the Q factor much, but for the same Q, we get different values of L (where L decreases as current J2 increases).

Conclusion:

Changing the bias values changes the parameters of the active inductors as expected. This has led us to characterize an active inductor having a good quality factor of greater than 2.5 in the 1 GHz to 3 GHz range. The target of this chapter is to make some changes in the topology to get an optimized performance (i.e. better quality factor in this case). Nevertheless, before changing topology, we will replace the ideal current

sources J1 and J2 by transistors sourcing the same current value. Since saturated transistors behave as lossy, non-ideal current sources, we will evaluate the performance loss when using non-ideal elements.

3.2)Basic Active Inductor with lossy saturated transistors replacing the ideal current sources

Now, we replace the ideal current sources with transistors in saturation to get similar performance. We keep transistor (M3) biasing the feedback transistor (M2) and transistor (M4) biasing the main transistor (M1).

The schematic looks as following:

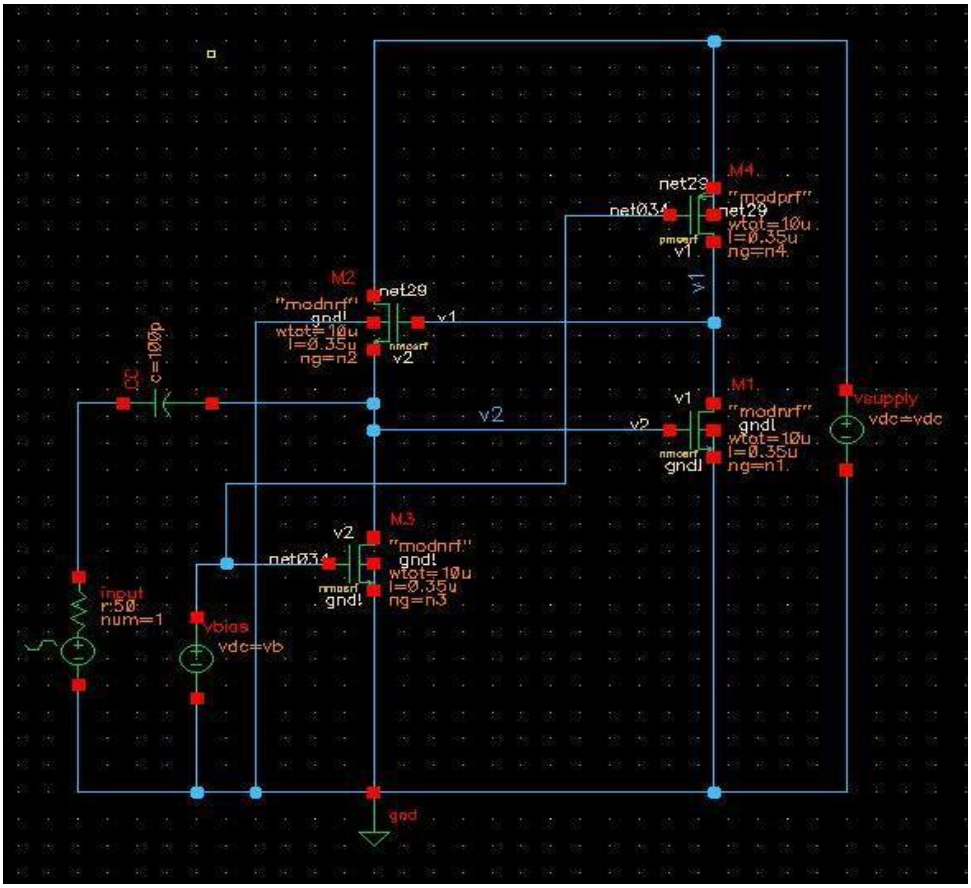


Fig. 3.3: Schematic: Basic Active Inductor 2

We have seen in the previous section that changing the parameters of the transistor (like g_m,C_{gs}) changes the parameters of the active inductor. Changing the parameters of this transistor can be done in two ways – changing the width of the transistor or changing the bias points (or voltages).

As transistors have to be always operated under saturation, their voltage swing is limited between V_T to V_{DD}-V_T-V_{SAT}. Hence we cannot use them for tuning for a long range of inductances (since inductance value depends on g_m, C_{gs}).

So, for larger tuning, we can change the widths of the transistors and get the parameters like the previous section. Changing the widths gives us larger tuning. But since fabrication is permanent, we cannot change the widths of the transistors after fabrication. Hence, in the next section when we use these active inductors in the LNA´s, we will keep the width of the transistor having the optimum value of inductance. Then we can tune the inductance for a small range (fine tuning) by changing the bias voltage.

In this section we change the values of widths of the transistors and keep the bias voltage (of transistors M3 and M4 which bias the main transistor (M1) and feedback transistor (M2), respectively) to be 1.5 V (for all subsequent stages) and try to get an optimized active inductor.

First, we start with changing the values of width of transistor (M2). We get the following values of the parameters:

Table 3.3:Simulation of active inductors using transistors - 1

W2						
10µm					gm1	1.726mA/V
f	Re{Y11}	Im{Y11}	Q	L(in nH)	gm2	1.977mA/V
1GHz	0,0069	-0,0085	1,223	18.85	Cgs1	12.57fF
2.4GHz	0,0032	-0,0037	1,182	17.59	Cgs2	12.33fF
f(self resonant)	6.48 GHz				g01	37.73uA/V

20µm					gm1	1.737mA/V
f	Re{Y11}	Im{Y11}	Q	L(in nH)	gm2	3.362mA/V
1GHz	0,0083	-0,0132	1,582	12.06	Cgs1	12.6fF
2.4GHz	0,0041	-0,0054	1,302	12.31	Cgs2	24.64fF
f(self resonant)	6.42 GHz				g01	38.46uA/V
30µm					gm1	1.74mA/V
f	Re{Y11}	Im{Y11}	Q	L(in nH)	gm2	4.553mA/V
1GHz	0,0089	-0,0156	1,755	10.21	Cgs1	12.62fF
2.4GHz	0,0048	-0,0062	1,258	11.01	Cgs2	36.94fF
f(self resonant)	6.33 GHz				g01	39.1uA/V
50µm					gm1	1.743mA/V
f	Re{Y11}	Im{Y11}	Q	L(in nH)	gm2	6.525mA/V
1GHz	0,0089	-0,0172	1,932	9.25	Cgs1	12.63fF
2.4GHz	0,0057	-0,0061	1,074	10.83	Cgs2	61.5fF
f(self resonant)	5.58 GHz				g01	39.83uA/V

- Increase in width of M2 (W2) leads to increase in g_{m2} and C_{gs2}.
- Increase in g_{m2} leads to decrease in parallel resistance (R_p) and series resistance (R_s). Hence Q factor increases as the width increases.
- There is increase in C_{gs2} as well as g_{m2}. But C_{gs2}/g_{m2} decreases. This leads to decrease in resonant frequency and a decrease in inductance (L).

Next, we change the values of width of transistor (M3). We get the following values of the parameters:

Table 3.4:Simulation of active inductors using transistors - 2

W3						
20µm					gm1	1.739mA/V
f	Re{Y11}	Im{Y11}	Q	L(in nH)	gm2	7.959mA/V
1GHz	0,0111	-0,0208	1,897	7.63	Cgs1	12.61fF
2.4GHz	0,0068	-0,0075	1,101	8.85	Cgs2	61.62fF
f(self resonant)	5.69 GHz				g01	38.81uA/V

30µm					gm1	1.735mA/V
f	Re{Y11}	Im{Y11}	Q	L(in nH)	gm2	8.8mA/V
1GHz	0,0125	-0,0229	1,832	6.95	Cgs1	12.59fF
2.4GHz	0,0076	-0,0081	1,075	8.15	Cgs2	61.69fF
f(self resonant)	5.58 GHz				g01	38.17uA/V
50µm					gm1	1.726mA/V
f	Re{Y11}	Im{Y11}	Q	L(in nH)	gm2	9.913mA/V
1GHz	0,0147	-0,0259	1,762	6.15	Cgs1	12.57fF
2.4GHz	0,0088	-0,0088	0,996	7.58	Cgs2	61.84fF
f(self resonant)	5.31 GHz				g01	37.73uA/V

- Increase in width of M3(W3) means there is an increase in current J1. This leads to increase in g_{m2}, but this does not change C_{gs2} and hence we get decrease in R_p and R_s.
- Increase in g_{m2} leads to decrease in inductance (L), and also decrease in resonant frequency.

We see that we have achieved inductance of nearly 8nH in this case and hence we are getting a good approximation of the ideal current source in this case. In the further cases we will try to get a good range of inductance by further increasing the width of the other transistor and invariably increasing the current.

Now that we have properly biased the transistor (M2), we change the values of width of transistor (M1). We get the following values of the parameters:

Table 3.5:Simulation of active inductors using transistors - 3

W1						
20µm					gm1	2.905mA/V
f	Re{Y11}	Im{Y11}	Q	L	gm2	9.91mA/V
1GHz	0,0188	-0,038	2,02	4.188	Cgs1	25.21fF
2.4GHz	0,011	-0,0141	1,41	4.703	Cgs2	61.82fF
f(self resonant)	6.26 GHz				g01	52.75uA/V
30µm					gm1	3.854mA/V
f	Re{Y11}	Im{Y11}	Q	L	gm2	9.905mA/V
1GHz	0,0212	-0,0471	2,217	3.381	Cgs1	37.82fF
2.4GHz	0,0109	-0,0172	1,577	3.855	Cgs2	61.83fF
f(self resonant)	6.65 GHz				g01	63.63uA/V

50µm					gm1	5.254mA/V
f	Re{Y11}	Im{Y11}	Q	L	gm2	9.897mA/V
1GHz	0,0231	-0,0551	2,391	2.891	Cgs1	62.91fF
2.4GHz	0,0121	-0,0196	1,619	3.383	Cgs2	62.84fF
f(self resonant)	6.69 GHz				g01	78.97uA/V

- Increasing the width of M1 increases g_{m1}, C_{gs1} and g_{01}.
- Increase in g_{m1} has led to decrease in inductance (L) value.
- Increase in g_{01} has led to increase in R_s.

There is decrease in both series resistance (R_s) and inductance (L) and this has led to increase in Q factor and a decrease in the inductance (L) value.

We next increase the width of M4. This means increasing the current J2, means there is an increase in gm1. But this also increases g01 to such an extent that it increases the series resistance and hence we get a much degraded quality factor and hence we keep the width of M4 to a minimum of 10µm.

Conclusion:

We have characterized the transistors to get an optimized performance. The series resistance seems to causing a difficulty in optimizing the active inductor more. Hence, we have to make some changes to this topology to get an improved performance. We keep the widths of transistors and the bias voltages as a reference for further improvement. We keep W1=W2=W3=50µm and W4=10µm and try to get a better quality factor in the subsequent stages.

3.3)Yodprasit – Ngarmnil Active Inductor

As the series resistance was causing problem, we have to make a change in the topology to compensate for it i.e. nullify the effect of series resistance.

As seen before, the spiral inductor can be modelled as a combination of inductor, resistor and capacitor in parallel. The parallel equivalent inductance and resistance of an inductor and resistor in series is:

$$L' = L\left(1 + \frac{1}{Q^2}\right)$$

$$R_p' = R_p\left(1 + Q^2\right)$$

To nullify the effect of this resistance, we can add a negative resistance in parallel and hope to get a better quality factor.

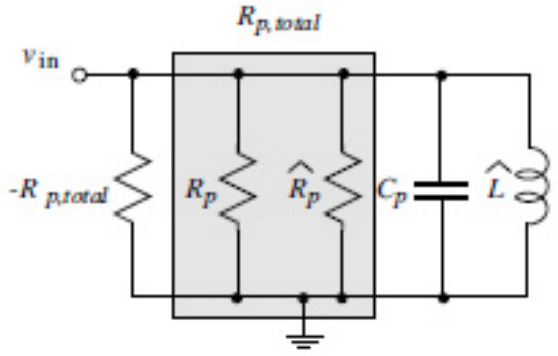


Fig. 3.4: Parallel equivalent model and change

This configuration is called Yodprasit-Ngarmnil active inductor and this is implemented by adding a transistor M2 and adding current sources (J3 and J2) according to the Fig.3.5.

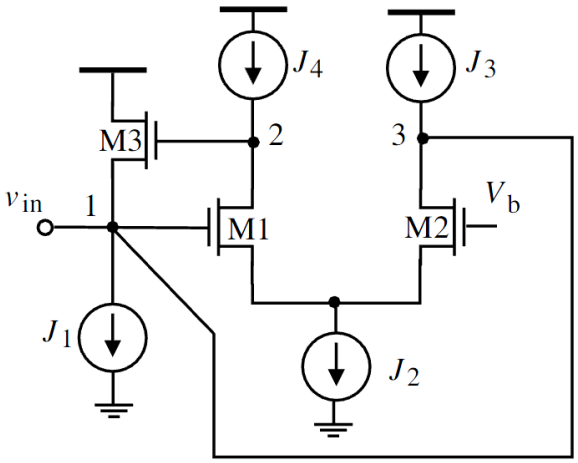


Fig. 3.5: Yodprasit-Ngarmnil active inductor

In this topology the widths are: W1=W3=W4=50µm and W6=10µm. Now, we have the liberty of changing the widths of transistor M2, M5 (replacing current source J_2) and M7(replacing current source J_3). M5 is the transistor which acts as a common current source (replacing J2) for the transistors M1 and M2 and hence changing the width of M5, changes the parameters of this active inductor topology.

The schematic is shown as given in Fig. 3.6:

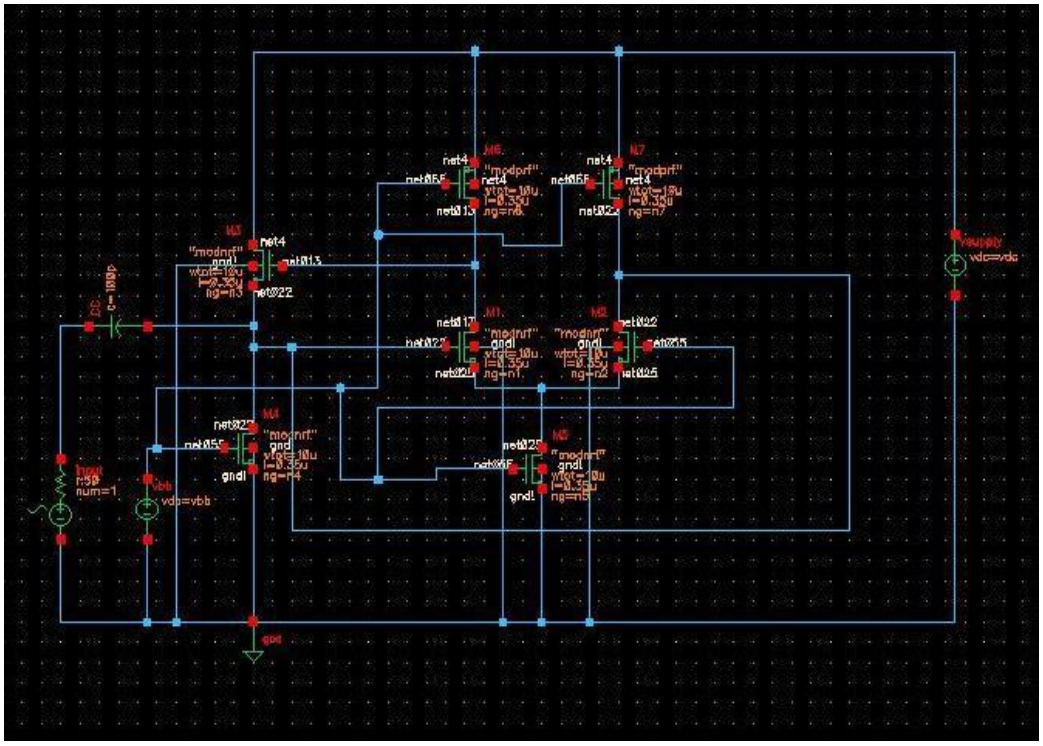


Fig. 3.6: Schematic: Yodprasit Ngarmnil Active Inductor

First, we change the width of transistor (M5) by keeping other widths (M7 and M2) to be at a minimum of 10µm.

Table 3.6: Simulation of Yodprasit-Ngarmnil active inductors

W5					gm1	5.226mA/V
10µm					Cgs1	61.87fF
f	Re{Y11}	Im{Y11}	Q	L(in nH)	gm3	10.85mA/V
1GHz	0,0214	-0,0126	0,588	12.631	Cgs3	62.85fF
2.4GHz	0,013	-0,0054	0,414	12.326	g01	89.12uA/V
f(self resonant)	4.24 GHz				g03	397uA/V
20µm					gm1	5.664mA/V
f	Re{Y11}	Im{Y11}	Q	L(in nH)	Cgs1	62.27fF
1GHz	0,026	-0,024	0,935	6.549	gm3	10.95mA/V
2.4GHz	0,0136	-0,0099	0,734	6.645	Cgs3	62.22fF
f(self resonant)	5.1 GHz				g01	94.68uA/V
					g03	381.8uA/V

50µm					gm1	5.873mA/V
f	Re{Y11}	Im{Y11}	Q	L(in nH)	Cgs1	62.58fF
1GHz	0,0308	-0,0415	1,347	3.835	gm3	11.02mA/V
2.4GHz	0,0146	-0,0163	1,109	4.068	Cgs3	62.12fF
f(self resonant)	6 GHz				g01	95.9uA/V
					g03	376.2uA/V
100µm					gm1	5.925mA/V
f	Re{Y11}	Im{Y11}	Q	L(in nH)	Cgs1	62.7fF
1GHz	0,0342	-0,051	1,491	3.121	gm3	11.04mA/V
2.4GHz	0,0153	-0,0196	1,281	3.383	Cgs3	62.1fF
f(self resonant)	6.39 GHz				g01	95.75uA/V
					g03	376.3uA/V
200µm					gm1	5.947mA/V
f	Re{Y11}	Im{Y11}	Q	L(in nH)	Cgs1	62.77fF
1GHz	0,0357	-0,056	1,568	2.842	gm3	11.05mA/V
2.4GHz	0,0157	-0,022	1,401	3.014	Cgs3	62.09fF
f(self resonant)	6.62 GHz				g01	95.58uA/V
					g03	377uA/V

$$Q = \frac{\sqrt{g_{m3} g_{m1} C_{gs3} C_{gs1}}}{C_{gs1} g_{01} + 2 C_{gs3} g_{03}}$$

- A high value of g_{01} and g_{03} degrades the quality factor here (compared to basic active inductor).
- Here increase in the width of M5 increases g_{m1} and hence the quality factor.
- Further increase in width of M5 can increase the quality factor only upto 1.5 at 1 GHz and also 2.4GHz.

We now keep the width of 50µm at M5 and increase the width of M2 and M6. Increasing the width of M2 and M6 degrades the quality factor as it increases g_{01} much more. Hence we keep the widths of M2 and M6 to a minimum of 10µm.

Conclusion:

We find the quality factor to a maximum of 1.5. This topology has not succeeded in increasing the quality factor, compared to the basic active inductor. Hence we have to look for a different topology.

3.4)Weng – Kuo Cascode Active Inductor

Compensating for the series resistance, we add a cascode transistor (M3) to the main transistor. As seen in the case of basic active inductors, changing the widths of the transistors changes the transconductance and gate capacitance at the same time i.e. we cannot tune the inductance and quality factor independently. By adding a transistor in cascode, we can tune the inductance and quality factor independently (it is seen that g_{m1} is proportional to J1+J3 while g_{m3} is only proportional to J1). The topology considered can be shown as in Fig. 3.7 and its schematic as in Fig. 3.8.

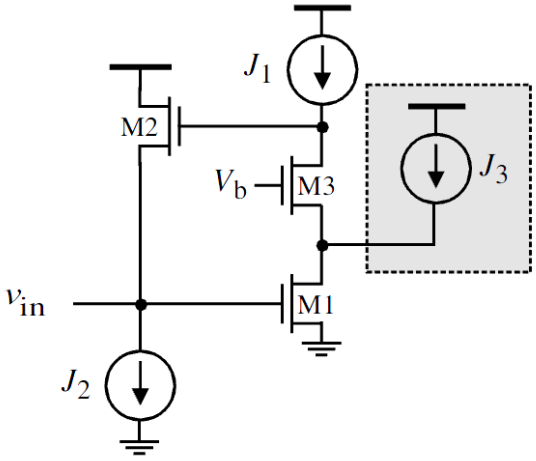


Fig. 3.7: Weng - Kuo Active Inductor

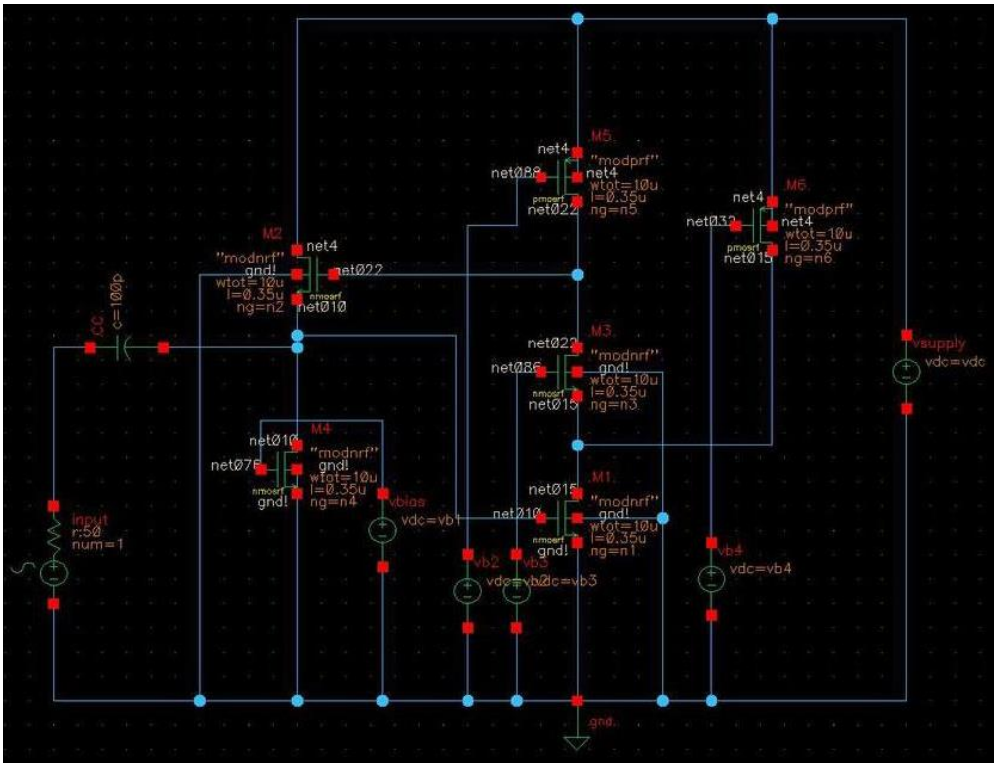


Fig. 3.8:Schematic: Weng - Kuo Active Inductor

In this topology as a difference to the basic active inductor we have transistor M3 as the cascode transistor. Its bias voltage is 1.5V (the bias voltage is fixed here and will be changed later while designing the LNA). We have kept transistor (M6) as an equivalent to current source J3 and its bias voltage to be 1.5V.As this topology is a modification to the topology of basic active inductor. We keep W1 (main transistor)=W2 (feedback transistor)=W4 (current source biasing M2)=50µm and W5 (current source biasing M1)=10µm.

The characterization of active inductor is different from the basic topology.

$$L = \frac{C_{gs2}}{g_{m1} g_{m2}}$$

$$R_s = \frac{g_{01} g_{03}}{g_{m1} g_{m2} g_{m3}} \text{ instead of } R_s = \frac{g_{01}}{g_{m1} g_{m2}} \text{ for basic active inductor.}$$

$$C_p = C_{gs1}$$

$$R_p = \frac{1}{g_{02}}$$

The self – resonant frequency is given by

$$\omega_0 = \sqrt{\frac{g_{m1} g_{m2}}{C_{gs1} C_{gs2}}}$$

$$Q = \frac{\omega L}{R_s} = \frac{\omega C_{gs2} g_{m3}}{g_{01} g_{02}} \quad \text{instead of } Q = \frac{\omega C_{gs2}}{g_{01}} \text{ for the basic active inductor.}$$

We keep the value of width of transistor M3 (W3) to be at a minimum of 10µm.

So now we increase the width of transistor (M6) to check the parameters.

Table 3.7:Simulation of weng-kuo active inductors - 1

W6	20µm	30µm	50µm
gm1	7.277mA/V	7.798mA/V	8.587mA/V
Cgs1	68.39fF	69.33fF	70.48fF
gm2	10.92mA/V	10.9mA/V	10.85mA/V
Cgs2	62.28fF	62.47fF	63.05fF
gm3	1.796mA/V	1.739mA/V	1.573mA/V
Cgs3	12.44fF	12.41fF	12.36fF
g01	1.068mA/V	1.441mA/V	1.922mA/V
g02	385.6uA/V	401.3uA/V	437.1uA/V
g03	43.78uA/V	41.53uA/V	35.62uA/V

W6				
20µm				
f	Re{Y11}	Im{Y11}	Q	L(in nH)
1GHz	0,0341	-0,0529	1,551	3
2.4GHz	0,0028	-0,0186	6,663	3.561
f(self resonant)	4.79 GHz			
30µm				
f	Re{Y11}	Im{Y11}	Q	L(in nH)
1GHz	0,0347	-0,0412	1,182	3.881
2.4GHz	0,00479	-0,0174	3,634	3.813
f(self resonant)	4.75 GHz			

50µm				
f	Re{Y11}	Im{Y11}	Q	L(in nH)
1GHz	0,0319	-0,0266	0,833	5.981
2.4GHz	0,00745	-0,0142	1,906	4.672
f(self resonant)	4.59 GHz			

- Increasing the width of M6 (W6) increases the value of g_{m1} and g_{02} and hence decreases both R_p as well as R_s. The decrease in parallel resistance is more pronounced and hence this leads to degradation in the quality factor.
- g_{m1} decreases, but the decrease is not much. Degradation in quality factor has led to an increase in effective inductance, as compared to the expectation of an increase in inductance value due to a decrease in g_{m1}.

Hence we keep the value of width of M6 to a minimum of 10µm.

Now, we change the values of width of transistor M3 (the cascode transistor).

Table 3.8: Simulation of weng-kuo active inductors - 2

W3	10µm	20µm	30µm	50µm
gm1	6.559mA/V	6.881mA/V	6.96mA/V	7.019mA/V
Cgs1	67.52fF	66.8fF	66.7fF	66.63fF
gm2	10.94mA/V	10.94mA/V	10.94mA/V	10.94mA/V
Cgs2	62.14fF	62.13fF	62.13fF	62.12fF
gm3	1.838mA/V	3.091mA/V	4.138mA/V	5.76mA/V
Cgs3	12.47fF	24.91fF	37.33fF	62.09fF
g01	658.3uA/V	404.3uA/V	353.8uA/V	318.5uA/V
g02	372.9uA/V	371.9uA/V	371.6uA/V	371.4uA/V
g03	46.03uA/V	67.46uA/V	83.67uA/V	107.7uA/V

W3				
10µm				
f	Re{Y11}	Im{Y11}	Q	L(in nH)
1GHz	0,0295	-0,0781	2,647	2.041
2.4GHz	0,00365	-0,0245	6,712	2.706
f(self resonant)	7.26 GHz			
20µm				
f	Re{Y11}	Im{Y11}	Q	L(in nH)
1GHz	0,0262	-0,0748	2,855	2.127
2.4GHz	0,0022	-0,0241	10,955	2.763
f(self resonant)	7.28 GHz			

30µm				
f	Re{Y11}	Im{Y11}	Q	L(in nH)
1GHz	0,0269	-0,0671	2,494	2.381
2.4GHz	0,0011	-0,0201	18,273	3.299
f(self resonant)	7.32 GHz			
50µm				
f	Re{Y11}	Im{Y11}	Q	L(in nH)
1GHz	0,0219	-0,0641	2,927	2.486
2.4GHz	0,00088	-0,0199	22,546	3.332
f(self resonant)	7.34 GHz			

- g_{03} increases and g_{01} decreases as the width increases. Also g_{m3} increases, hence the quality factor increases. The quality factor increases as the width of M3 increases.
- The parameters of inductance L (i.e. g_{m1},g_{m2},C_{gs2}) do not change much. Also due to a high quality factor the effective inductance does not change much. In this case it just increases slightly (not a significant change).

Conclusion:

At the expense of adding two more transistors, we have got a very good quality factor with a maximum of 22. But as more current sources are used, this topology has higher power consumption. Also adding transistors may lead to a higher non-linearity. Hence this topology has succeeded in giving a good quality factor at the expense of higher power consumption and can be used in the LNA´s.

3.5)Using a resistive feedback – topology

To decrease the power consumption and non-linearity, we use a different topology (retaining the same motive of increasing the quality factor and inductance range). We use a resistance here (a linear element). The idea behind using a resistance in feedback is to increase the parallel resistance. The feedback resistance should decrease the effect of series resistance and hence lead to an increase in quality factor. The schematic is as follows:

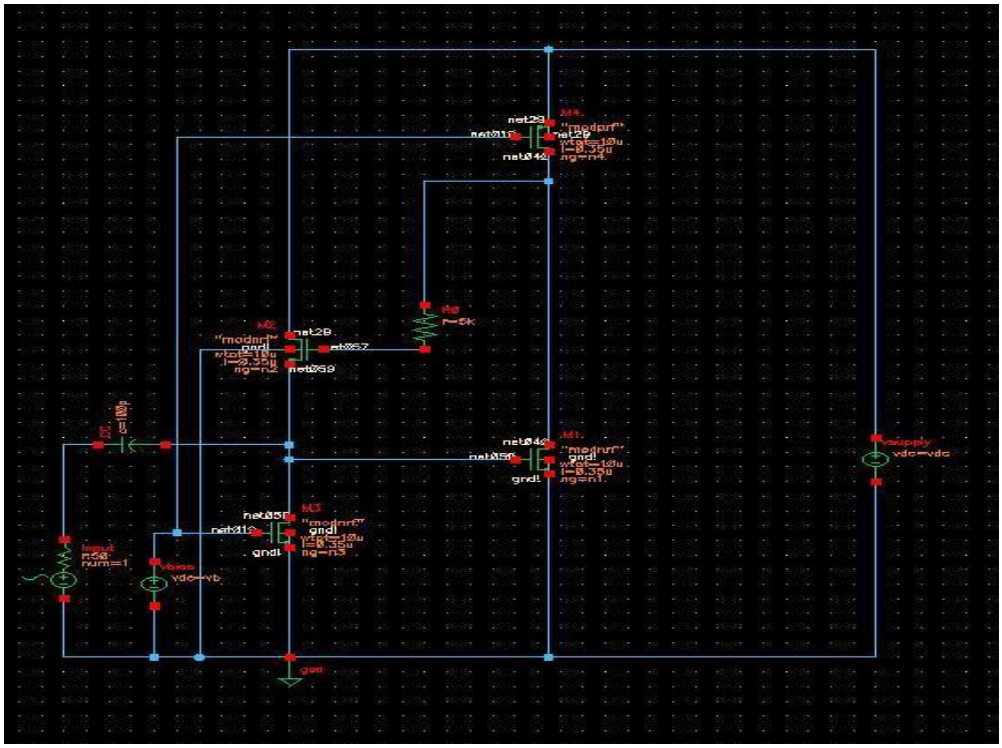


Fig.3.9: Schematic: Resistive Feedback Active Inductor

For different values of feedback resistance we get the following observations:

Table 3.9: Simulation of resistive feedback active inductors 1

R				
100Ω				
f	Im{Y11}	Re{Y11}	Q	L
1GHz	-0,0632	0,0348	1,81	2.526nH
2.4GHz	-0,0246	0,0143	1,72	2.695nH
500Ω				
f	Im{Y11}	Re{Y11}	Q	L
1GHz	-0,0649	0,0277	2,343	2.452nH
2.4GHz	-0,0237	0,0086	2,758	2.798nH
1kΩ				
f	Im{Y11}	Re{Y11}	Q	L
1GHz	-0,064	0,0191	3,368	2.486nH
2.4GHz	-0,0206	0,0034	6,005	3.219nH
2kΩ				
f	Im{Y11}	Re{Y11}	Q	L
1GHz	-0,0592	0,0065	9,063	2.697nH
2.4GHz	-0,0134	0,00073	18,306	4.948nH

- Increasing the resistance increases R_p (parallel resistance) and decreases the effect of series resistance. Hence the quality factor increases as the resistance (R) increases. Also the inductance value does not change much.

Conclusion:

We get quality factor upto maximum of 18.3 at a parallel resistance of 2kΩ. The increasing quality factor is at the expense of higher noise due to resistance.

3.6)Using a regulated cascode:

In the previous section, we saw addition of a noisy element (resistor) in the circuit. So, we move on to design a new topology which uses the regulated cascode method. The topology is shown in Fig. 3.10 and the schematic is shown in Fig. 3.12.

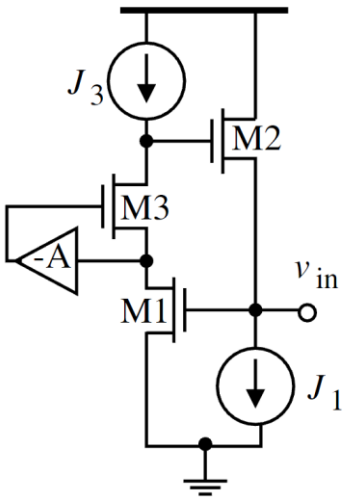


Fig 3.10: Regulated Cascode Active Inductor

Here in place of a negative amplifier, we have kept an inverter of nmos transistor (M6) and pmos transistor (M7) in the fashion as shown in Fig 3.11:

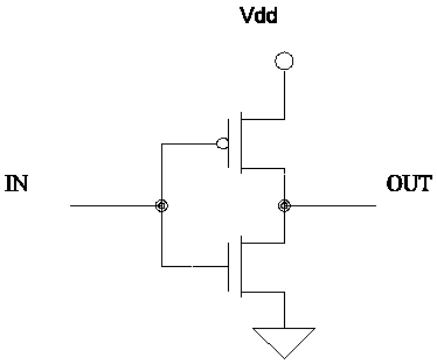


Fig 3.11: A typical CMOS inverter

This inverter used in the active inductor acts as a negative amplifier by taking the input as the voltage at the drain of main transistor (M1) and feeding it back to the cascode transistor (M3 according to the topology shown and M5 according to the schematic as shown in Fig. 3.12).

Now, changing the values of widths of the transistors, we try to get optimized performance.

In this case the expression for series resistance is what changes from that of the basic active inductor as shown below:

$$R_s = \frac{G_{01}}{g_{m1} g_{m2}} \text{ where}$$

$G_{01} = g_{01}$ for basic active inductor &

$$G_{01} = \frac{1}{g_{01}(r_{06} g_{m6})(r_{07} g_{m7})} \text{ for regulated cascode active inductor}$$

Keeping the width of the cascode transistor (M5) at a minimum of 10µm, we change the values of the widths of transistor (M6 and M7) which make up the inverter (to change r_{06},g_{m6},r_{07},g_{m7}):

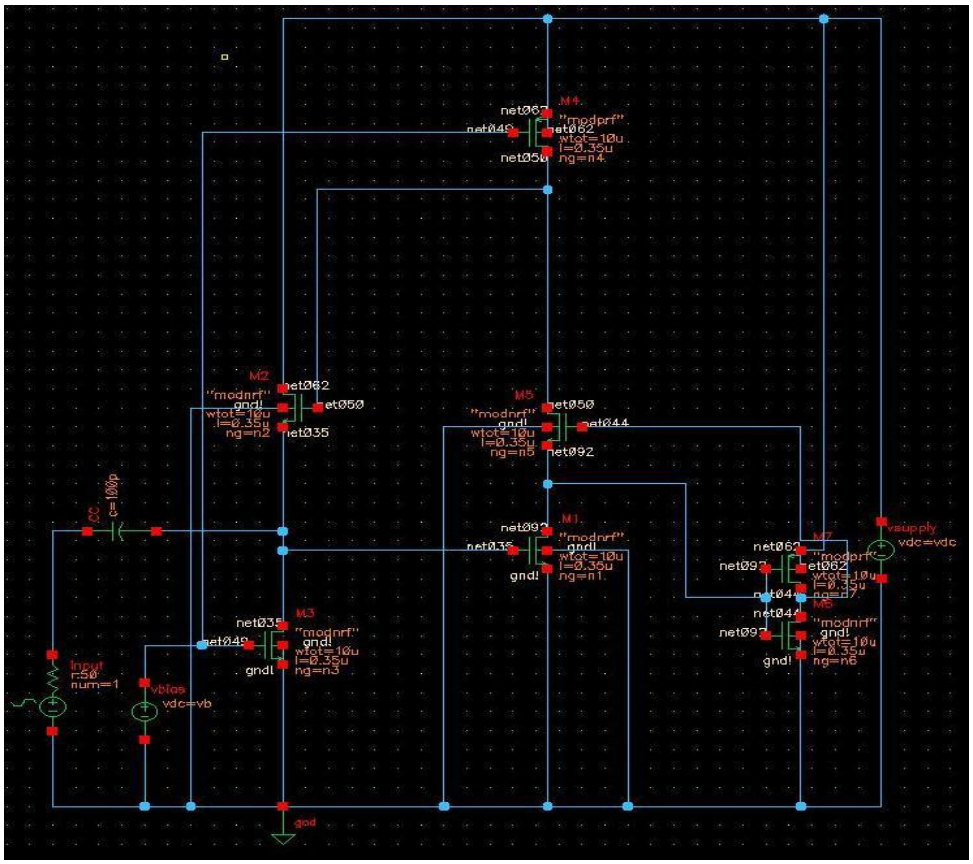


Fig 3.12 : Schematic: Regulated Cascode Active Inductor

Table 3.10 :Simulation of regulated cascode active inductors

Inverter				
W6	W7			
10µm	10µm			
f	Im{Y11}	Re{Y11}	Q	L
1GHz	-0,042	0,055	0,764	3.789nH
2.4GHz	-0,0295	0,0126	2,341	2.248nH
W6	W7			
20µm	20µm			
f	Im{Y11}	Re{Y11}	Q	L
1GHz	-0,0431	0,052	0,827	3.701nH
2.4GHz	-0,028	0,0097	2,889	2.368nH
W6	W7			
10µm	20µm			
f	Im{Y11}	Re{Y11}	Q	L
1GHz	-0,045	0,051	0,882	3.536nH
2.4GHz	-0,026	0,0082	3,17	2.551nH
W6	W7			
10µm	50µm			
f	Im{Y11}	Re{Y11}	Q	L
1GHz	-0,048	0,039	1,233	3.308nH
2.4GHz	-0,0171	0,0031	5,516	3.878nH
W6	W7			
50µm	50µm			
f	Im{Y11}	Re{Y11}	Q	L
1GHz	-0,0469	0,045	1,042	3.393nH
2.4GHz	-0,0215	0,0028	7,651	3.084nH

Increasing the width of the transistors making up the inverter, we are increasing the g_{m6} and g_{m7} and hence decreasing the series resistance. Hence this topology has succeeding in decreasing the series resistance and so we get a better quality factor compared to the basic active inductor.

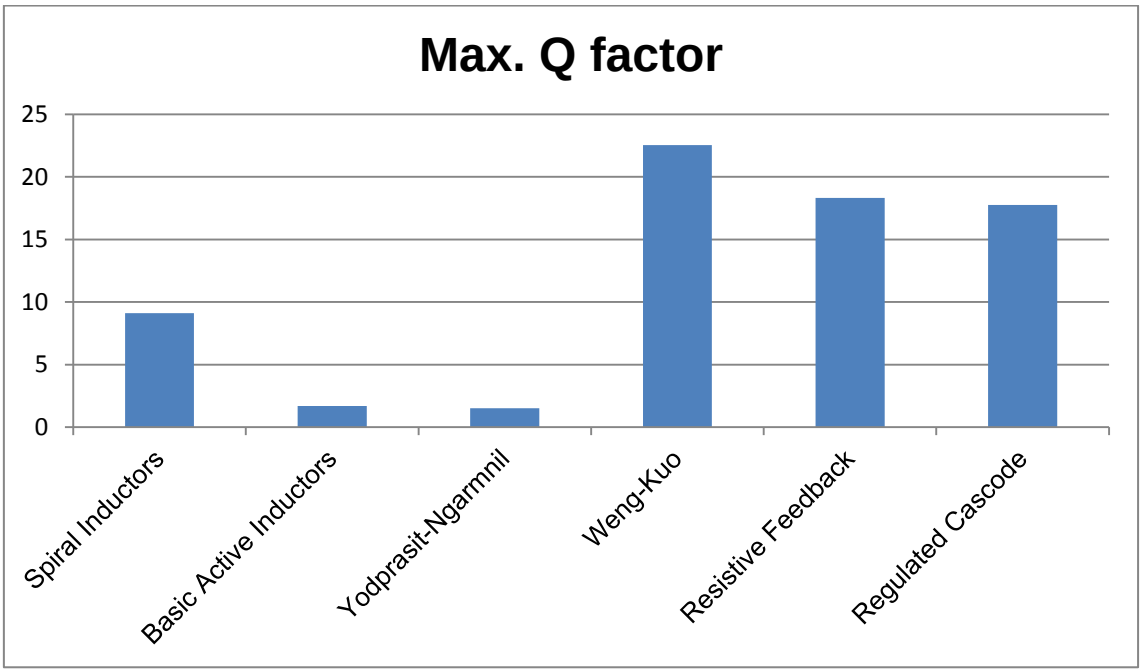
Conclusion:

Hence, in this topology gives a good quality factor of a maximum of 17 at 2.4 GHz.

However, due to the addition of three more transistors (compared to basic active inductors), it introduces more non-linearity in the circuit.

3.7)Conclusion on Active Inductors

This section consists of summarizes the main results that we have found in the previous sections.



With the above graph we can see that we can get a very good quality factor with active inductors also compared to spiral inductors.

We started with a basic active inductor consisting of back to back transistors. In the subsequent sections we have tried to decrease the series resistance (as the series resistance was causing a problem and leading to low quality factor).

As said before, we have changed the widths (keeping the bias voltage of the biasing transconductors constant) in this section to get a wide range of inductance. Numerically, the inductances we got ranged from 1nH to 15nH. Thus we got a very wide range of inductances.

We will choose an optimal inductance value, by selecting the width corresponding to the value required. For example, for a 1pF load to resonate at 2.4 GHz, we will need a 4nH inductor. Now, changing of bias voltage (within the voltage swing constraint) also

changes inductance and invariably the frequency of operation and this will be seen in the next section.

The Yodprasit-Ngarmnil active inductor did not change the quality factor much and hence will not be used in the next section. Also the regulated cascode has addition of three transistors to the topology and hence can be expected to have more non-linearity. If power consumption is neglected, then weng-kuo cascode can be expected to be the best active inductor in terms of quality factor and also noise figure.

In the next section we will use these active inductors along with spiral inductors in tuned narrowband LNA and wideband LNA.

4)Tuned narrowband LNA

An LNA can be characterized on the basis of its gain, noise figure, isolation, matching and linearity. The figures of merit ideally found in an LNA are:

- Low noise figure
- Moderate gain
- Good input matching (usually 50Ω)
- Isolation between input and output
- Acceptable linearity(low distortion)
- Stability
- Low power consumption

In the subsequent stages we will be characterizing the LNA´s on the basis of above factors and try to get an optimized LNA. The s – parameters are an excellent way to know about the matching, isolation and gain. Consider a two-port network as shown in the figure below:

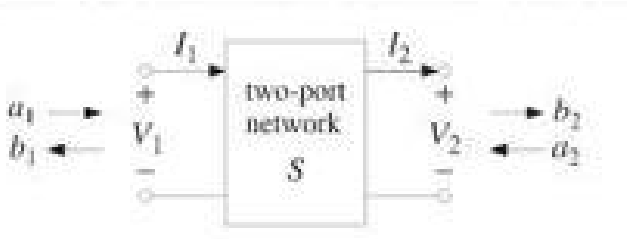


Fig. 4.1: A two-port network

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11}S_{12} \\ S_{21}S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix}$$ ----- scattering matrix

The s-parameters are given by

$$S_{11} = \frac{b_1}{a_1}, S_{12} = \frac{b_1}{a_2}, S_{21} = \frac{b_2}{a_1}, S_{22} = \frac{b_2}{a_2}$$

Hence S_{11} gives input matching, S_{12} gives the isolation from input to output, S_{21} gives the gain and S_{22} gives the output matching.

Noise figure (NF):

The noise figure characterizes the degradation of signal to noise ratio at the receiver and it has to be at the lowest possible level, typically in the range of 2-3 dB.

$$NF = \frac{(SNR)_{output}}{(SNR)_{input}}$$

The receivers have to deal with very low power signals. The noise added by the circuit should therefore be small in order not to degrade the signal-to-noise ratio and guarantee that the information is correctly received. Hence the noise figure is very critical in the design of LNA.

Linearity (IIP3):

Ideally an amplifier should behave linearly:

$$y(t) = \alpha x(t)$$

But, a more realistic situation is:

$$y(t) = \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) + ...$$

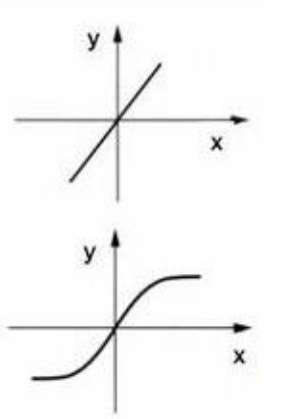


Fig. 4.2: transfer function graph

Intermodulation:

One important effect of circuit non-linearity is the appearance of intermodulation products when two different frequencies are present at the input. This phenomena gives rise to a parameter to quantify the non-linearity, which is the IIP3 or third-order interception point. Consider an input signal of

$$x(t) = A\cos(\omega_1 t) + A\cos(\omega_2 t)$$

If we take the cube of x(t) we see that we get components at frequencies of $2\omega_2$-ω_1 and $2\omega_1$-ω_2 which interfere with the amplified signal at frequencies ω_1 and ω_2.

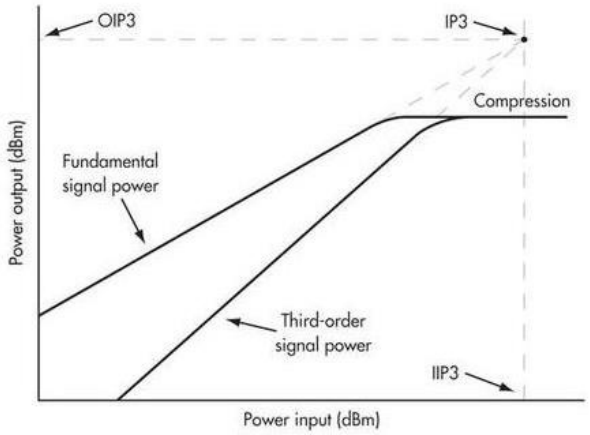


Fig. 4.3: calculating IIP3

By definition, the IIP3 is the input power at which the power of the amplifier signals at frequencies w1 or w1 matches the power of the intermodulation products at $2\omega_2-\omega_1$ and $2\omega_1-\omega_2$. It is obtained after a two-tone test of signals with the same amplitudes and similar frequencies. The measurement is done at low power levels, and IIP3 can be found by extrapolating the point, from where the signal has started the compression. Higher the IIP3, more the linearity and hence the amplifier behaves more ideally.

4.1)Tuned LNA design using spiral inductors

We show here the design of a narrowband LNA tuned at 2.4 GHz, using the common inductively degenerated common-source cascode configuration. The inductances used here are to match the LNA to the source resistance of 50Ω and also to resonate at the frequency of operation. The cascode structure is used to isolate the output port from the input port. At the output port, an inductance is used to resonate at a frequency of $f = \frac{1}{2\pi\sqrt{LC}}$ where C comes from the drain parasitics of the cascode transistor and, mainly, from the input capacitance of the subsequent stage.

The schematic of the LNA is:

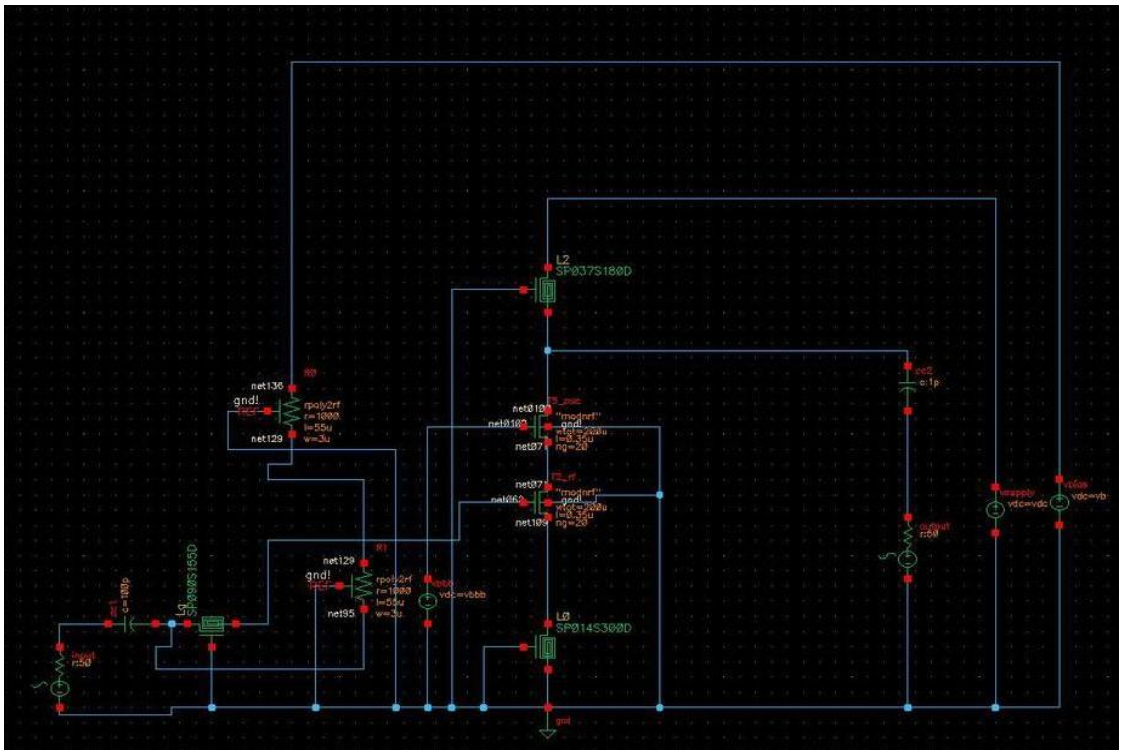


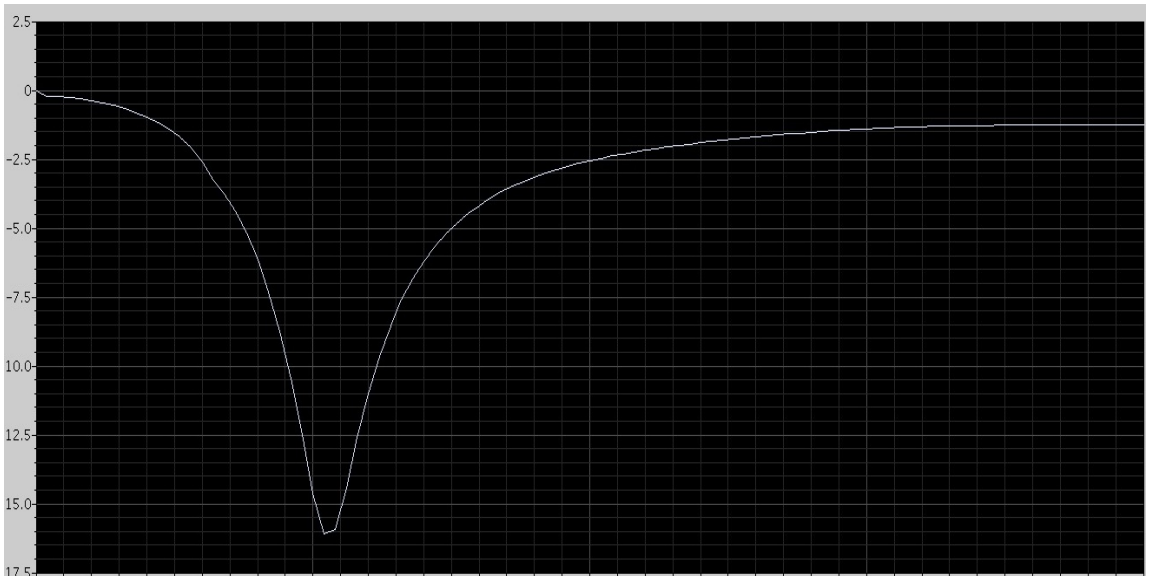
Fig. 4.4:Schematic: Tuned LNA using spiral inductors

In this LNA we have used, input of peak amplitude 0.1mV. The gate inductance Lg=SP090S155D (10.88nH at 2.4 GHz), the source inductance Ls=SP014S300D (1.38nH at 2.4 GHz) and load inductance of L0=SP037S180D (4.13nH at 2.4 GHz). We use a load capacitance of CL=1pF. The LNA is tuned at 2.4 GHz at the input and resonates at the output at 2.4 GHz as $f = \frac{1}{2\pi\sqrt{4.13\times10^{-9}\times1\times10^{-12}}} \approx 2.4GHz$

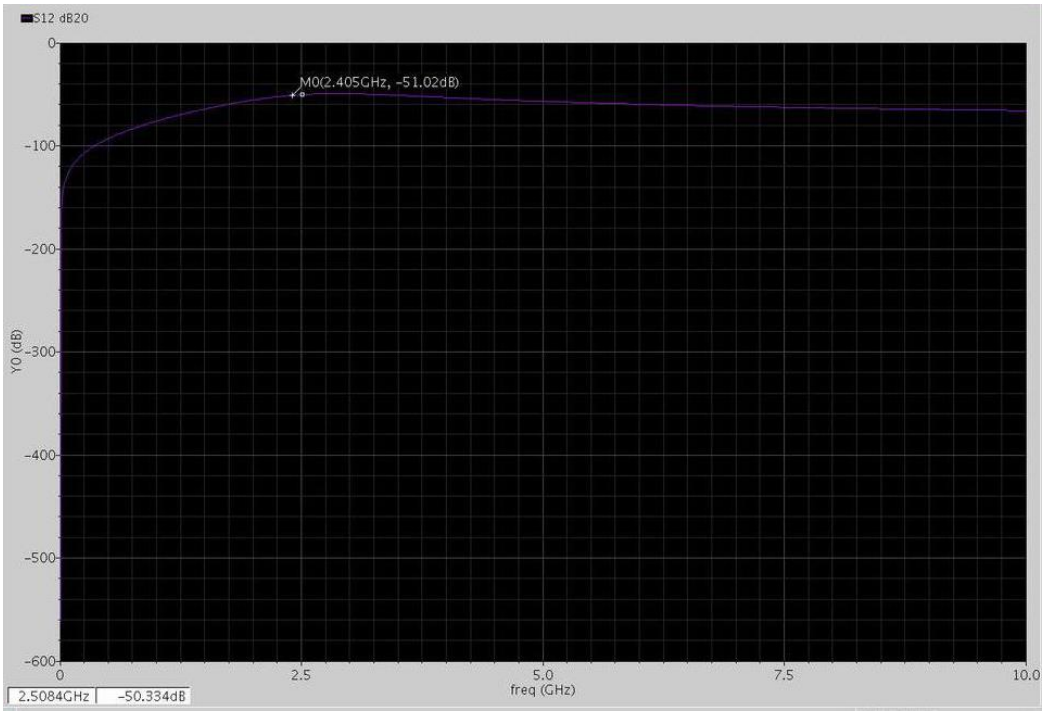
We use a power supply voltage of 3.3V. The bias voltage of the main transistor (T1) is 0.8V and bias voltage of cascode transistor (T2) is 1.1V. The widths of the transistors (T1 and T2) are kept at 200µm. The target is to obtain reasonable figures of merit thus we can validate the circuit as a test vehicle for the active inductors.

We use SpecreRF simulator to perform s-parameters analysis and characterize the circuit. Here are the plots obtained for the main figures of merit:

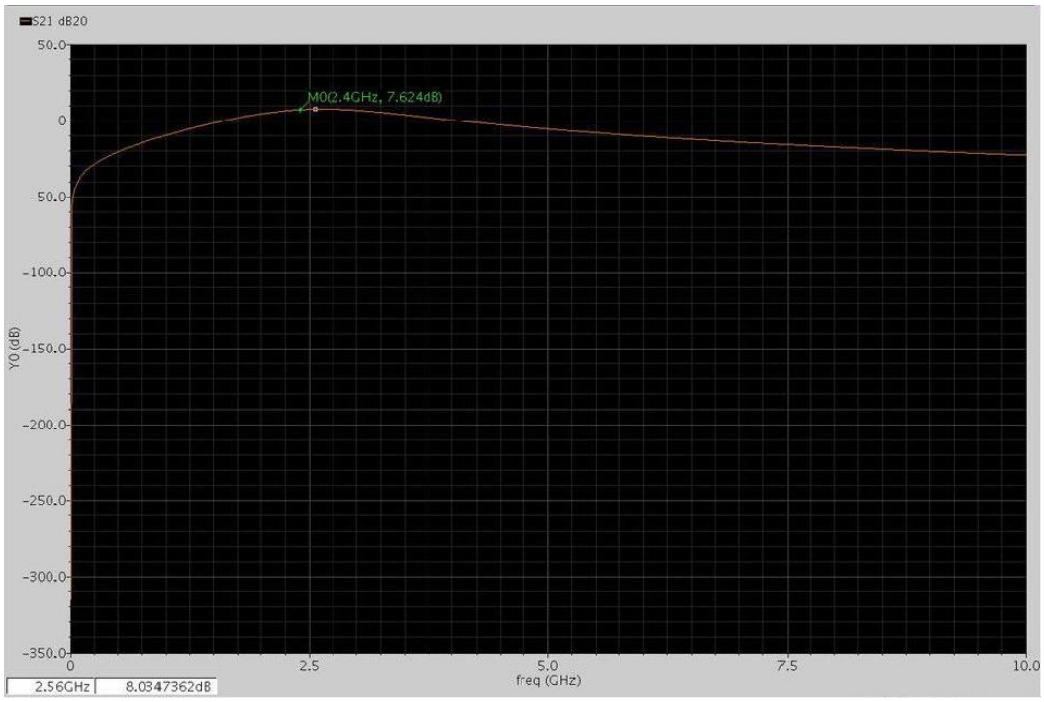
S11 = -12.48 dB at 2.4 GHz (good matching at the input)



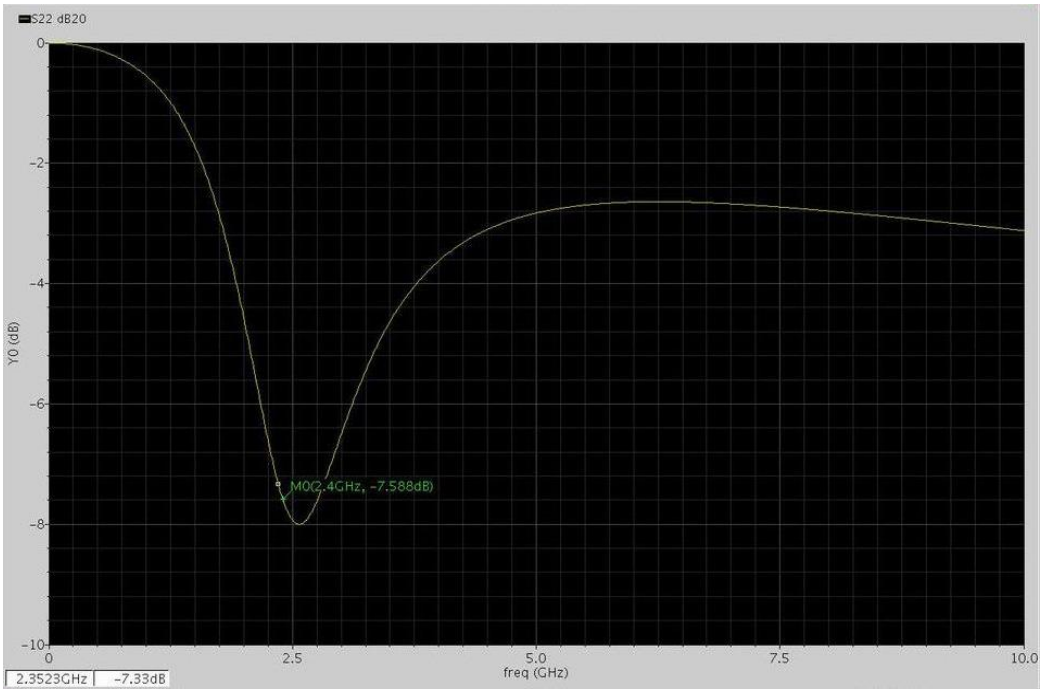
S12 = -51.02 dB at 2.4 GHz (very good isolation between the input and output)



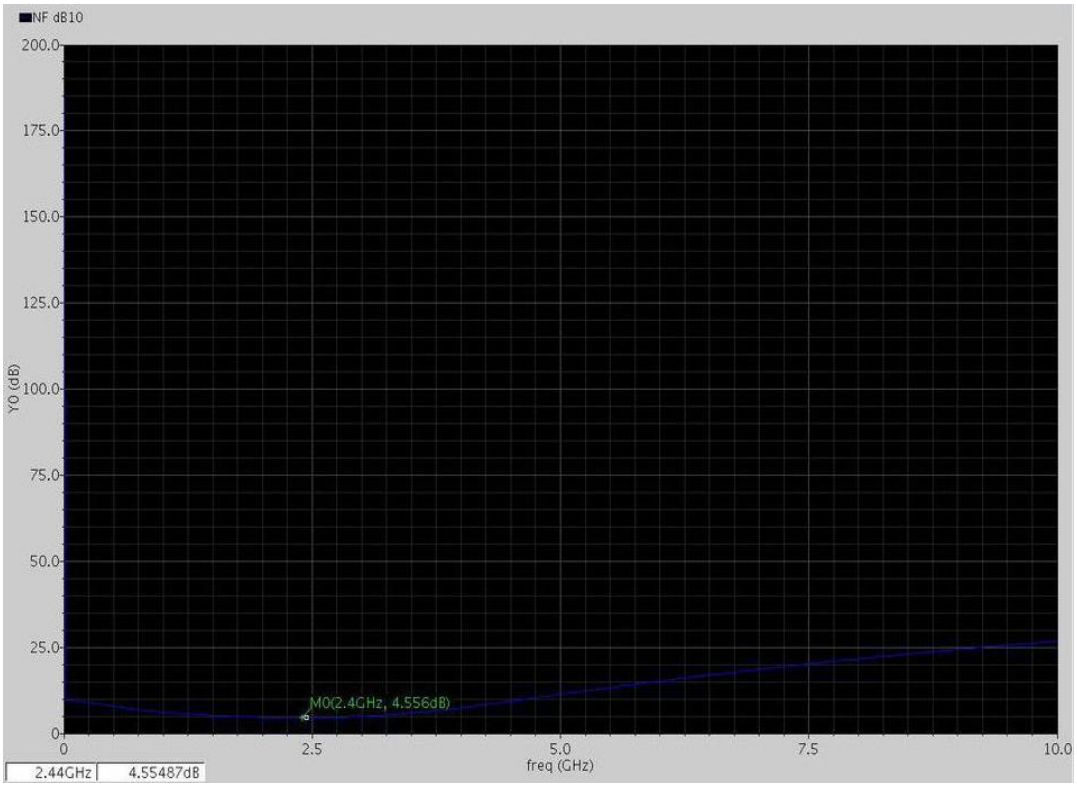
S21= 7.642 dB at 2.4 GHz (reasonable gain)



S22 = -7.588 dB at 2.4 GHz (reasonable resonance at the output)



NF = 4.556 dB at 2.4 GHz (good noise figure)



Linearity analysis:

We do a quasi-periodic steady state analysis (at 2.4 GHz) to find the IIP3 of the LNA (IIP3 characterizes the linearity of LNA).

Table 4.1:IIP3 of tuned LNA using spiral inductors

Extrapolation point(or power)(in dBm)	IIP3(in dBm)
-15	-6,16
-25	-8,51
-35	-9,07
-45	-8,99
-55	-9,13

We get IIP3 to a minimum of -9.13 dBm. This serves as a point where we can compare this with the LNA´s which use active inductors.

Conclusion:

As a summary, we get the following parameters at the frequency of interest (2.4 GHz).

S11 = -12.48 dB

S12 = -51.02 dB

S21 (gain) = 7.642 dB

S22 = -7.588 dB

NF = 4.556 dB

Minimum IIP3 = -9.13 dBm

The circuit gives a good matching at the input, good isolation, reasonable gain and resonance at the output, good noise figure and a good IIP3.

These values will be used for comparison to the performance of the active inductor used in LNA.

4.2)Tuned LNA using active inductor:

4.2.1)Using a basic active inductor

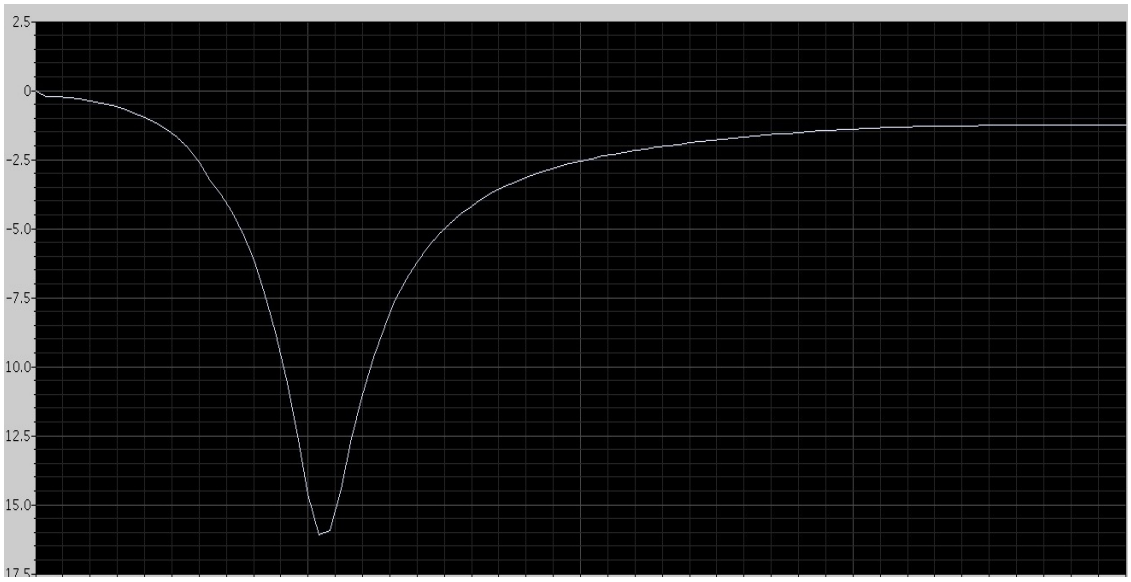
We will now replace one of the spiral inductors, i.e. that at the load with an active inductor having the same value of inductance as the spiral inductor at 2.4 GHz.

While using the active inductor along with the existing LNA, we have to omit the transistor M3 (which implemented the current J1) which biases the feedback transistor M2), as the DC current is already being supplied by the drain of the transistors which are a part of the amplifier.

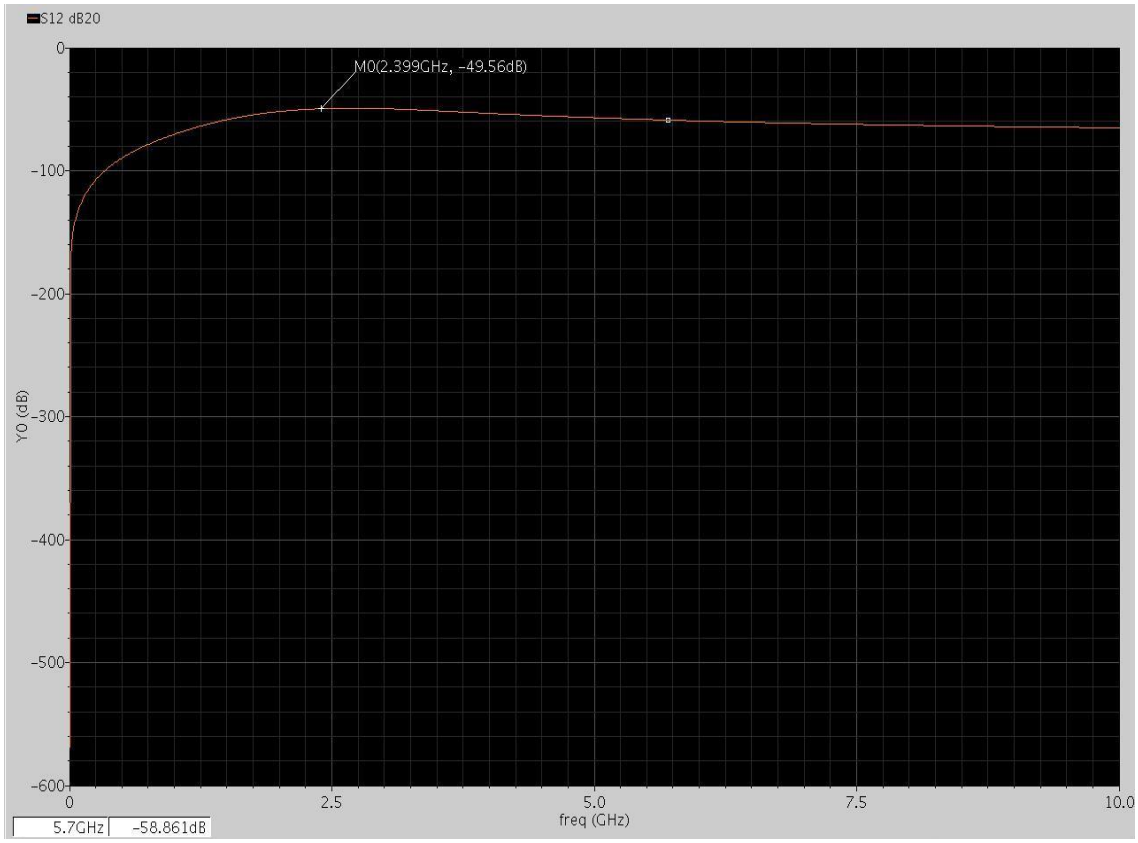
Keeping W1=W2=50um and W4=20um and bias voltage (Vb) = 2.25 V and a load capacitance of CL=1pF. The bias voltage biases the transistor (M4) which biases the main transistor (M1).

Fig. 4.5:Schematic: LNA using basic active inductor

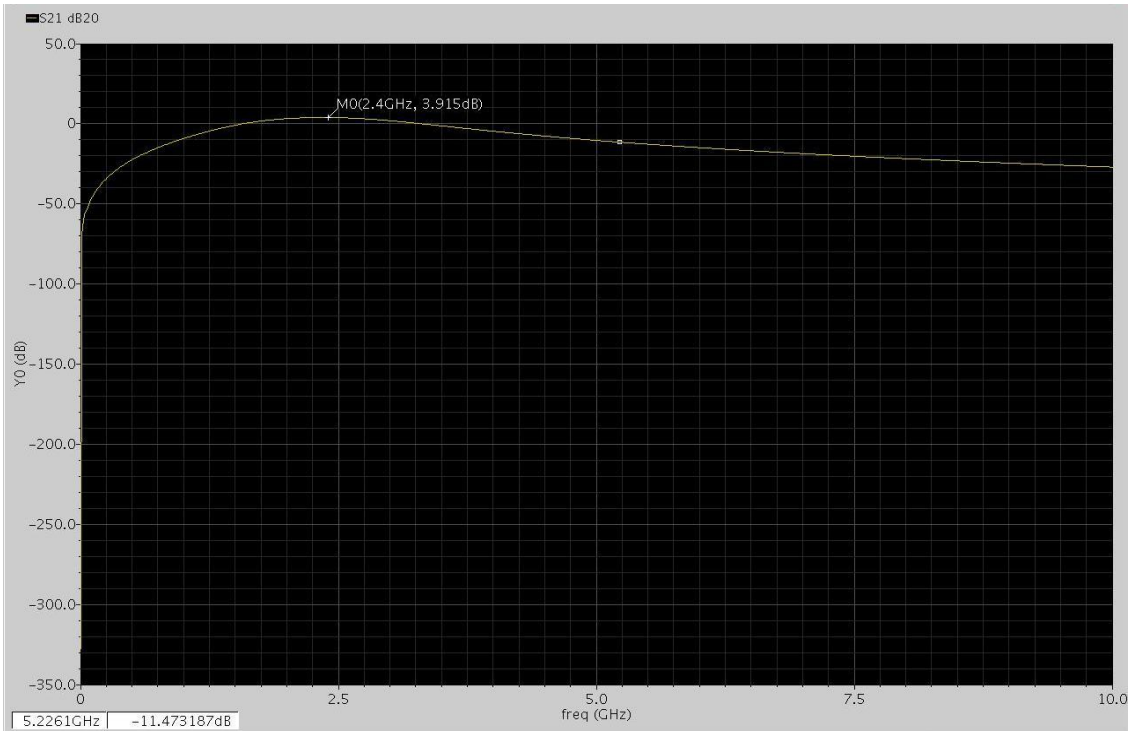
S11 = -12.48 dB at 2.4 GHz (good matching at input)



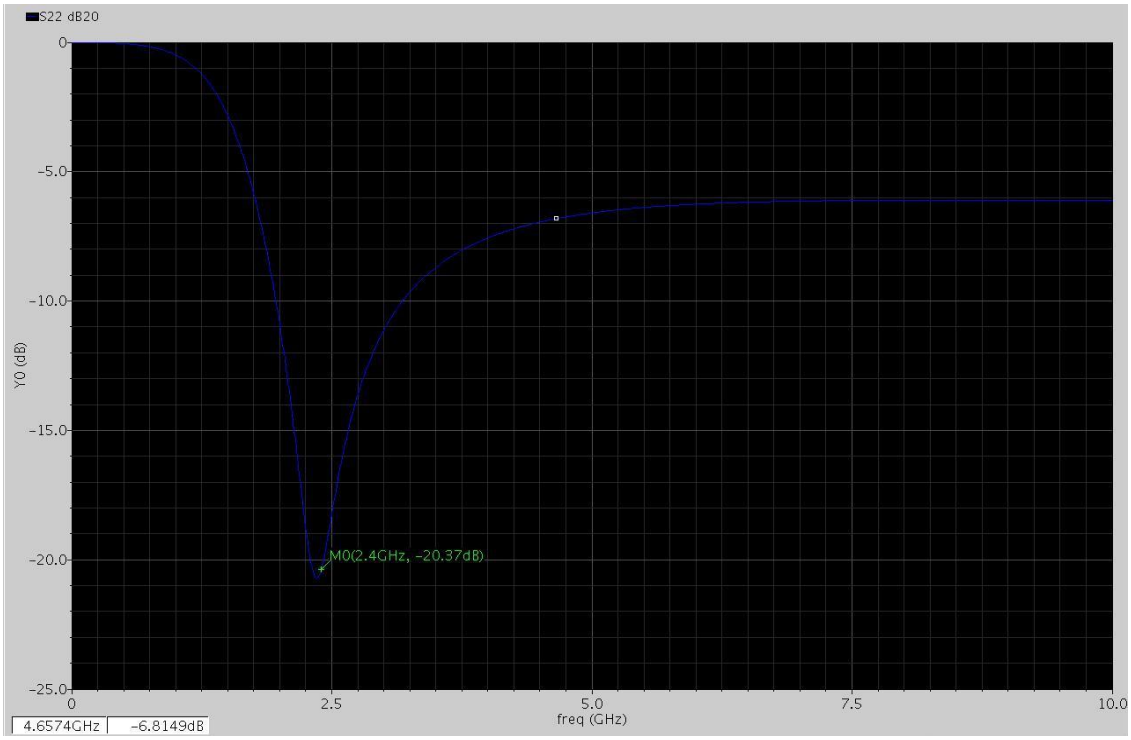
S12 = -49.56 dB at 2.4 GHz (good isolation between the input and output)



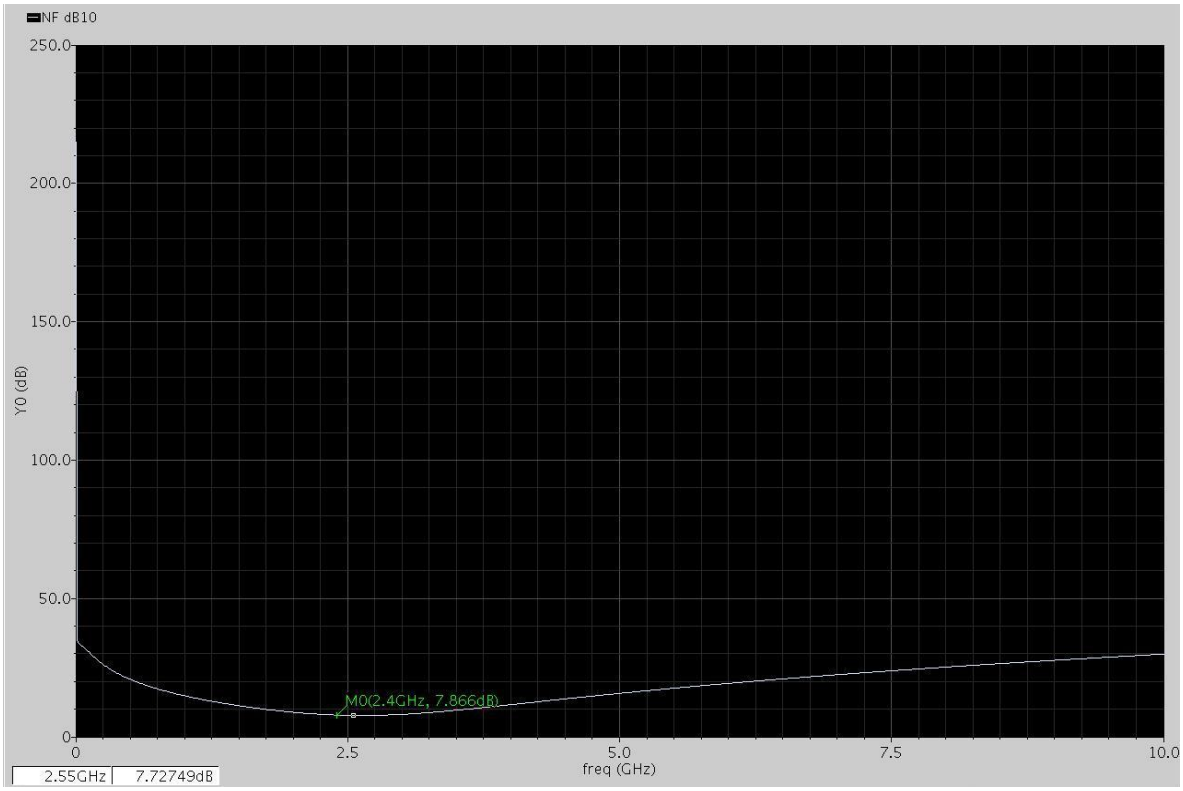
S21 = 3.915 dB at 2.4 GHz (low gain, will be improved later)



S22 = -20.37 dB at 2.4 GHz (good resonance at the output)



NF = 7.886 dB (high noise figure)



Linearity analysis:

Table 4.2:IIP3 of tuned LNA using basic active inductor

Extrapolation point(or power)(in dBm)	IIP3(in dBm)
-15	-6,49
-25	-9,78
-35	-10,44
-45	-9,78
-55	-14,93

We get IIP3 to a minimum of -14.93 dBm, which is lesser than the one using spiral inductors. Hence, there is more non-linearity than the one using spiral inductor.

Comparison:

At the frequency of 2.4 GHz, we get:

Table 4.3: comparison between spiral inductor LNA and basic active inductor LNA

Inductor	Spiral inductor	Basic Active Inducto
S11(input matching)(indB)	-12,48	-12,48
S12(isolation)(in dB)	-51,02	-49,56
S21(gain)(in dB)	7,642	3.915
S22(output resonance)(in dB)	-7,588	-20,37
NF(noise figure)(in dB)	4,556	7.886
Min. IIP3(in dBm)	-9,13	-14,93

Frequency tuning:

By changing the bias voltage, we change the value of inductance and hence this changes the frequency of operation as the frequency depends on inductance and capacitance value. For the following bias voltages, we get the following frequency of operation. In this case the bias voltage is the bias voltage of transistor (M4) which biases the transistor (M1).As the active inductor is used only at the output stage, there is a mismatch between the input and output as the input is matched to a frequency which is different from that of the output. Hence in this case we will focus on the gain at the frequency of resonance and not on the gain at input matching frequency.

Table 4.4: Frequency tuning of tuned LNA using basic active inductor

Vb	f(resonance)	S22(output matching)(in dB)	S21(gain)(in dB)
2	2.94 GHz	-28,52	3,264
1,75	3.27 GHz	-35,23	2,94
1,5	3.49 GHz	-35,86	1,87

As seen in this case, the frequency tuning goes on degrading as the voltage gain cannot be the same for every value of inductance. Changing the value of bias voltage changes the value of inductance and invariably changes the value of the resonant frequency.

Conclusion:

With a good matching at both input and output along with good isolation, this topology is good. But the gain is very low here and also the noise figure is higher, due to a low quality factor of the active inductor. This topology also gives a degraded IIP3 (more non-linearity) compared to the spiral inductors.

4.2.2)Using the resistive – Feedback Active Inductor

Here, we use the resistive feedback topology. This topology gave us a better quality factor and hence we hope to characterize this LNA better than the one with active inductor. The widths of transistor used here is the same as those used in the basic active inductor.The schematic is as follows:

Fig. 4.6: Schematic: Tuned LNA using resistive feedback active inductor

For different values of resistances we get different quality factors and hence we do the same analysis here. For different values of feedback resistance used here, we check the parameters of the LNA at 2.4 GHz. This is as shown in Table 3.5:

Table 4.5: observations of tuned LNA using resistive feedback active inductor

R	100Ω	500Ω	1kΩ	2kΩ
S11(in dB)	-12,48	-12,48	-12,48	-12,48
S12(in dB)	-50,52	-50,79	-51,45	-52,23
S21(in dB)	5,036	6,092	9,768	11,33
S22(in dB)	-18,67	-20,29	-21,45	-21,79
NF(in dB)	7,74	7,82	7,88	7,89
Min. IIP3(in dBm)	-6,63	-11,06	-11,84	-11,47

Conclusion:

For these values of resistance, we get a good gain along with good matching at the output. This is due to the better quality factor of this active inductor. With similar noise figure as that of basic active inductor, we get a good gain in this topology. Also we get a better IIP3 than the one using basic active inductor (Min. of -11,47 compared to -14,93 of that of the basic active inductor).

4.2.3)Using a Weng – Kuo cascode active inductor

Here, we use a weng – kuo cascode active inductor, which has a very good quality factor and also doesn't have a noisy element (for example resistor – in the resistive feedback active inductor). The width of the cascode transistor and additional current source transistor is 50µm and 10µm, respectively and widths of other transistors are the same as ones used in basic active inductor. The schematic is as follows:

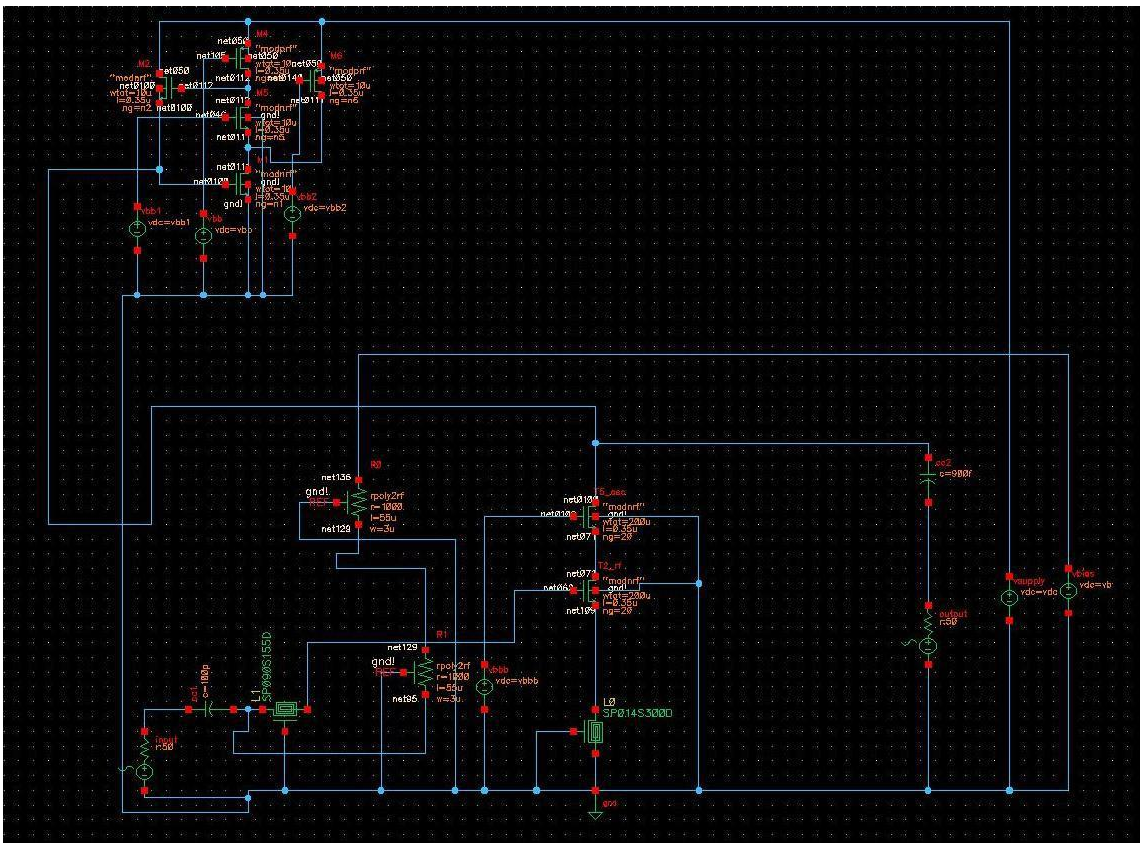
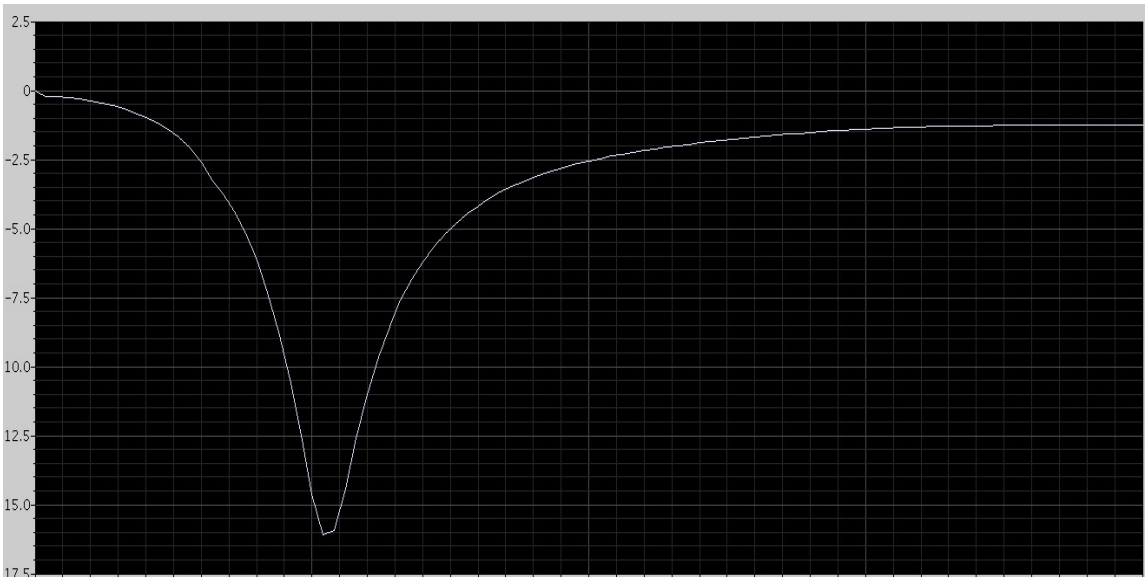
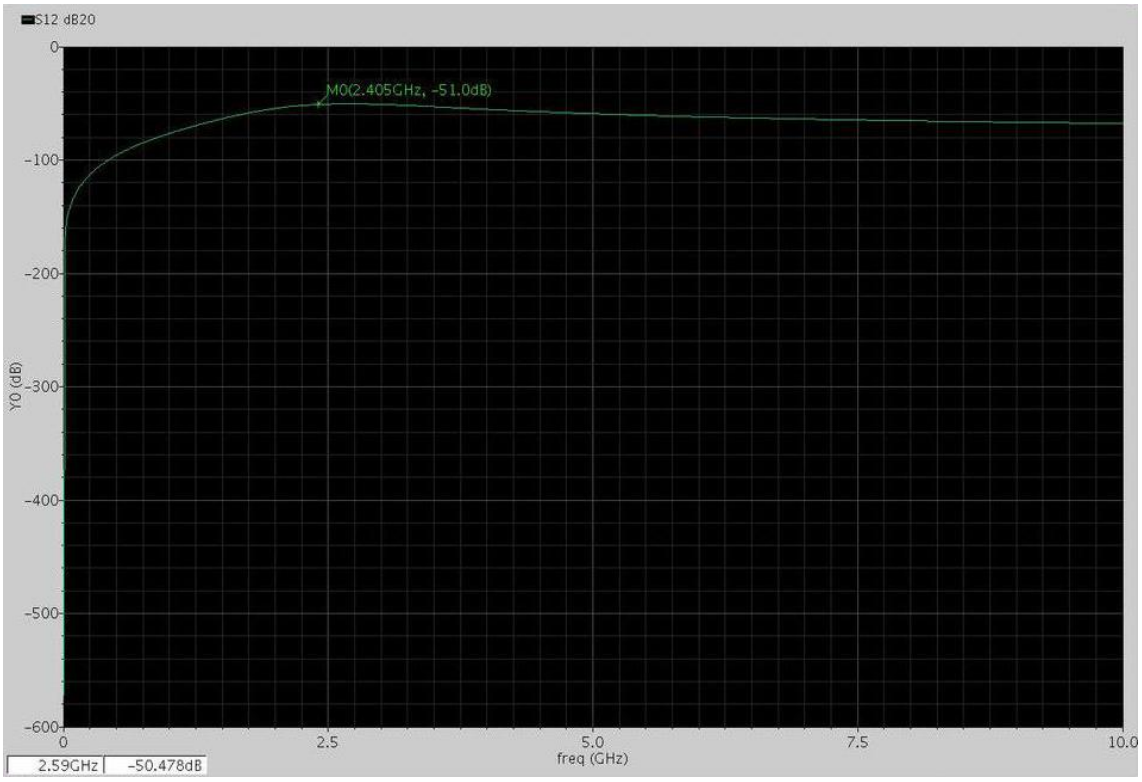


Fig. 4.7:Schematic: Tuned LNA using Weng-Kuo cascode active inductor

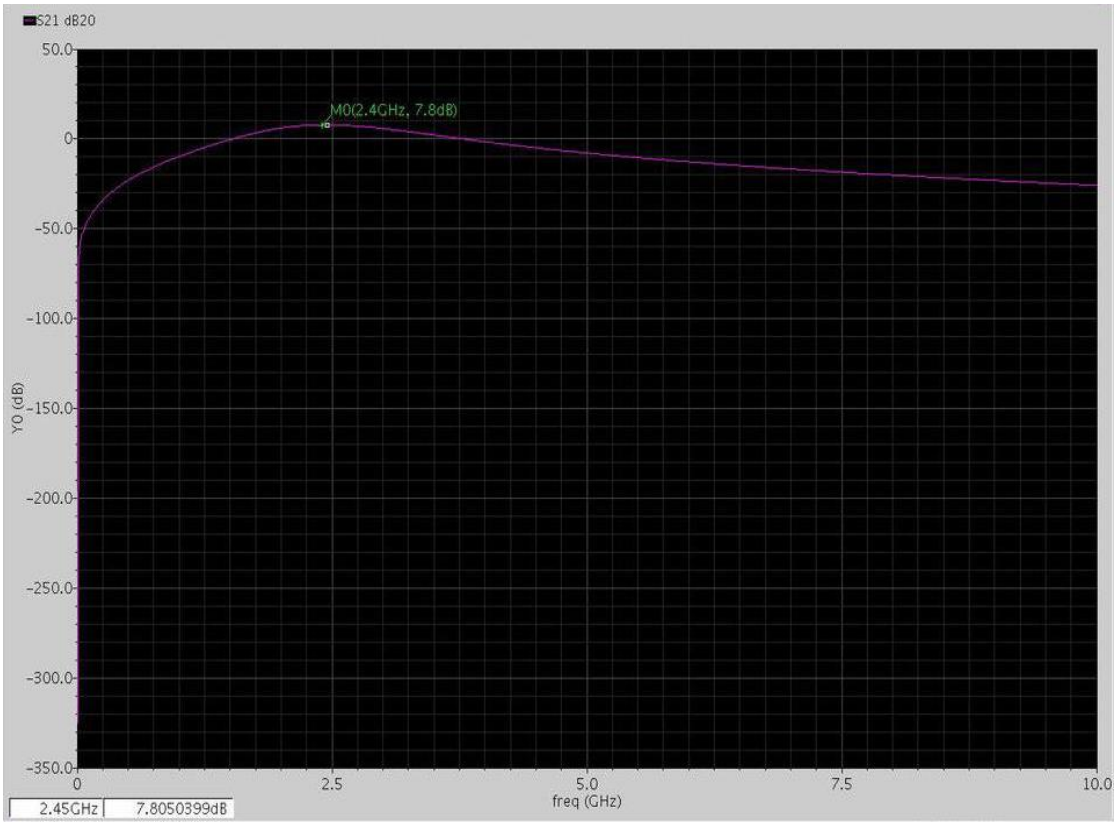
S11 = -12.48 dB at 2.4 GHz (good matching at the input)



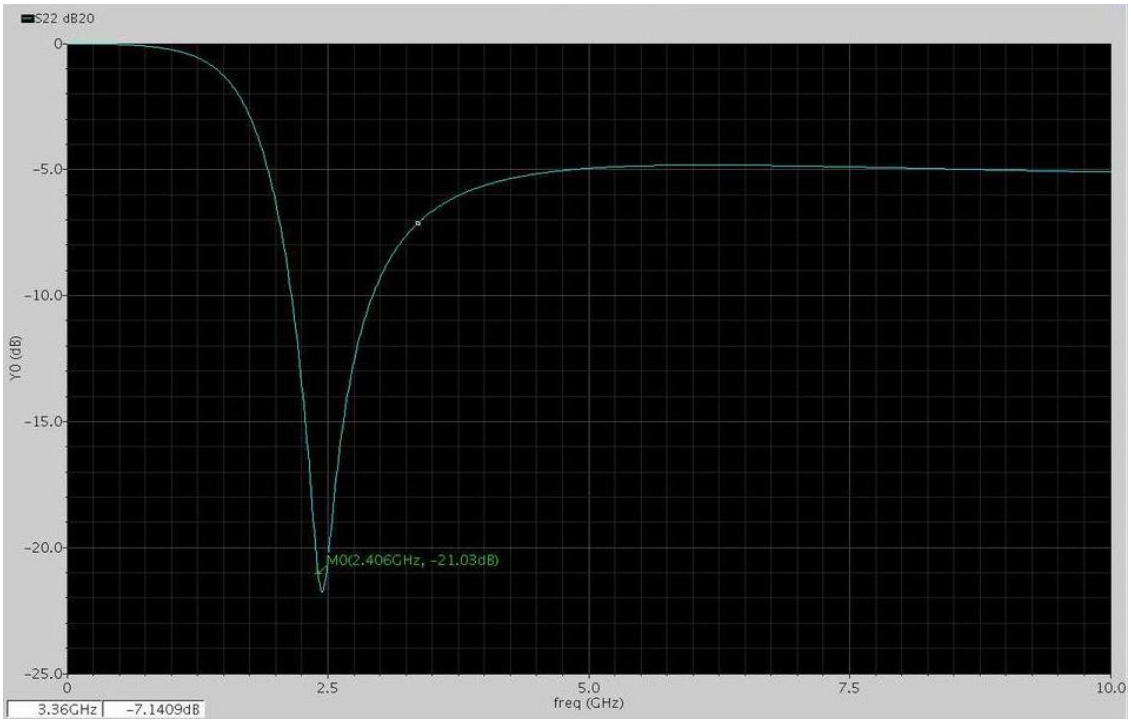
S12 = -51.01 dB at 2.4 GHz (good isolation between the input and output)



S21 (gain) = 7.8 dB at 2.4 GHz (reasonable gain and better compared to before)



S22 = -21.03 dB at 2.4 GHz (good resonance at the output)



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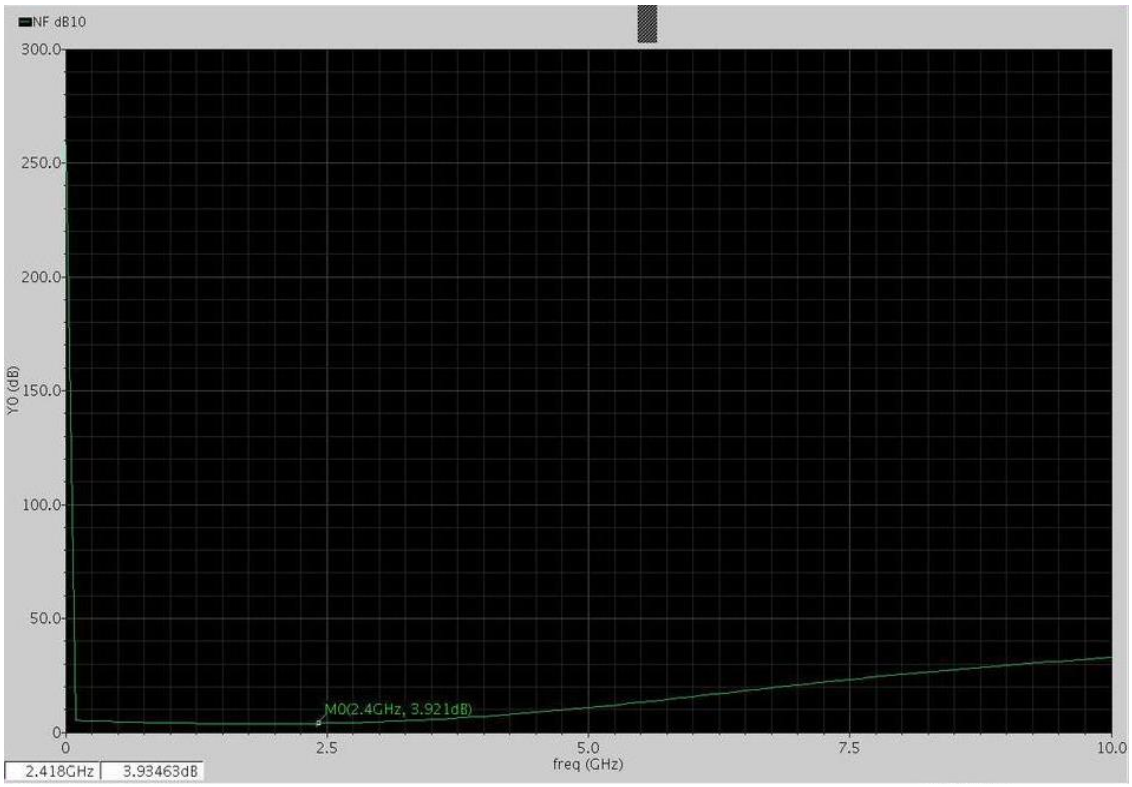
NF = 3.921 dB at 2.4 GHz (very good noise figure, the best so far)



Linearity:

The IIP3 found at frequency of 2.4 GHz is:

Table 4.6: IIP3 of tuned LNA using weng-kuo cascode active inductor

Extrapolation point(or power)(in dBm)	IIP3(in dBm)
-15	-6,63
-25	-11,01
-35	-11,85
-45	-11,47
-55	-14,93

Comparison:

Table 4.7: comparison between the inductor topologies used in the LNA at 2.4 GHz

Inductor	Spiral inductor	Basic Active Inductor	Weng-Kuo cascode
S11(input matching)(indB)	-12,48	-12,48	-12,48
S12(isolation)(in dB)	-51,02	-49,56	-51,01
S21(gain)(in dB)	7,642	3.915	7,8
S22(output resonance)(in dB)	-7,588	-20,37	-21,03
NF(noise figure)(in dB)	4,556	7.886	3,92
Min. IIP3(in dBm)	-9,13	-14,93	-14,93

Frequency Tuning

i)Changing the bias voltage of the cascode transistor (M3)

Changing the bias voltage changes the frequency of operation. As said before, the gain and output matching is seen at the frequency of resonance at the output.

Table 4.8: Frequency tuning - 1

Vbias(M3) (in V)	1	1.25	1.5	1.6
f(self resonant)(in GHz)	1.651	2.308	2.402	2.436
S21(gain)(in dB)	5.171	7.694	7.802	7.807
S22(output matching)(in dB)	-9.379	-29,58	-21,03	-21,72
Vbias(M3) (in V)	1.75	1.9	2	
f(self resonant)(in GHz)	2.501	2.513	2.533	
S21(gain)(in dB)	7.815	7.807	7.779	
S22(output matching)(in dB)	-20,07	-19,81	-19,61	

For the above bias voltages we get the respective resonant frequency, gain and matching at the output (input matching and isolation do not change much in this case).

The bias voltage of the cascode transistor can be used to control the inductance and hence the self – resonant frequency. The gain does not change much here.

ii)Changing the bias voltage of transistor (M4)

Also in the case of basic active inductor, we had done frequency tuning and seen that it degrades over the bias voltage range. Here we get the following observations at the frequency of resonance:

Table 4.9: Frequency tuning - 2

vbias(M4) (in V)	1	1.25	1.5
f(self resonant)(in GHz)	2.521	2.483	2.401
S21(gain)(in dB)	4.896	5.694	6.297
S22(output matching)(in dB)	-23,681	-34,47	-21,46
vbias(M4) (in V)	1.75	2	2.25
f(self resonant)(in GHz)	2.352	2.185	2.012
S21(gain)(in dB)	6.308	7.778	9.555
S22(output matching)(in dB)	-17,18	-12,93	-10,75

The frequency tuning done here is better than the basic active inductor in terms of getting a good gain and also a good output matching.

Conclusion:

For different values of bias voltage, we find that this topology gives a very good gain and also a very good noise figure, also compared to that of spiral inductors. We also get a good frequency tuning as the gain is high in spite of having a mismatch between the input and the output. The IIP3 of the amplifier is slightly degraded than resistive feedback active inductor.

4.2.4) Using a regulated cascode active inductor

A regulated cascode active inductor is used here and due to its good quality factor we can expect to get good characteristics of LNA.

The schematic is given as follows:

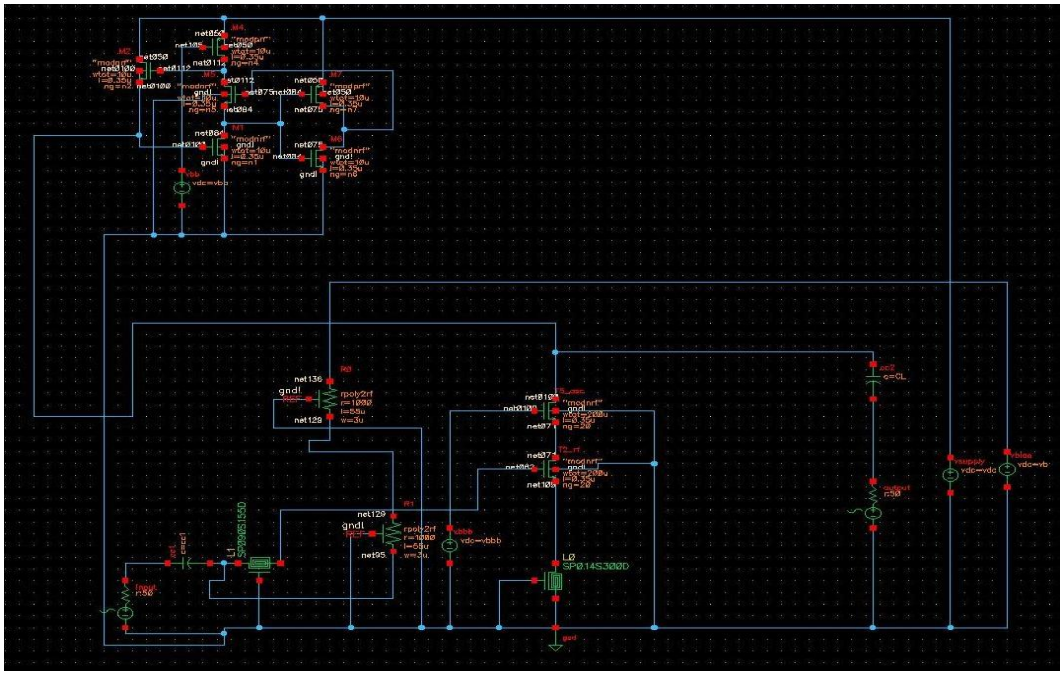
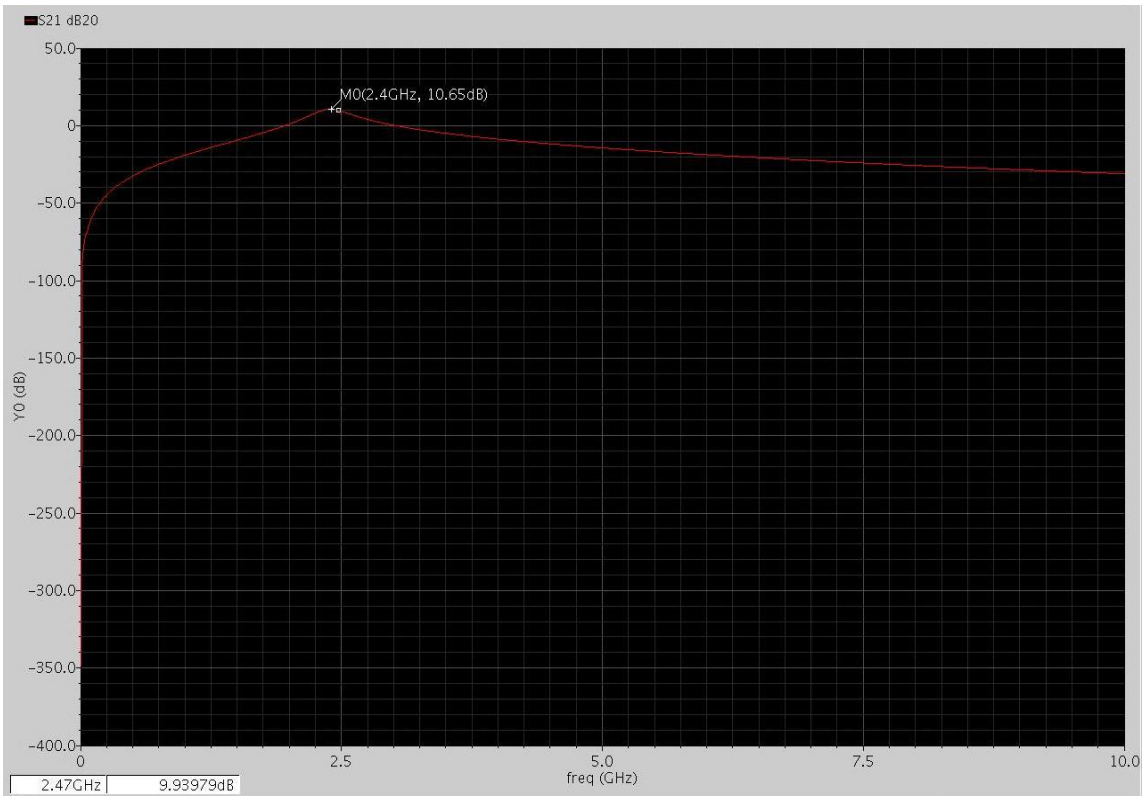


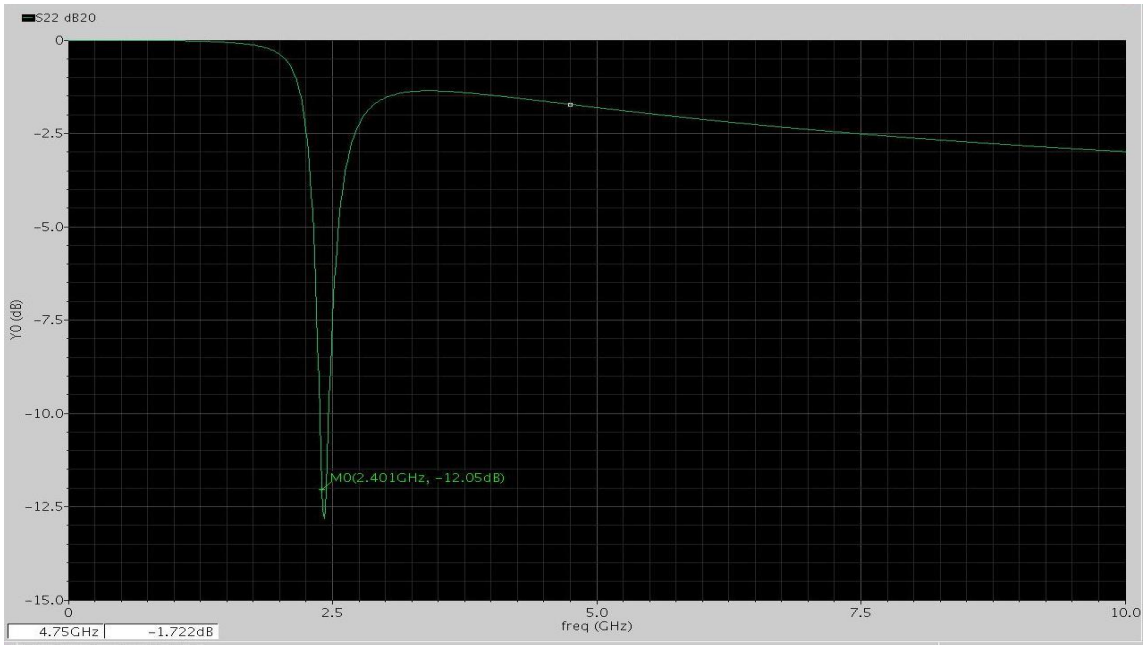
Fig. 4.8: Schematic: Tuned LNA using a regulated cascode active inductor

While using the regulated cascode, we use W5 = 100µm (width of cascode transistor) and W6=W7=30µm (width of the transistors used to make the inverter). Width of other transistors is the same as used in basic active inductor. With the same S11 (input matching) we have:

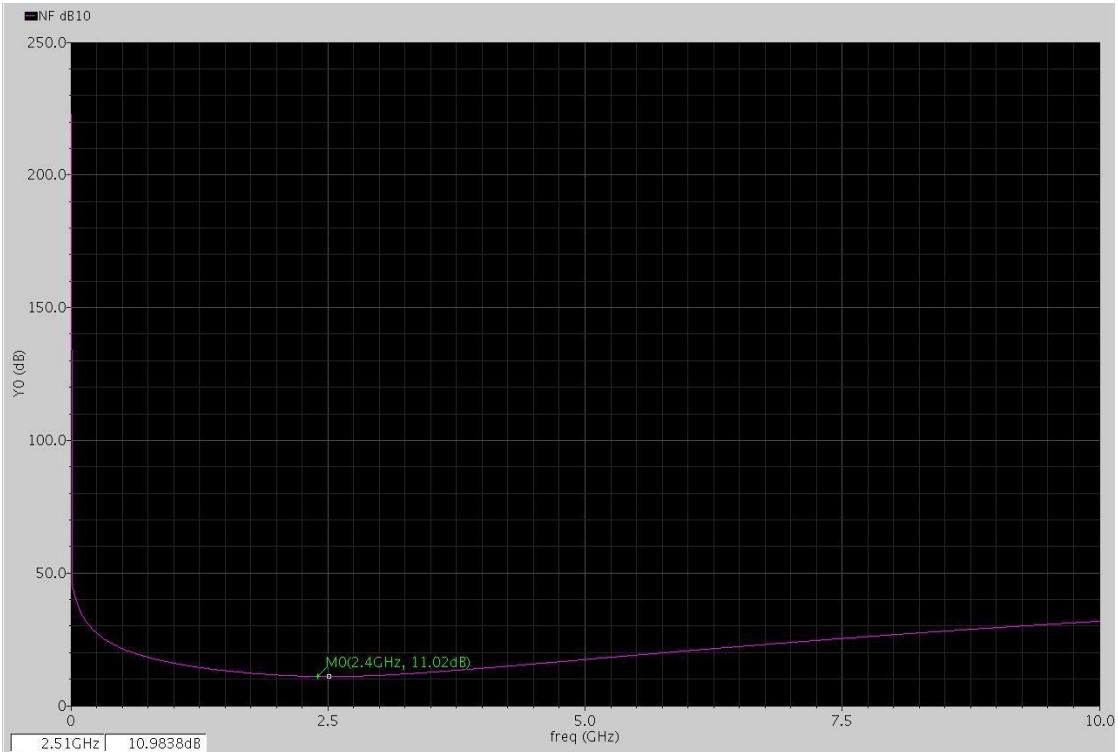
S21 = 10.65 dB at 2.4 GHz (good gain, the best so far)



S22 = -12.05 dB (good resonance at the output)



NF= 11.02 dB (very low noise figure, the worst so far)



Linearity:

Table 4.10: IIP3 of tuned LNA using regulated cascode active inductor

Extrapolation point(or power)(in dBm)	IIP3(in dBm)
-15	0,269
-25	-7,17
-35	-5,57
-45	-12,13
-55	-14,93

Frequency tuning:

Now, we change the bias voltage of transistor (M4) which biases the main transistor (M1). We get the following observations at the frequency of resonance:

Table 4.11:Frequency tuning of tuned LNA using regulated cascode active inductor

vbias(in V)	1,5	1,75	2	2,25	2,5
f(self - resonant)(in GHz)	3.796	3.525	3.106	2.403	1.331
S21(in dB)	2.649	4.971	8.207	10.852	2.894
S22(in dB)	-10,71	-8,294	-6,292	-12,05	-3,209
NF(in dB)	14.781	13.793	12.344	11.022	11.856

Conclusion:

This topology gives a very good gain along with good frequency tuning. But the noise figure is very high.

4.3)Conclusion on tuned narrowband LNA:

We get a very good input matching and isolation in all the cases (both spiral and active inductors). The change has been in the gain, output matching, noise figure and linearity. The following lists these parameters at the frequency of 2.4GHz.

Table 3.12: Final conclusion on tuned LNA

LNA type	Max. Gain(in dB)	Min. N.F(in dB)	Min. IIP3(in dBm)
spiral inductor	7.64	4.56	-9,13
basic active inductor	3.92	7.89	-14,43
resistive feedback active inductor	11.33	7.74	-11,84
Weng - Kuo cascode active inductor	9.55	3.92	-14,93
Regulated cascode active inductor	10.82	11.02	-14,93

From the above table we see that the Weng – Kuo cascode is the best active inductor as it gives a better performance also than the spiral inductors. It gives a very good noise figure and a good enough gain with a compensation of linearity.

The resistive feedback LNA also has good gain, but it has a higher noise figure compared to the Weng – Kuo cascode. The reason for the noise figure not having much change from the basic active inductor(inspite of having a noisy element such as the resistor) is the fact that parallel resistance which has contributed to higher quality factor compensates for the effect of the noisy resistor.

Also we see that the noise figure of the regulated cascode active inductor is very high and has a high IIP3 at higher input power levels.

5)Wideband Shunt Peaked LNA

This chapter consists of a preliminary study for the design of wideband LNA. The wideband amplifier used here is a basic common source amplifier cascaded with a common drain amplifier. The first stage is the common-source stage which provides a good gain and the next stage, which is the common drain stage, provides a low output resistance, helpful for getting a higher bandwidth when the load is a capacitor. This circuit has a pole at a frequency:

$$f = \frac{1}{2\pi RC}$$

We see that the bandwidth is limited by the output resistance and output capacitance. The low – drain amplifier stage at the output of the amplifier is used to get a low resistance. This increases the bandwidth upto a certain extent.

A technique called as shunt peaking is used to increase the bandwidth, more than what is available. This can be done by introducing a zero (instead of a pole) by introducing an inductor in series with the resistance at the drain of first stage. This inductor introduces peaking in the output of the amplifier and increases the bandwidth. The gain is increased by the peaking factor of

$$m = \frac{L}{R^2 C}$$

Peaking factor of 1.414 gives a flattest bandwidth and hence gives the most maximum bandwidth extension.

Increasing the peaking factor above this value increases the peaking (i.e. the gain of the amplifier at certain frequencies). So, we can also increase the gain of the amplifier.

5.1)Using spiral inductors

This section focuses on basic wideband amplifier and techniques used to increase the gain and bandwidth of the amplifier.

First we design a basic two-stage amplifier for a load of 1pF. Using the width of all transistors to be 200µm, we get a very high g_m for the first stage to get a high gain and a high g_m in the second stage to get a lower output resistance. We use a bias voltage of 0.786 V for the first stage. We use a resistance of 100Ω at the drain of the first stage. Also the power supply voltage used here is 3.3V.

The schematic is as follows:

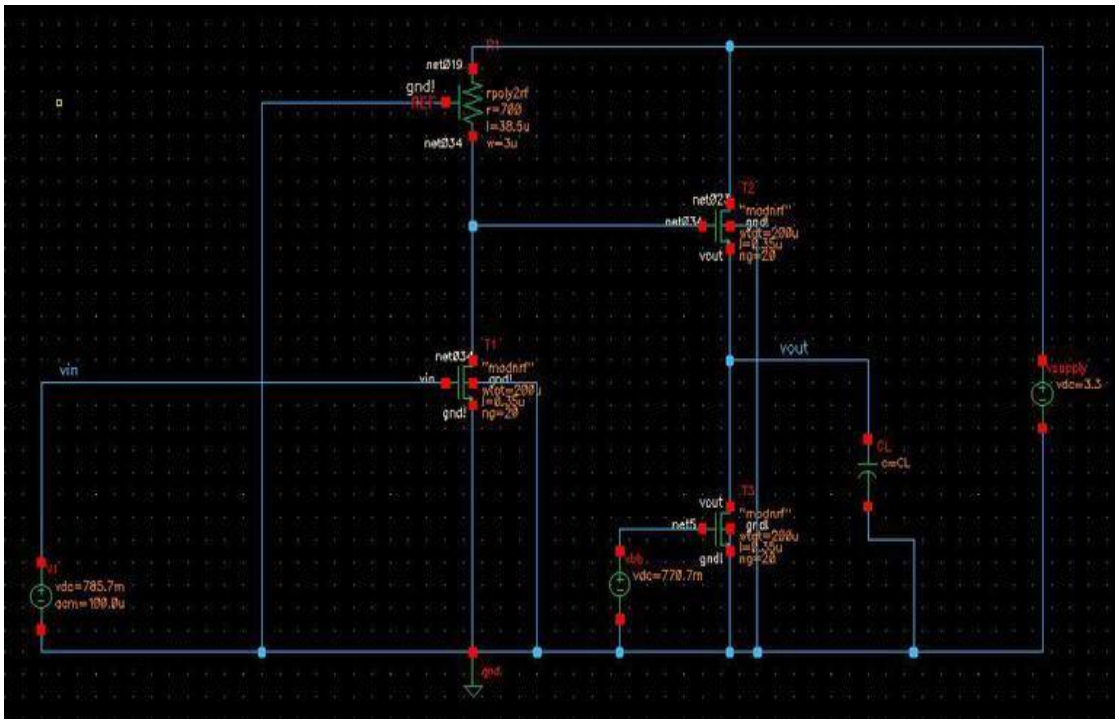
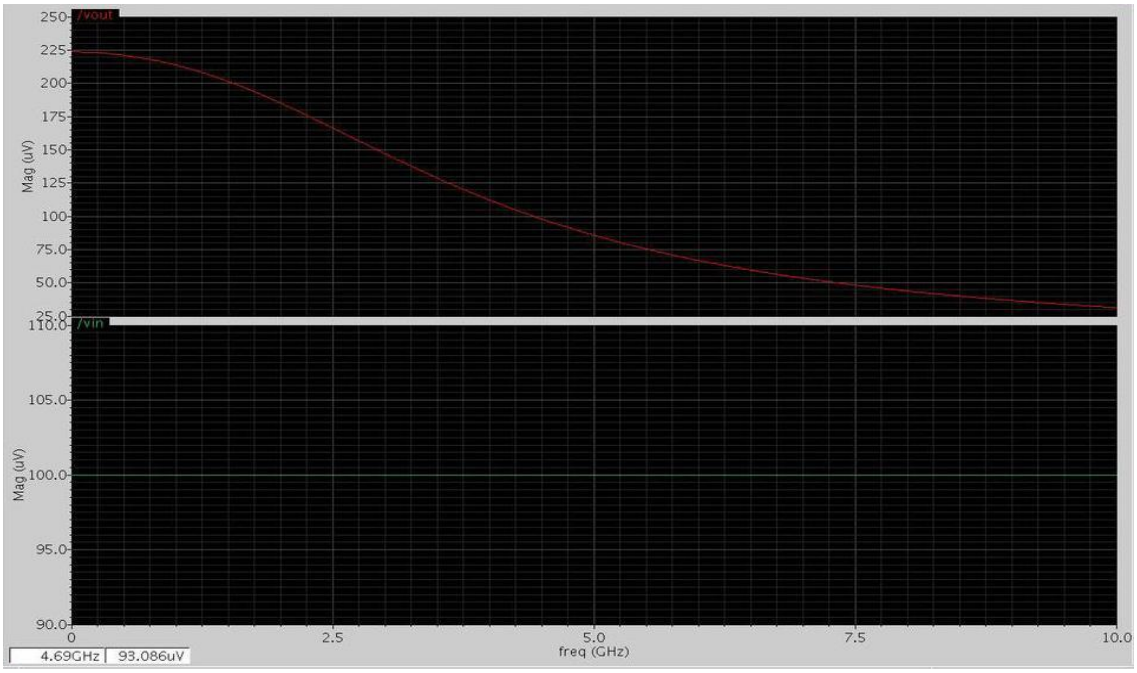


Fig. 5.1: Wideband LNA using spiral inductors



Using R=100Ω drain resistance in the first stage we get

The output we get is:

Vin = 100µV, Vout = 223.52µV

Gain = 2.24 = 3.493 dB

Bandwidth = 2.7 GHz

In the next step, we use the shunt – peak technique to increase both – bandwidth as well as gain.

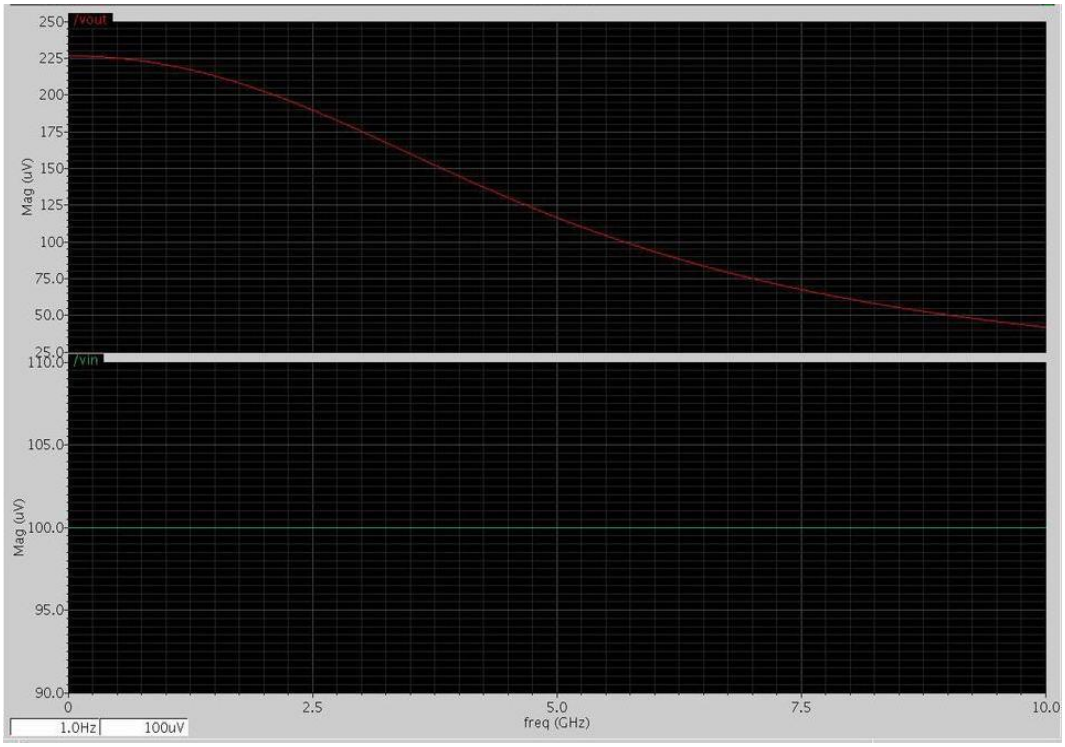
Output resistance is $R_{out} \approx \frac{1}{g_m} = \frac{1}{23\times10^{-3}} = 43.47\Omega$, where g_m is the transconductance of the transistor at the output stage of the wideband amplifier.

For a load capacitance of CL=1pF, we get

$m = \frac{L}{R^2 C} \Rightarrow m = \frac{L}{1.89}$, where L is the inductance used for shunt peaking in nH.

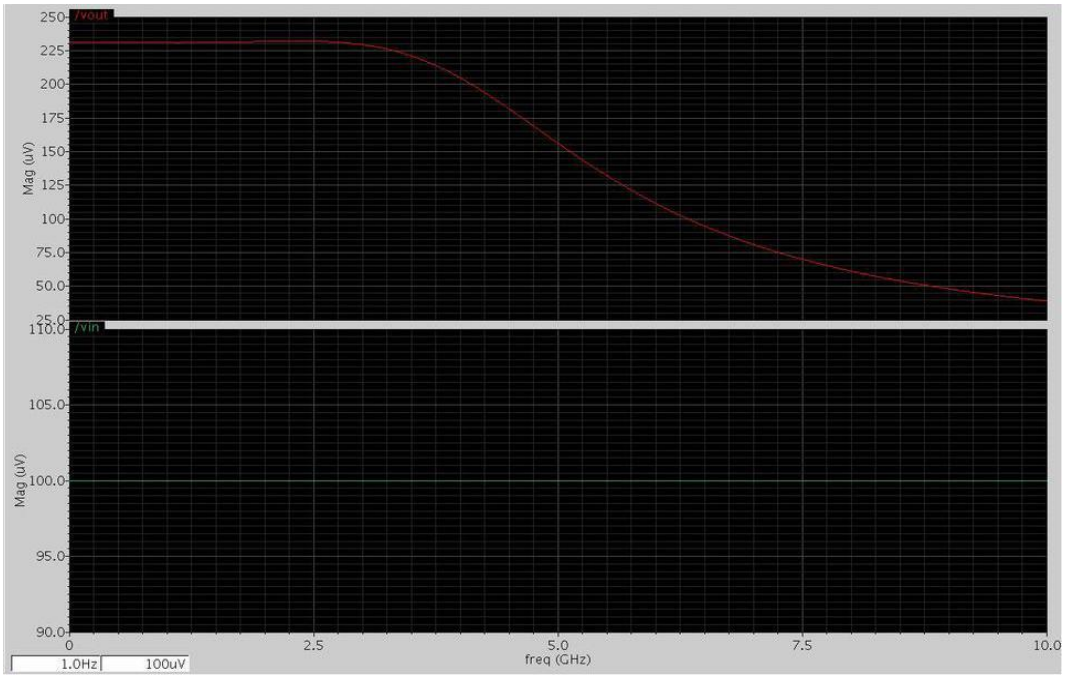
The inductances used and the observations made are:

i) SP015S250T – 1.5nH,m=0.794



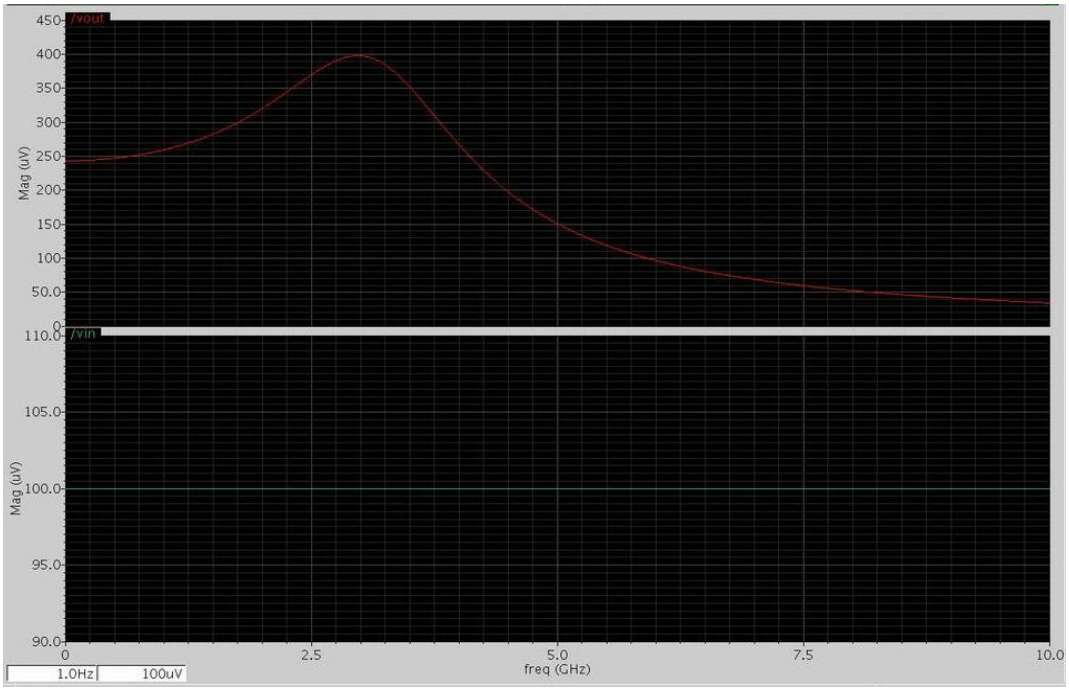
We don´t get peaking here but a good bandwidth extension.

ii) SP031S250T – 3.2nH,m=1.693



We get a good flat response for a good range of frequency and also a good bandwidth extension. With m near to the value of 1.414, we get the best bandwidth extension here.

iii) SP060S300T – 6.69nH,m=3.54



We get a good amount of peaking here at the expense of bandwidth which has reduced from the one seen in the previous example.

Results:

Table 5.1:Results of wideband LNA

Vin	100µV	
L(inductance)	no inductance	SP015S250T(1.5nH)
Vout(in µV)	223.52	226.62
Bandwidth(in GHz)	2.7	3.49
Max. Vout	223.52µV at dc	226.62µV at dc
L(inductance)	SP031S250T(3.2nH)	SP060S300T(6.69nH)
Vout(in µV)	231.29	243.22
Bandwidth(in GHz)	4.85	4.75
Max. Vout	231.29µV at dc	397.57µV at 2.94 GHz

5.2)Using active inductors

We now change the inductance of the active inductor, make observations and give conclusions later.

5.2.1)Using basic active inductor

We use the same topology of the active inductor as used in the tuned LNA. The schematic is as follows:

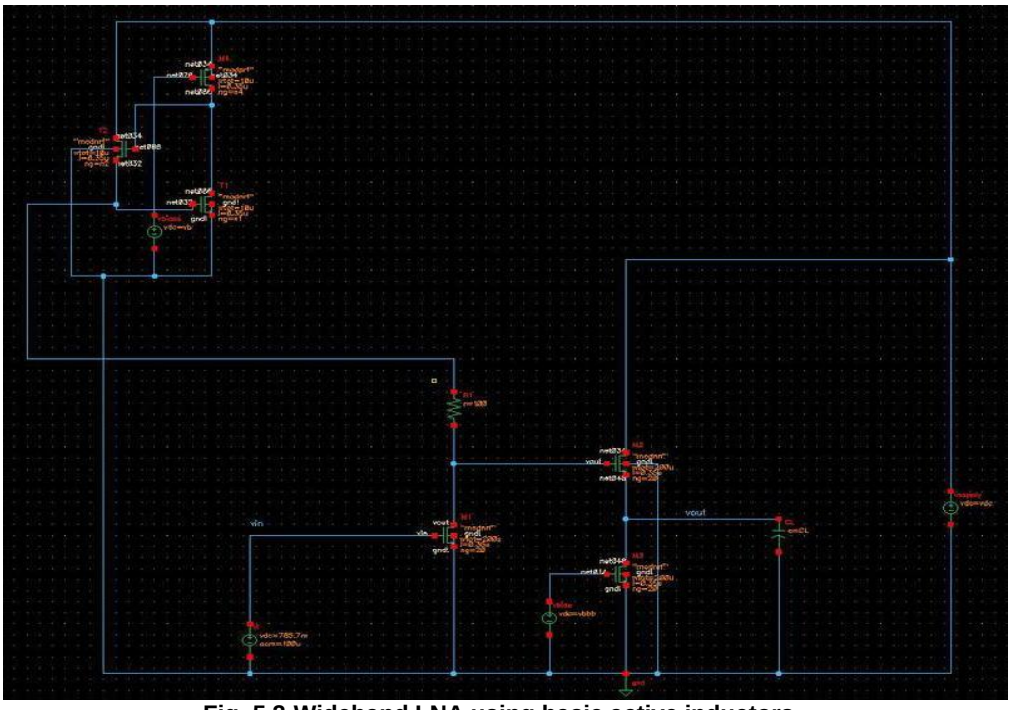


Fig. 5.2:Wideband LNA using basic active inductors

Now, we change the bias voltage to change the value of inductance and invariably the peaking and bandwidth. We get the following observations:

Table 5.2:Results of wideband LNA using basic active inductor

Vin	100µV	
vbias(in V)	1	1,25
L(inductance)	4.15nH	4.33nH
Vout(in µV)	232.14	222.02
Bandwidth(in GHz)	5.38	5.69
Max. Vout	234.56µV at 1.94GHz	231.09µV at 2GHz

Vin	100µV	
vbias(in V)	1,5	1,75
L(inductance)	4.42nH	4.49nH
Vout(in µV)	214.65	208.26
Bandwidth(in GHz)	5.87	6.05
Max. Vout	228.5µV at 2.24GHz	228.66µV at 2.31GHz
Vin	100µV	
vbias(in V)	2	2,25
L(inductance)	5.12nH	5.27nH
Vout(in µV)	201.83	194.69
Bandwidth(in GHz)	6.17	6.13
Max. Vout	232.71µV at 2.45 GHz	247.04µV at 2.22 GHz

5.2.2)Using resistive feedback active inductor

We use the resistive feedback active inductor here.

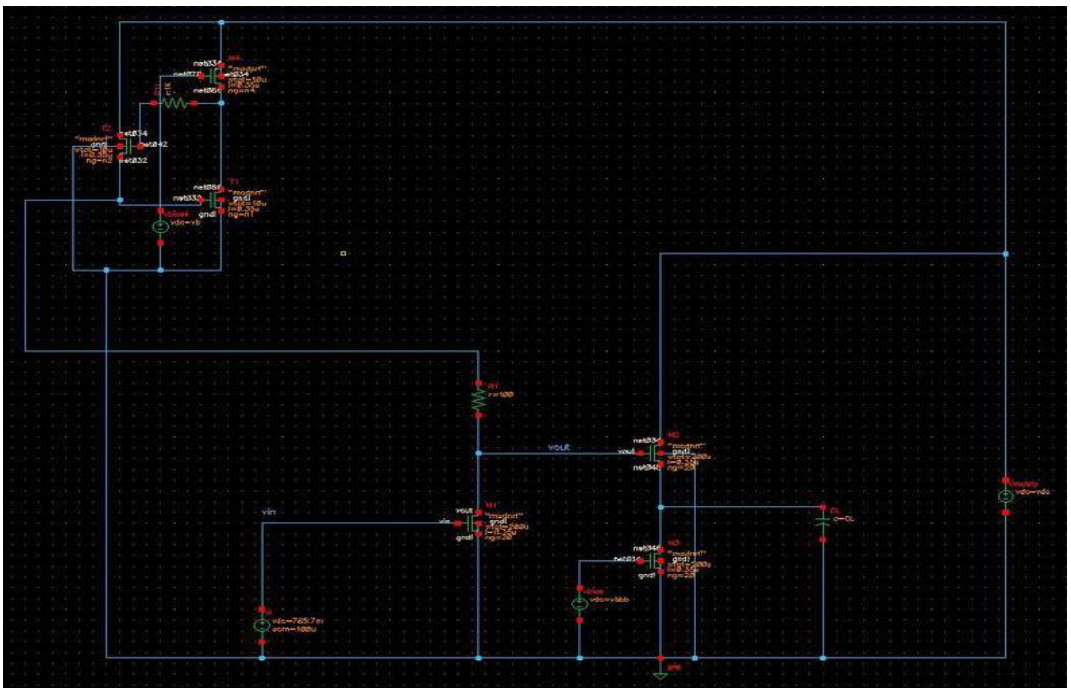


Fig. 5.3:Wideband LNA using resistive feedback active inductors

Now, we change the feedback resistance to change the value of inductance and invariably the peaking and bandwidth. We get the following observations:

Table 5.3: Results of wideband LNA using resistive feedback active inductor

Vin	100µV	
R(in Ω)	100	500
L(inductance)	6.2nH	7.24nH
Vout(in µV)	194.69	194.68
Bandwidth(in GHz)	6.26	5.92
Max. Vout	311.24µV at 2.76GHz	445.71µV at 2.49GHz

5.2.3)Weng – Kuo cascode active inductor

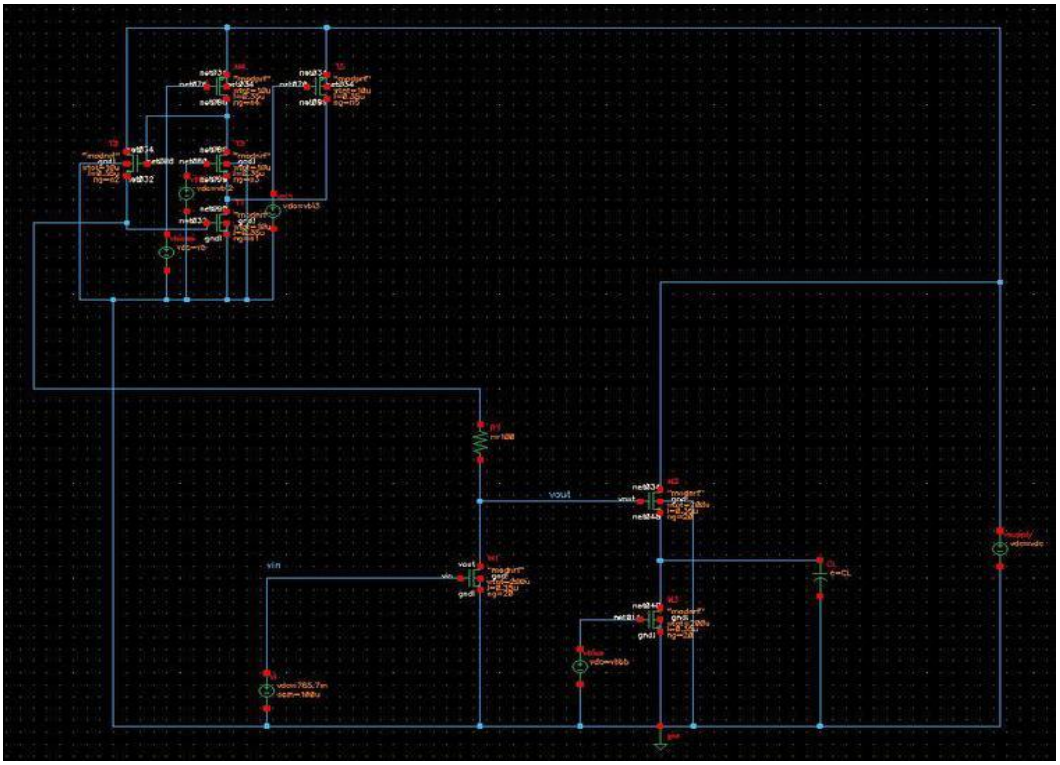


Fig. 5.4:Wideband LNA using weng-kuo cascode active inductor

Table 5.4: Results of wideband LNA using weng-kuo cascode active inductor

Vin	100µV		
vbias(in V)	1	1,25	1,5
L(inductance)	4.35nH	4.44nH	4.68nH
Vout(in µV)	240.37	225.94	223.69
Bandwidth(in GHz)	5.25	5.69	5.72
Max. Vout	431.67µV at 1.49GHz	425.86µV at 2.28GHz	421.73µV at 2.52GHz
Vin	100µV		
vbias(in V)	1,75	2	
L(inductance)	4.73nH	4.79nH	
Vout(in µV)	222.6	221.83	
Bandwidth(in GHz)	5.79	5.81	
Max. Vout	421.44µV at 2.58GHz	419.92µV at 2.61GHz	

5.2.3)Regulated cascode active inductor

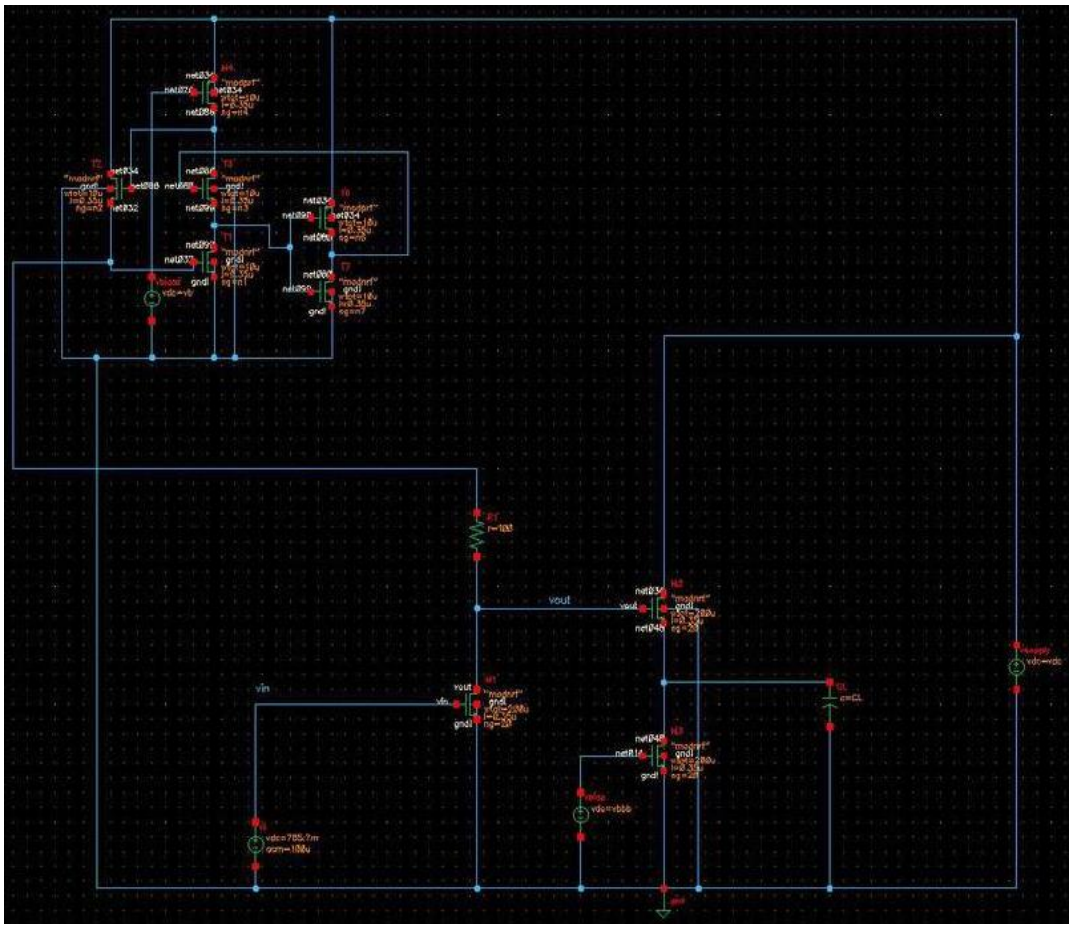


Fig. 5.5:Wideband LNA using regulated cascode active inductor

Table 5.5: Results of wideband LNA using weng-kuo cascode active inductor

Vin	100µV		
vbias(in V)	1	1,25	1,5
L(inductance)	4.57nH	4.65nH	4.92nH
Vout(in µV)	238.23	235.74	226.34
Bandwidth(in GHz)	4.97	5.14	5.36
Max. Vout	397.53µV at 1.69GHz	401.56µV at 2.13GHz	396.84µV at 2.38GHz
Vin	100µV		
vbias(in V)	1,75	2	
L(inductance)	5.26nH	5.53nH	
Vout(in µV)	222.98	219.62	
Bandwidth(in GHz)	5.76	5.89	
Max. Vout	391.21µV at 2.44GHz	387.45µV at 2.53GHz	

5.3)Conclusion on wideband shunt peak LNA

Wideband LNA´s are characterized in terms of their bandwidth extension and peaking. Hence we compare the maximum gain of all the inductors (both spiral and active) and also compare the maximum bandwidth.

Table 5.6: Final conclusion of wideband LNA

Inductor	Maximum bandwidth(in GHz)
Without inductor	2.7
Spiral	4.96
Basic active inductor	6.17
Resistive Feedback active inductor	6.26
Weng - Kuo active inductor	5.81
Regulated cascode active inductor	5.53

We see that resistive feedback active inductor gives maximum bandwidth extension and is the ideal wideband amplifier for circuits where noise figure is not much of a problem (i.e. not constrained). Where noise figure is constrained, we can go for weng – kuo cascode active inductors which give good amount of bandwidth extension and also a low noise figure. Also due to a good quality factor of weng-kuo cascode and regulated cascode, we get more peaking for the same value of inductance. The peaking is not much (constrained to just increase of 200µV from dc) and hence this can be used for comparison with other topologies.

6)Conclusions and Recommendations

Inductors are a critical component in many circuits present in radio-frequency communication receivers. In low-noise amplifiers (LNA) in particular, they are partly responsible for the noise performance of the circuit, matching and gain. Integration of communication receivers in integrated circuits technology implies the challenge of implementing passive components, inductors in particular. Spiral inductors are the common solution adopted, although they present a lot of inconvenient, namely the huge area consumption –related to cost, in IC technology-, losses which degrade the quality factor, and rigidity. Other solutions such as using active circuits showing an inductive behavior have not been popular, essentially since they add other disadvantages like added non-linearity. Anyhow, the advent of multi-standard and reconfigurable receivers may raise the attractive of active inductors, since they are easily tunable.

This thesis had the purpose to evaluate the potential performance of active inductors compared to spirals, compare different alternative topologies, and make a preliminary study of circuit performance using either the passive solution or the active solution, in both a narrowband and a wideband amplifier.

In the first part of the thesis, a set of spiral inductors from a commercial IC technology were characterized by means of s-parameter simulation. Focusing on the desired 2.4 GHz frequency band, the inductors showed inductances in the range 1 nH – 12.5 nH and quality factors in the range Q=3.5 to Q=9.

Next, several active inductors circuits were designed trying to achieve a similar or better performance. Using a basic gyrator-C topology with two transistors and two current sources, we got Q of 2.5 and maximum and inductance values no smaller then 8 nH. When the ideal current sources were replaced by non-ideal elements, the quality factor was further worsened, which discards this topology as a solution.

Since the quality degradation was attributed to parallel losses, adding a negative resistance is expected the increase the inductors Q. There are several topologies that use this approach, we tested the Yodprasit – Ngarmnil circuit which allowed reasonable design flexibility. The results were pretty deceiving, with quality factors still below 1.5.

Another promising alternative is the Weng – Kuo Cascode circuit, which adds design flexibility by adding an extra current source in the circuit and a cascode stage. In this case the results were excellent, with quality factors up to 22.5 and inductance valued in the range of 2nH – 3 nH. Note this is the range of inductances we need to resonate with a 1 pF capacitance at the targeted frequency of 2.4 GHz.

Using a resistive feedback topology also allowed increasing the quality factor as the value of the feedback resistance increased, but this increases the noise generated by the circuit. As a last solution, a regulated cascode configuration also allowed good inductor quality factors, although in this case at a expense or worsened linearity.

We designed two amplifiers, one narrowband and one wideband, to serve as test vehicles to compare the expected performance of the circuit when replacing the spirals by active gyrator-C active inductors. In the case of the tuned narrowband LNA, we used the typical inductively degenerated common-source topology and designed the circuit in a 0.35 µm technology to achieve amplification at 2.4 GHz with a reasonable performance in terms of S-parameters, Noise Figure (NF), and linearity (IIP3). We then replaced the load inductor by the different active inductors designed before. As a summary, the Weng – Kuo cascode topology is the only solution that allowed both better gain and better NF compared to the circuit with only passive spiral inductors, but this is at the cost of a worsened linearity, in the range of 5 – 6 dB. All other solutions showed worse linearity, but they showed improvements either in the gain alone, of NF alone, or no improvement at all –like in the case of the basic topology-. Therefore, it was shown how some topologies allowed competitive performance compared to classical implementations with spiral inductors. Besides that, we also showed the potential for tunability, with the potentiality to vary the output resonance of the circuit –and therefore, the inductance value- by using just an adjustment knob.

To complete the preliminary study on application to amplifiers, we designed a second circuit, in this case a wideband amplifier, in which inductors were used to implement the shunt-peaking bandwidth extension. We observed how active inductors could do the job perfectly, with the added advantage of reduced silicon area and tunability.

In summary, we have demonstrated that active inductors can show competitive characteristics compared to spiral inductors when used in RF communication circuits. The performance obtained varies significantly depending on the circuit solution chosen, but after our study we recommend the Weng – Kuo Cascode topology as showing the best potential for improved quality factor, with a relatively small circuit complexity. In all cases, the use of active inductors worsens the linearity of the circuit (amplifier) in which they are used, but we have shown that they can even improve the noise performance of the circuit, gain, and above all cost –because of the reduced silicon area consumed- and tunability.

7)Acknowledgement

Working on the project has been an excellent learning experience and I would like to first thank my supervisor, Prof. Xavier Aragones, without whom this project would not have been possible.

I would also like to thank the international office of ETSEIB and Amrita Vishwa Vidyapeetham for providing me an opportunity to do this project on the basis of student exchange.

I am also thankful to the director of ETSEIB, to provide me an opportunity to do the final year project.

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