ETSETB - UPC
Department of Electronics Engineering

FULL CUSTOM DESIGN OF A TDC CORE FOR LASER RANGEFINDER APPLICATION

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ABSTRACT

A topology to implement a time-to-digital converter in 130 nm technology for a laser rangefinder application is proposed in this work. Its architecture comprises a delay line as a fine measurement and a synchronous binary counter as a coarse part; this work is mainly focused in the design of the fine measurement. The target is to achieve a 50 ps time interval measure in the device.

The presented approach has been done in order to implement multi-channel multi-hit delay line with the purpose to preserve performance in terms of minimum time interval detectable. Thus, two topologies are proposed on schematic level to achieve multi-channel multi-hit TDC being the one with decoupling inverter the best to implement several channels sharing the delay line. This topology allows keeping the delay element steady regardless the number of channels implemented. Hence, the limitation of channels is given by mismatch variations and metastability errors.
Decoupling inverter topology has been realized on layout and several layout designs have been properly simulated in order to optimize tradeoff among performance and layout size. It is concluded and shown that it can be achieved 35.51 ps as minimum detectable time interval with a maximum number of 15 channels to optimize metastability errors in sampling stage.

RESUMEN

En este trabajo se ha propuesto una topología para implementar un convertidor tiempo-digital (TDC) para una aplicación de localización láser en la tecnología de 130 nm. La arquitectura se conforma de una línea de retardo que hace la función de medida fina y un contador binario asíncrono que hace la medida gruesa; principalmente, este trabajo se focaliza en el diseño de la parte fina de la aplicación. El objetivo es alcanzar una resolución en el tiempo de medida de 50 ps.

La propuesta presentada ha sido hecha para poder implementar una línea de retardo multicanal multipulso con el propósito de mantener el rendimiento en términos de mínimo intervalo de tiempo detectable. Así, dos topologías son presentadas a nivel esquemático para conseguir un TDC multicanal multipulso, siendo la topología con inversores de desacoplo la mejor para implementar varios canales en la línea de retardo. Esta topología permite mantener el retardo estable sin importar el número de canales que se quieran implementar. Por lo tanto, la limitación de canales se da por errores de metaestabilidad y de desajuste de variaciones en los parámetros de los componentes.
La arquitectura con inversores de desacoplo se ha realizado en layout y se han realizado varias simulaciones con diferentes layouts con el propósito de optimizar el compromiso entre el rendimiento y el tamaño de éste. Se concluye y se muestra que se puede obtener un retardo mínimo de 35,51 ps con un número máximo de 15 canales para optimizar errores de metaestabilidad en la etapa de muestreo.

RESUM

En aquest treball s'ha proposat una topologia per a implementar un convertidor temps a digital (TDC) per a una aplicació de localització làser en la tecnologia de 130 nm. L'arquitectura disposa d'una línea de retard que fa la funció de mesura curta i un comptador binari asíncron que fa la mesura gran; principalment, aquest treball s'ha focalitzat en el disseny de la part de mesura curta de l'aplicació. L'objectiu es aconseguir una resolució en el temps de mesura de 50 ps.

La proposta presentada ha sigut feta per a poder implementar una línea de retard multicanal multipols amb el propòsit de mantenir el rendiment en termes de mínim interval de retard mesurable. Així, dos topologies són presentades a nivell esquemàtic per aconseguir un TDC multicanal multipols, essent la topologia amb inversors de desacoblament la millor per implementar varis canals en la línea de retard. Aquesta topologia permet mantenir el retard estable sense importar el número de canals que es volen implementar. Per tant, la limitació de canals ve donada pels errors de metaestabilitat i de desajust de les variacions en els paràmetres dels components.
L'arquitectura amb inversors de desacoblament s'ha realitzat amb layout i s'han realitzat varies simulacions amb diferents layouts amb el propòsit d'optimitzar el compromís entre el rendiment i la mida del d'aquest. S'ha conclòs i mostrat que es pot obtenir un retard mínim de 35,51 ps amb un número màxim de 15 canals per optimitzar els errors de metaestabilitat en la etapa de mostreig.

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Firstly, I would like to thank UPC to allow me working on this project, as well as my supervisors, Piotr Michalik and Jordi Madrenas, for guiding and supporting me during the project.

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LIST OF ACRONYMS

TDC	Time to Digital Converter
MTBF	Mean Time Between Failures
MUX	Multiplexer
FF	Flip-Flop
MQO	Miniature Q-switched Oscillator
LIDAR	Light Detector and Ranging
MPPC	Multi Pixel Photon Counter
INL	Integral Non-Linearity
DNL	Differential Non-Linearity
LSB	Least Significant Bit

LIST OF FIGURES

CHAPTER 1

1. INTRODUCTION

1.1. Background

The aim of many researches on instrumentation is to measure a short period of time; trying to reach the best performance in terms of time-interval. Nowadays the demand to achieve precise and short time-intervals is growing (data converters, high-energy physics, laser range finder, to name just a few) and new architectures are needed to develop to reach good resolution for that purpose. It should be noted that pico-second is typically the considered time range.

It has to be taken into account that the system to measure the time-intervals are analog and mixed-signals circuits. Thus, a digital representation of the time in the output is wanted since the measurement will have to be treated by other digital circuits. Digital circuits give more simplicity to the design and logic functions can be done by small and compact circuits; also the design can be programmable or reconfigurable.

A common way to measure these time intervals is using TDC (Time to Digital Converters). Nowadays, TDC are very commonly used in the electronic field and they lead research to find the best solution in terms of time-interval resolution. Besides, there are some issues that one has to take into account for the design such as quantization error, nonlinearity problems, power consumption, metastability, area occupied and so on.

TDC has been used during years as a phase detector, however other applications are emerging quickly such as biomedical imaging [14], time-of-flight measures [15] or laser rangefinder in robots [16]. Clearly, new applications need different kind of requirements than the phase detector.

There are several methods used to measure precisely time-intervals and then convert it into a digital data [1]. The most well known methods are the coarse counting, fine measurement methods and Vernier method among others. A lot of researches have studied those TDC methods and the idea expand to use brand new technologies which gives more resolution and better performance; at the same time these new technologies present important challenges to the designers since new problems can appear.

1.2. Problem Definition

The first approach to define a TDC consists of two stages; translating a physical event into voltage and then convert this voltage into a digital value. In figure 1.1 is shown a simple case of TDC.

As it can be seen in figure 1.1, the detectors have to perceive the pulses which come from to some physical event. Once the physical events have been detected, the time discriminators are in charge to generate the pulses, afterwards the digital circuit has to measure the temporal distance between them and then show the result in a digital word. In this field, the pulses are commonly named start pulse and stop pulse.
It should be noted that this is only an example to show the generic function of a TDC. There are a lot of ways to design a TDC, each one depending on the goal of the designer, but the main aim is to measure time-intervals.

Although the architecture of the TDC is very clear, it has several issues to take into account at the time to design it. One of the biggest challenges for a designer is to achieve high time resolution. There are many factors which can degrade the resolution of the TDC such as mean time between failures (MTBF), metastability or technology limitations. Those factors have to be studied in each TDC design and they can affect in many different ways.

Time resolution leads researcher to use new technologies and to implement new TDC designs to get better performance for measuring time-intervals. Furthermore, new applications for TDCs are demanding multiple inputs and multiple physical events in the same signal, or commonly named multi-channel multi-hit TDC. This area opens a range of possibilities and also introduces other issues like the signal distribution.

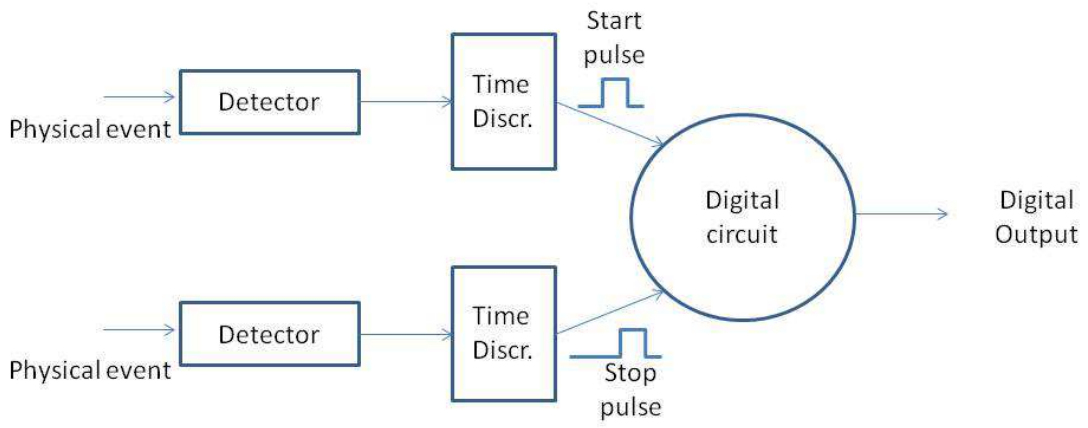


Figure 1.1: Simple TDC

1.3. Objectives and motivation

The goal of this work is to study the different factors that can be critical to reach a high time-interval resolution and to do a design for an application.
In laser rangefinder applications, a laser emits pulses to the surface, and then the time-interval between the emitted pulse and the echo pulse is calculated. Once the time-interval has been calculated, the distance among the laser and the surface can be located. This project has been done in collaboration with CD6 (Centre for sensors, instruments and systems developments located at the campus of the UPC in Terrassa). Their aim is to generate a 3D image from the time-of-flight measurement of a laser beam that is scanned in a space area. An example is shown in figure 1.2; in this context, this project is focused on the time-interval measurement between the transmitted and received pulse, which contains the TDC.

The way to detect the echo pulses is by a photon detector followed by an amplifier discriminator. In this project a photon detector [2] and NINO ASIC [3] have been used for the amplifier discriminator due to its excellent timing resolution at very high rate, while at the same time it provides a very low noise and the power consumptions is also good. Since the pulses are received at very high rate it is needed a system to detect them properly to calculate the time-of-flight accurately. Therefore, a TDC is introduced in the application.

In this work a TDC design based on fine measurement method and coarse counting to serve the laser application is used. Moreover, receiving more than two physical events is needed; hence, multi-channel multi-hit TDC is required in the design.
The fine measurement part has been done with a delay line, which is one of the subjects that limit the time-interval resolution. The coarse counting part has been done using an error-free sampling method using only two counting samplers [17].
Also the simulation and verification of the designs have been done following the steps until the chip fabrication. Those steps include the proposal of many designs, the simulation and verification of their functionality using the appropriate tools (mostly Cadence), the realization of the layouts taking into account the rules of layout design and finally the accomplishment of the full layout of the TDC chip.
It should be noted that during the work several designs of TDC have been done in order to achieve the best possible performance for our goals. Therefore, in this work is described the path to design TDC for serving the laser rangefinder application, both schematic and layout level.

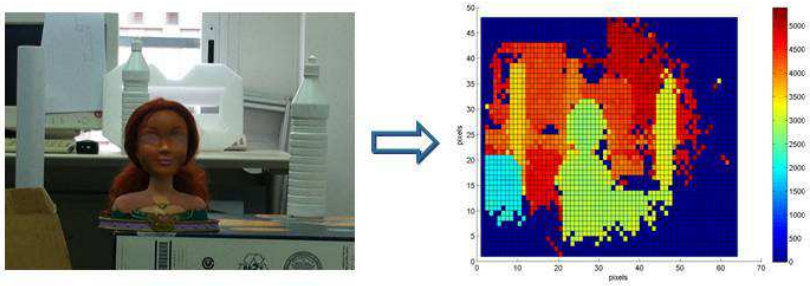


Figure 1.2 : 3D image generated from the laser beam [21]

1.4. Overview

This work is organized as follows:

Chapter 2

Environment of this work is presented in this chapter. Different parts of the TDC will be shown and explained one by one. Also, the last section contains the requirements and properties of the TDC.

Chapter 3

Schematic design are discussed and shown in this chapter. All the features we have to take into account will be shown and the design procedure during the project will be explained regarding the schematic design.

Chapter 4

The study about the metastability in the TDC is described in this chapter. Proper characterization of metastability in the delay line has been done.

Chapter 5

The implementation of the delay line in layout is shown in this chapter. Different features will be discussed and guidelines will be shown in order to decribe the design procedure.

Chapter 6

Conclusions are contained in this chapter.

CHAPTER 2

2. ENVIRONMENT

This work is focused on the analog design of the TDC; specifically, the fine measurement part. The main parts of the fine measurement are introduced and besides, all the parts involved in the full system are shortly explained. Therefore, a general view of the full system is presented in this chapter.

2.1. Laser emitted and detection

As it can be seen in figure 2.1, the first step in the system is to emit a laser against the surface and then, detect the reflected beam with photo detectors. Afterwards, the signals generated from the photo detectors will be treated by an amplifier and a discriminator in order to make them suitable for the TDC.

A miniature Q-switched oscillator (MQO laser) has been used to generate the laser. This kind of laser allows having several operation modes and it can be easily changed by external data ports. The main features of the laser are its variable repetition rate and it can be emitted with constant energy [4], [5]. Nowadays, the applications of the laser are from light detector and ranging (LIDAR) until bioinstrumentation, being the field of its applications really wide.

The second step is the reception of the laser by the photo detectors. Concretely, a multi pixel photon counter (MPPC) of Hamamatsu Company [2] has been used in this system. It has an excellent photo-counting capability due to its implementation with multiple avalanche photodiode. Also it has a high time resolution, which is important for the TDC in next steps, and it has a low voltage operation. It is really important to be very accurate with the treatments of the signals since the next stages will be regarding the TDC. Thus, a detailed specification of the pulses is needed as it can be seen in section 2.1.1.

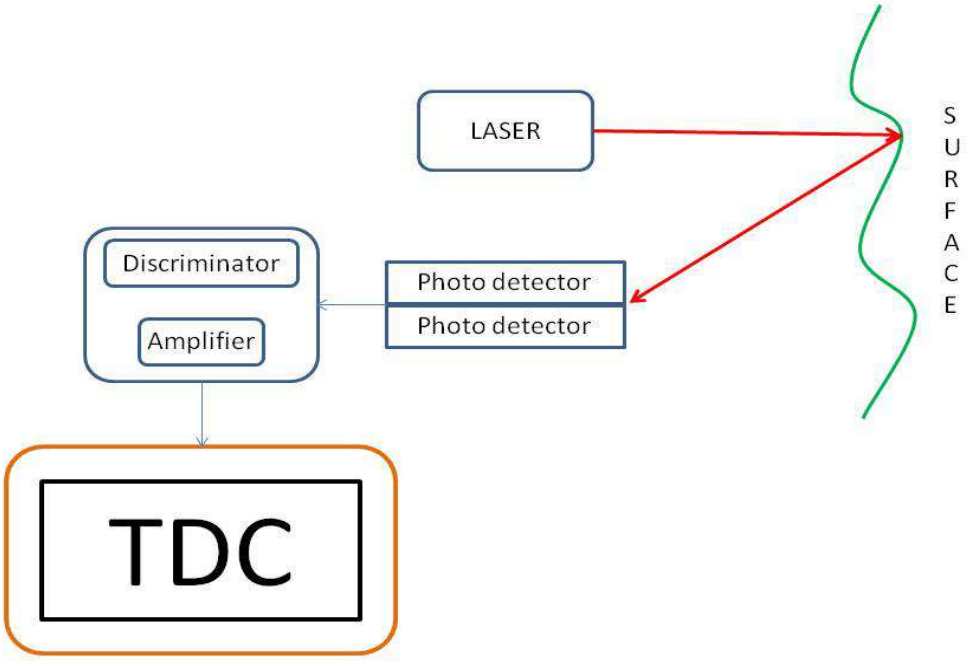


Figure 2.1: Laser emitted and detection scheme

Once the MPPC has detected the photons, a signal processing is necessary for having the right signals at the input of the TDC. Hence, an amplifier and a discriminator are used.

The amplifier gives to the TDC a voltage level that can be treated afterwards, very low voltage are converted into a range of some volts. In figure 2.2 is shown an example of circuit where the MPPC is working with the amplifier.

Then, a discriminator is needed after the amplifier for the purpose to avoid noise voltage at the input of the TDC and to discern the minimum value that the trigger can discriminate. The function of the discriminator is similar as a Schmitt trigger and it can be formulated as follows:

$$Discriminator\ Output = \begin{cases} 0\ for\ Discriminator\ input \leq X - Y \\ V_{dd}\ for\ Discriminator\ input\ > X + Y \end{cases} \quad (2.1)$$

Where V_{dd} is the input voltage of the TDC that can be interpreted as bit 1. The value $X - Y$ makes reference at the minimum necessary voltage to get V_{dd} at the output and $X + Y$ to get 0.

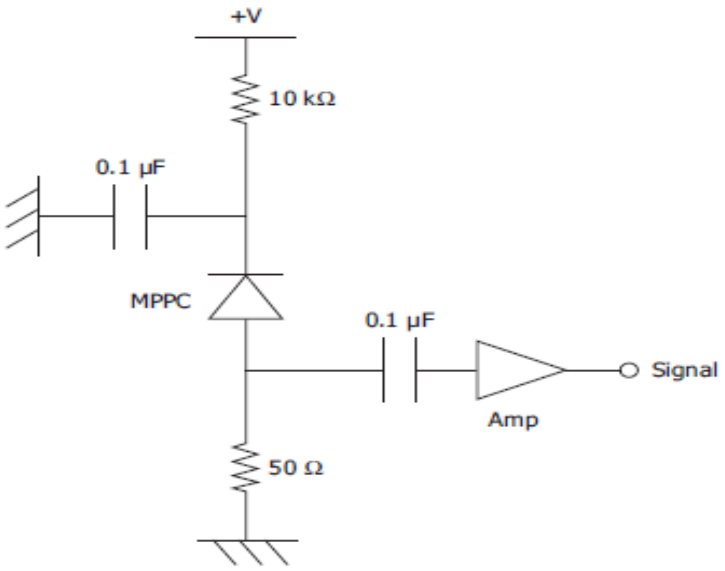


Figure 2.2: Photo-detector MPPD followed by an amplifier [2]

2.1.1. TDC Inputs

In this section we want to analyze the signals when they enter the TDC. The features of the TDC inputs are important to know them in precision since they will define some specifications in the TDC.
As it was mentioned before, these signals are taken from the discriminator and it can be discerned between two signals: start and stop pulses.

2.1.1.1. Start pulse

A start pulse is generated at each time the laser emits a pulse against the surface. It means that the laser launch time is known. A device inside the laser is required for the purpose to generate the start pulse. It is not necessary to go further in the details since the goal of the TDC is to know how the pulses are.

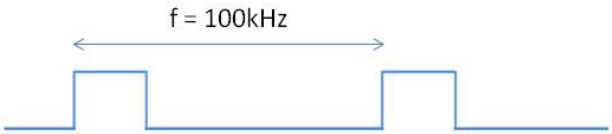


Figure 2.3: Start pulse

As it can be seen in figure 2.3, start pulse has a 100 kHz frequency. Among two start pulses, the stop pulses will arrive to the TDC from the discriminator.

2.1.1.2. Stop pulse

Stop pulses are generated due to multiple laser reflections, as it is shown in figure 2.1 and each reflection symbolize one stop pulse. The main features of these pulses can be seen in the next figure 2.4:

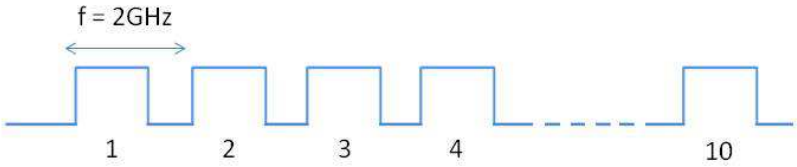


Figure 2.4: Stop pulse

As it is can be seen in figure 2.4 the stop pulse is a train of maximum 10 pulses with a maximum frequency of 2 GHz. This train of stop pulses will be between two consecutive start pulses and they can be generated either by the surface reflections or by obstacles between laser and surface (such as raindrops).

2.2. TDC Parts

In this section different parts of the TDC are described. The functionality of each part is shown, as well as a description of them. In the figure 2.5 the most important parts of the TDC are shown:

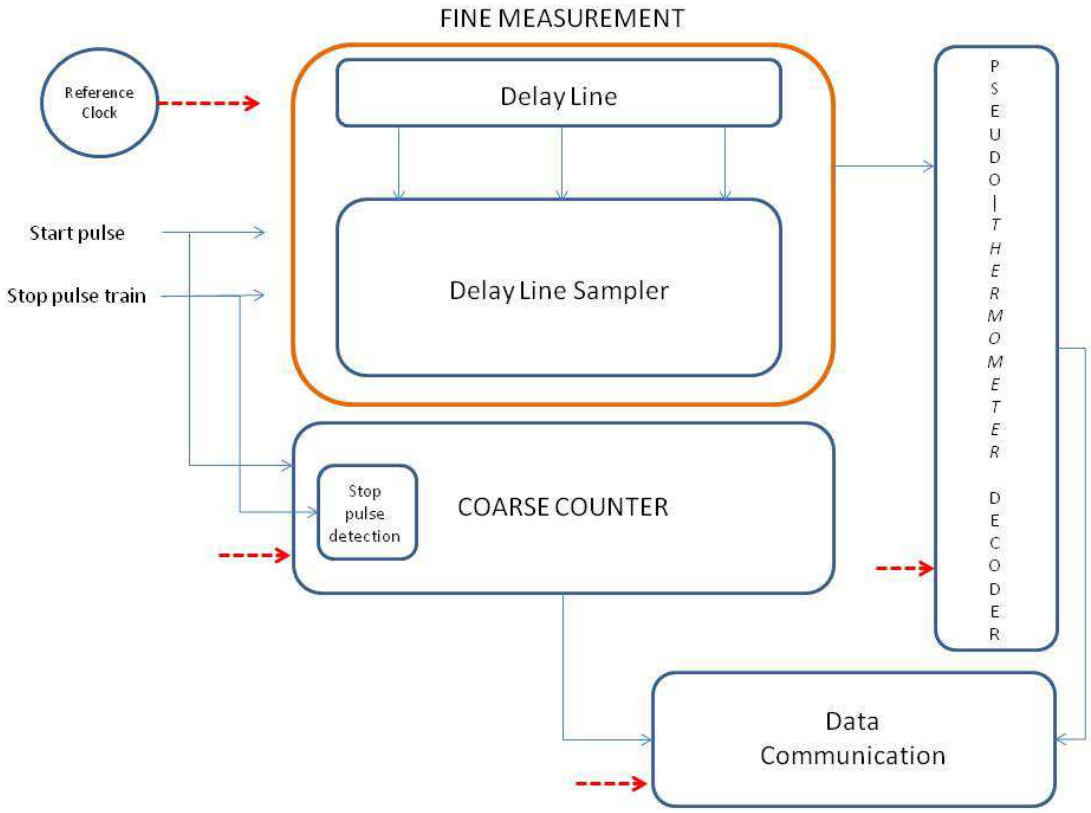


Figure 2.5: TDC architecture

The fine measurement consists of two different blocks: delay line and delay line sampler, which are the main focus of this work. Delay line consists of a train of buffers, each one having the delay τ, through which passes the clock reference. Then the state of the delay line is sampled by the rising edge of the stop signal. As the TDC is multi-channel, each channel has his own detection stage. However, the delay line is shared between all the channels.
Fine measurement is very important at the time to enhance the resolution of the system. The smaller the delay that is introduced to the signal, the better resolution can be reached by the TDC.

As it can be seen in figure 2.5, the stop pulses are received in a waveform as a train of pulses. Hence, the time each one arrives is necessary to be detected, so a stop pulse detection module is used for that purpose.

Once the pulses reach into the TDC structure, the coarse counter is responsible for measuring how many intervals of the reference clock are in the pulses, either the start or the stops ones.

At the final stage the pseudo-thermometer decoder can be found. It allows us to convert all the input bits that come from the fine measurement to output bits which can be interpreted easily.

2.2.1. Coarse Counter

The easiest way to measure time intervals is using coarse counting since it involves only the use of synchronous binary counters.
Binary counters are driven by the reference clock and their goal is to measure clock time intervals between start and stop signals.
A simple example is shown in figure 2.6 where the start pulse enables the counting of T_{CLK} and the stop pulse finish the counting. Therefore the result of the binary counter is:

$$T_{Counter} = n \cdot T_{CLK} \tag{2.1}$$

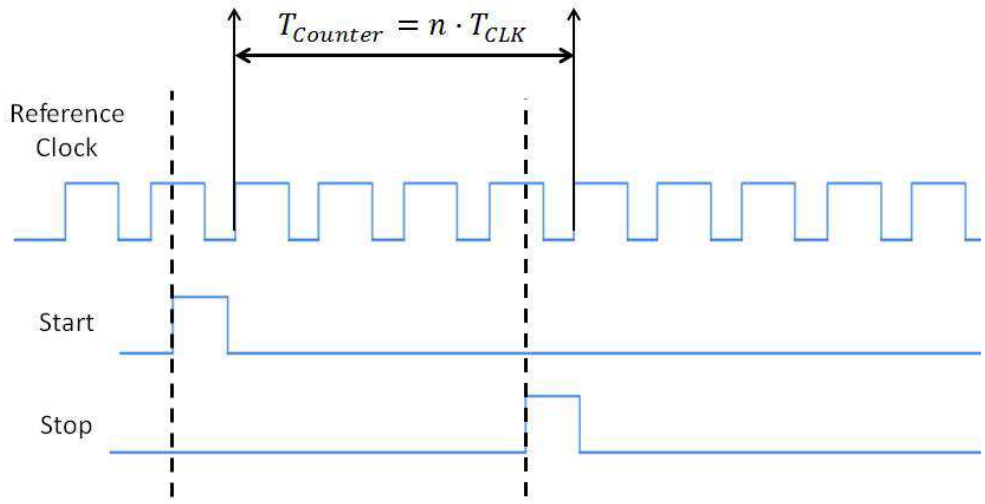


Figure 2.6: Coarse counter simple example

As it is shown in figure 2.6, the maximum discern value of the binary counter is T_{CLK}, thus the resolution is equal to T_{CLK}.
The error of a single measurement can achieve $\pm T_{CLK}$. For the purpose to improve this resolution a fine measurement is needed.
Besides, the n in equation (2.1) is the decimal equivalent of the integer binary number Q at the output of the binary counter as it can be seen in figure 2.7. Therefore, the number of bits used in the binary counter determines the maximum value that the

system can measure and the maximum distance available to detect. Number of bits is calculated in section 2.3.

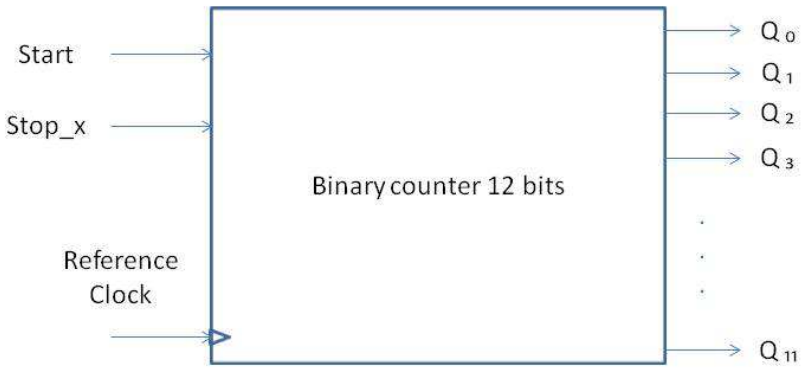


Figure 2.7: Binary counter block

Coarse counter architecture presented in [17] has been used in this work due to its simplicity. Also, it is suitable for multi-channel TDCs which fit our environment perfectly.

2.2.2. Fine measurement

In order to have better accuracy than the coarse counter, a fine measurement is applied. The fine measurement is based on delay lines and its sampling.
Delay line allows splitting the reference clock period as it is shown in figure 2.8 and 2.9 through several delay stages inserting a known delay Δt.

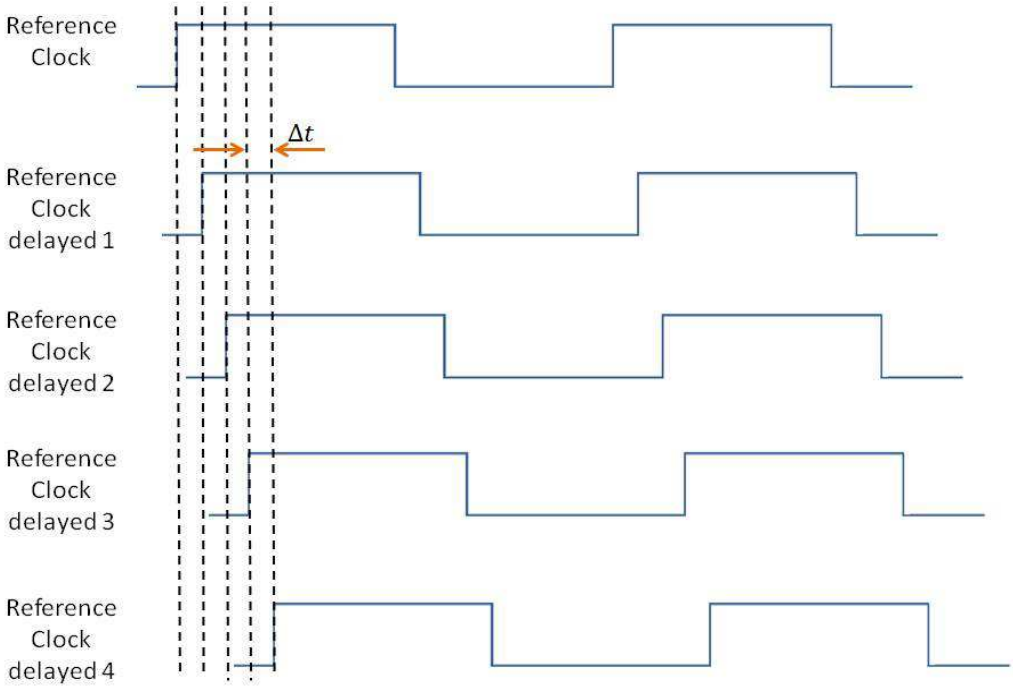


Figure 2.8: Reference clock delayed Δt

Flip-flops are used for the purpose of sampling the delay line. A simple example of a delay line and its sampling is shown in figure 2.9.
The stop pulse sampling is analogous to the start sampling; besides, it shares the same delay line.
Delay line is the main focus on this work as it has been said previously. Therefore, in next chapters it will be discussed deeply.

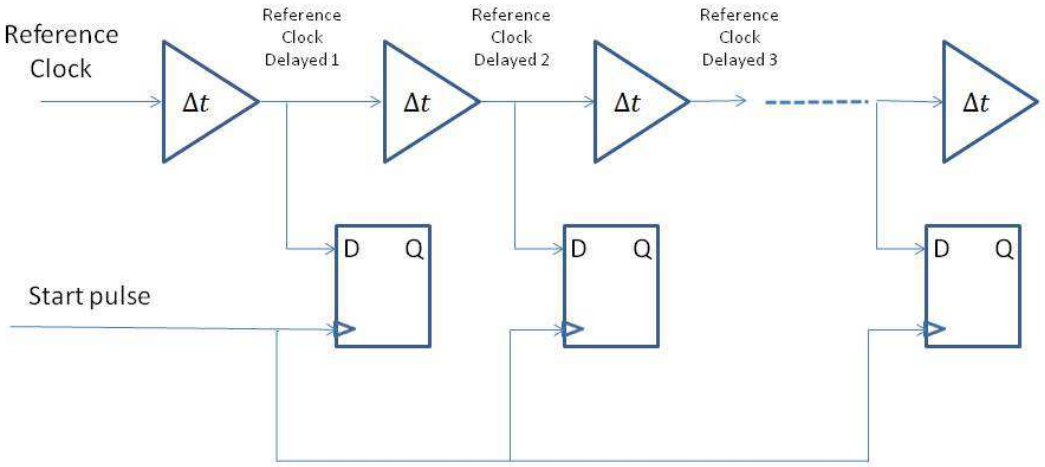


Figure 2.9: Delay line stages and sampling

If fine measurement is added to start and stop, the reading will be done as figure 2.10 shows:

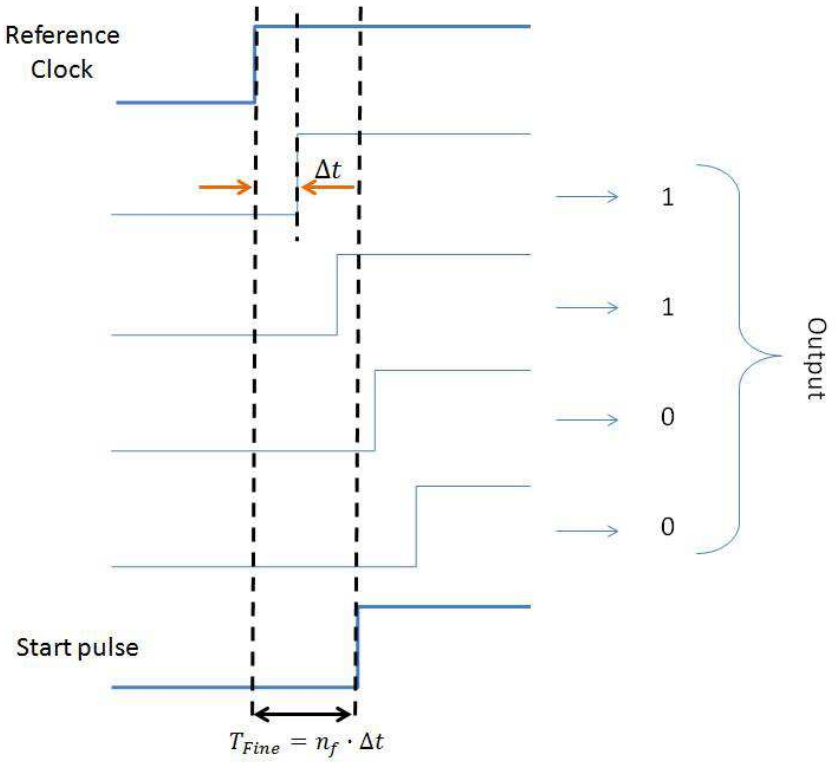


Figure 2.10: Coarse plus fine counting simple example

Where n_f is extracted from the output. Therefore, the resolution of the measurement turns into Δt as it is shown in figure 2.10.
Hence, the measurement of time interval among start and stop pulse involves both coarse and fine measurement.
Fine measurement will be explained in details in Chapter 3.

2.2.3. Bit Decoder

The code given by the outputs of the sampling stage consist of a specific number of 0's and 1's depending on where the rising/falling slope is in the delay line. An example is shown in figure 2.11.

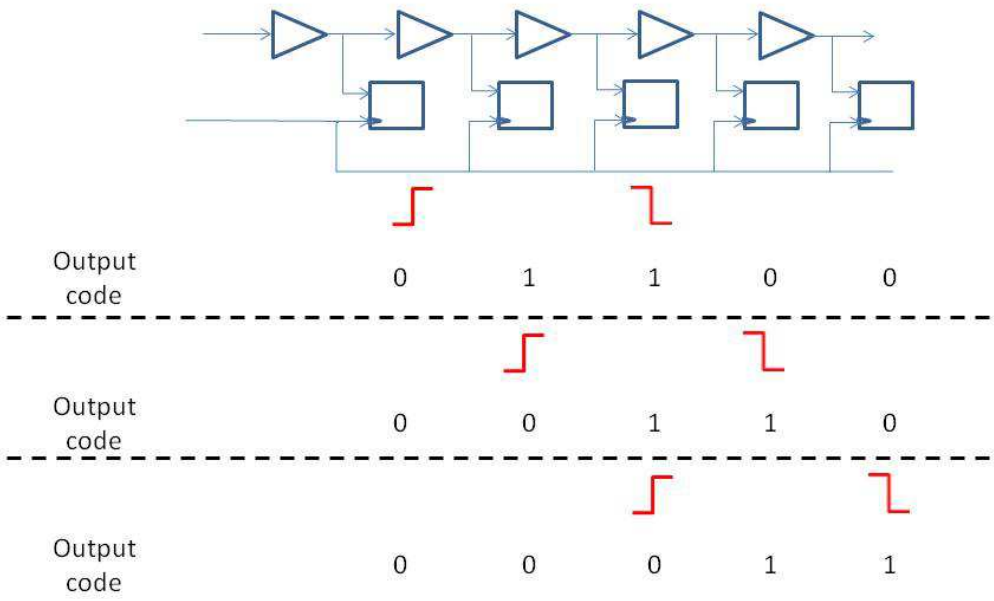


Figure 2.11: Code examples

The output of fine measurement generates a code which is similar to thermometer code; then, a pseudo-thermometer decoder is needed for the purpose to convert this code into an integer binary number as it can be seen in figure 2.12. The decoder counts the number of 1's and its phase difference along the delay line.
The output of the decoder means the number of delay elements that have switched until the start/stop pulse arrives. Thus, n_f is the decimal equivalent of the integer binary number at the output of the decoder.

In the design a pseudo-thermometer decoder with 7 output bits is used, according to equation (2.3), since the design will have up to $64 \pm N_{error\ stages}$ delay stages in the delay line which turns into 74 different states to decode in order to guarantee correct operation taking into account the process tolerances. The number of stages has to be equal as the maximum number of stages needed taking into account the best case in delay sampling as it is shown in section 5.2.1.

$$2^{N_{bits\ decoder}} = 74 \quad \rightarrow \quad N_{bits} = 7 \tag{2.3}$$

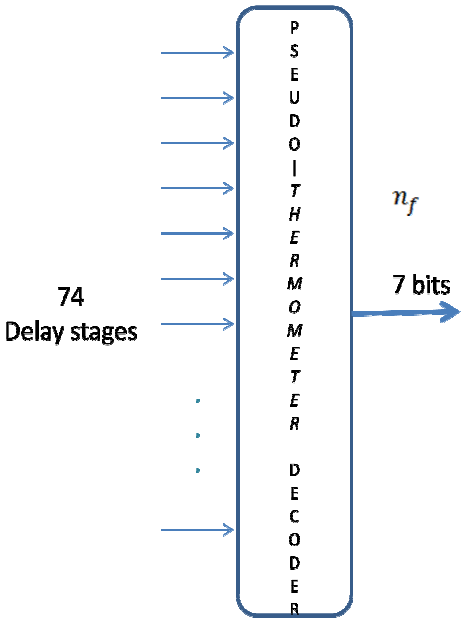


Figure 2.12: Pseudo -thermometer decoder

2.3. Assumptions

The principal assumptions to start the schematic design are specified in this section. It is necessary to set the features in the design in order to develop the architecture of the TDC.

The needs of the TDC are given by the resolution wanted for the laser rangefinder. The spatial resolution that is wanted is 7,5mm which means that the minimum time that should be detected is:

$$D = c \cdot \frac{t}{2} \tag{2.4}$$

Where c is the speed of light ($3 \cdot 10^8$ m/s) and t is the time for the laser to go and come back. The minimum time that can be measure determines the minimum possible distance. Hence, following equation (2.4) the minimum time that is wanted to measure is 50 ps in fine measurement. Therefore, the system should be able to discern this time-interval between two pulses. Also, the maximum distance that is wanted to measure determines the bits used in the coarse counting; thus, 1250 m represents a maximum time measure of 8,33 µs which turns into 3608,33 clock samples ($f_{CLK} = 433$ MHz). Following equation (2.5) the number of bits required for the coarse counting is 12.

$$2^{N_{bits\ coarse}} = 3608{,}33 \quad \rightarrow \quad N_{bits} = 12 \tag{2.5}$$

Another mandatory requirement concerns about the economic field. We want to do the application as cheaper as possible. As it will be explained later in this Chapter, many technologies are available to do the circuitry of the system, but the best ones will increase the price per chip. Because of that, it will be chosen the cheapest CMOS technology which fulfills the specifications.

Prices for CMP 65 nm technology: 7.500 €/mm2

Prices for CMP 130 nm technology: 2.200 €/mm2

Prices for Lfoundry 150 nm technology: 900 €/mm2

130 nm technology has been selected. At the time to choose the technology the tradeoff between performance and price is high. Hence, it has been decided not to use 150 nm due to its poor performance and skip the 65 nm technology because its price.

Regarding the delay line, buffers as delay elements are used in this work. This delay line has been chosen instead of delay line with inverters. It is well known that inverter delay line gives double resolution than buffer delay line [19], but it needs two coupled chain of inverters in comparison with the one chain of the buffer delay line. This simplifies the architecture of the TDC considerably. Besides, inverter delay line is more sensitive to mismatch variations since the inverters have different rise and fall time. Even compensating the characteristics of the inverters, local process variations can

cause faster delay in one chain, which can lead into a systematic non-linearity error. On the other hand, buffer delay line has less resolution but it divides the clock in equally spaced time being stronger in mismatch variation terms.

Two channels have been used to demonstrate multi-channels capability and further scalability of the system; besides, two channels can be used to improve the system performance by averaging the measured result. Each channel has its own start and stop signals; it means four loads per each single stage of the delay line since the stop hits will be detected by a shift register as it is shown in figure 2.13. This has been done in order to reduce the input load of the delay line. Hence, architecture with multi-channel multi-hit TDC is needed in order to satisfy the specifications regarding the 10 stop hits. Further details in the TDC architecture are described in Chapter 3.

Total error of the fine measurement is given by the error produced by the start and stop errors. Since start and stop events are independent, the total error is their root mean square as it can be seen in equation (2.6).

$$50\ ps = \left(\sqrt{\left(\varepsilon_{fine\ start}\right)^2 + \left(\varepsilon_{fine\ stop}\right)^2}\right) = \left(\sqrt{2 \cdot \left(\varepsilon_{fine}\right)^2}\right) \rightarrow\ \varepsilon_{fine} = 35{,}35\ ps \qquad (2.6)$$

Besides, a special metastability-robust flip-flop from the manufacturer standard library is used in the 130 nm design environment: FD2Q_SYNCHS. This flip-flop has been chosen due its better performance in terms of speed and error probability. Comparison between standard flip-flop and FD2Q_SYNCHS flip-flop is performed in chapter 4.

Assumptions Overview:

- Delay line composed by buffers
- Coarse Counting as in [17]
- Maximum stage delay 35,35ps
- Multi-hit architecture (up to 10 stop hits)
- Multi-channel architecture (2 channels)
- Shift registers to detect hits
- Technology used : 130nm (see section 3.1)
- Voltage supply : 1,2 Volts
- Flip-flop used: FD2Q_SYNCHS

During the design process several architectures have been done. Each one of them has been thought and simulated properly in the following chapters to see its performance in terms of keeping all the requirements. There are many designs that can fit the requirements but each one has its own properties, given commitments among its specifications.

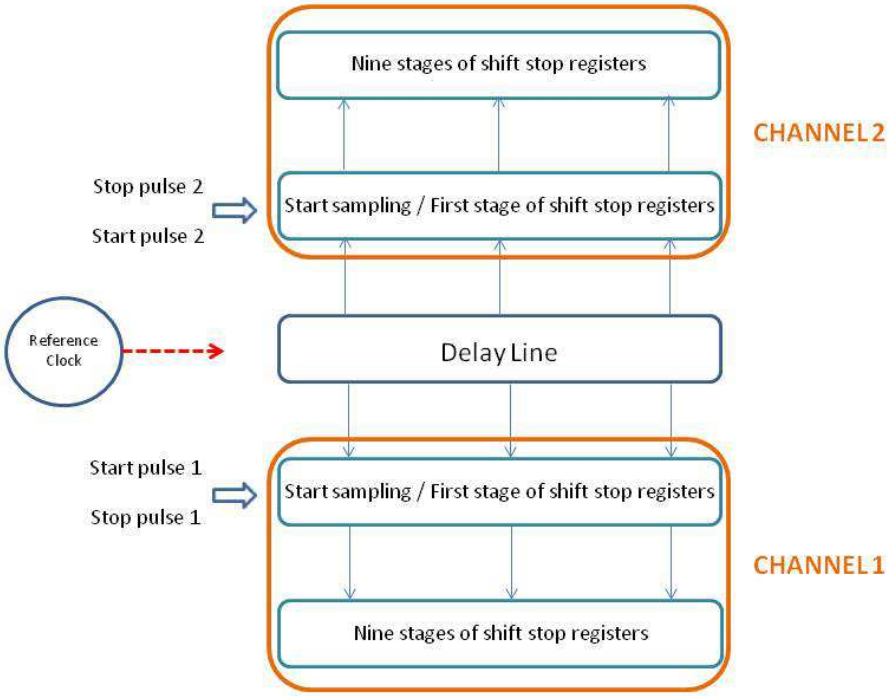


Figure 2.13: Scheme of TDC architecture

CHAPTER 3

3. FINE MEASUREMENT SCHEMATIC DESIGN

In this chapter is presented the main features to take into account at the time to design the delay line and its sampling stage. Different kind of architectures are presented and discussed properly in order to choose one to implement in layout design afterwards. Moreover, simulations have been done to justify which architecture is more suitable for the rangefinder application.

3.1. Schematic features

This section has the purpose to explain the main features that can affect the performance of the delay line.

3.1.1. Output load

Any logic gate has an output load determined by the number of devices connected to it. This input drive can affect at the response time of the device. Getting into details, the rise and fall time of the affected device can turn on bad performance if a big load is connected at the output. Each device connected at the output will increase the output load slowing down the performance of the slope.

Considering the fall time as the transition time among 10% and 90% of its total value and the rise time as the transition time among 90% and 10% of its total value; equation (3.1), (3.2) [18] shows the relation between rise/fall time and output capacitance.

$$t_f = k_n \cdot \frac{C_L}{\beta_p \cdot V_{DD}} \tag{3.1}$$

$$t_r = k_p \cdot \frac{C_L}{\beta_p \cdot V_{DD}} \tag{3.2}$$

Rise/fall time increases as the load capacitance increases. It can be seen in equations (3.1), (3.2) where C_L is the output load, V_{DD} is the voltage supply, $\beta_{p,n}$ is the MOS transconductance parameter and $k_{p,n}$ is a factor given by $k_{p,n} = \left(\frac{W}{L}\right)_{p,n} \mu_{p,n} C_{ox}$[1].

Moreover the response time of the device can be affected as well. Response time can be divided into two terms as the equation (3.3) shows:

$$t_d = t_e + t_p \tag{3.3}$$

$$t_e = t_{e1} \cdot f = t_{e1} \cdot \frac{F}{C_{in}} \tag{3.4}$$

Where t_e is the effort delay and it depends on the load connected at the output of the device. t_{e1} is the unitary effort delay and f is the relative fanout.
As it can be concluded from equation (3.4), effort delay increases as the fan-out rise up.

t_p is the parasitic delay and it depends on internals features of the device.

Proper simulations have been done in order to see the effects of a load capacitor at the device output. Figure 3.1 shows the setup simulation and figures 3.2 and 3.3 shows the results obtained.

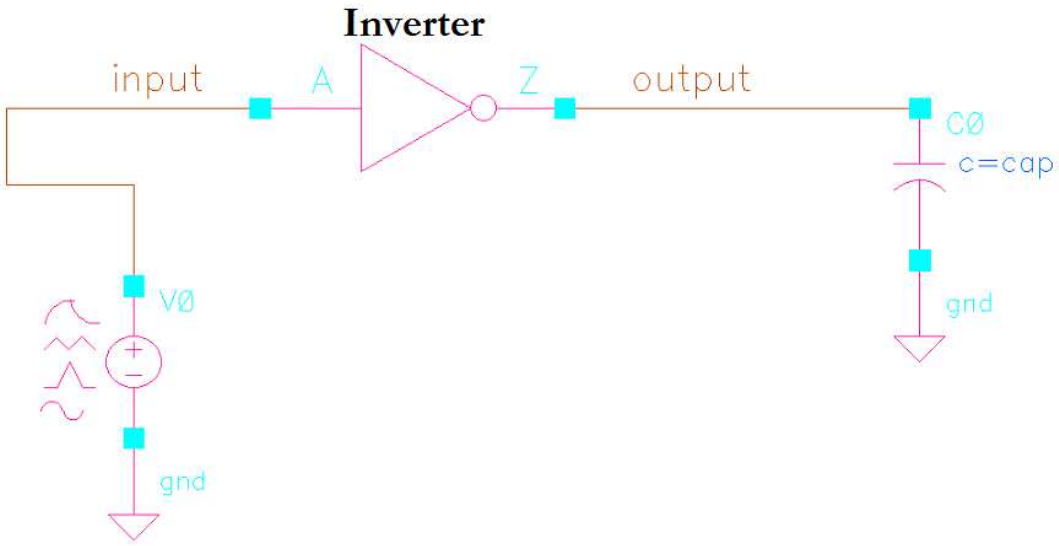


Figure 3.1: Schematic setup of an inverter loaded by a capacitor with Wn = 1.05 µm and Wp = 0.585µm

The purpose of this setup is to parameterize the value of the load capacitor at the output. The capacitor would simulate the load of the inverter. As much bigger is the capacitor value would mean more devices connected at the output of the inverter.

[1] $\left(\frac{W}{L}\right)$ is the channel length and width aspect radio, C_{ox} is the gate oxide capacitance and μ is the carrier mobility

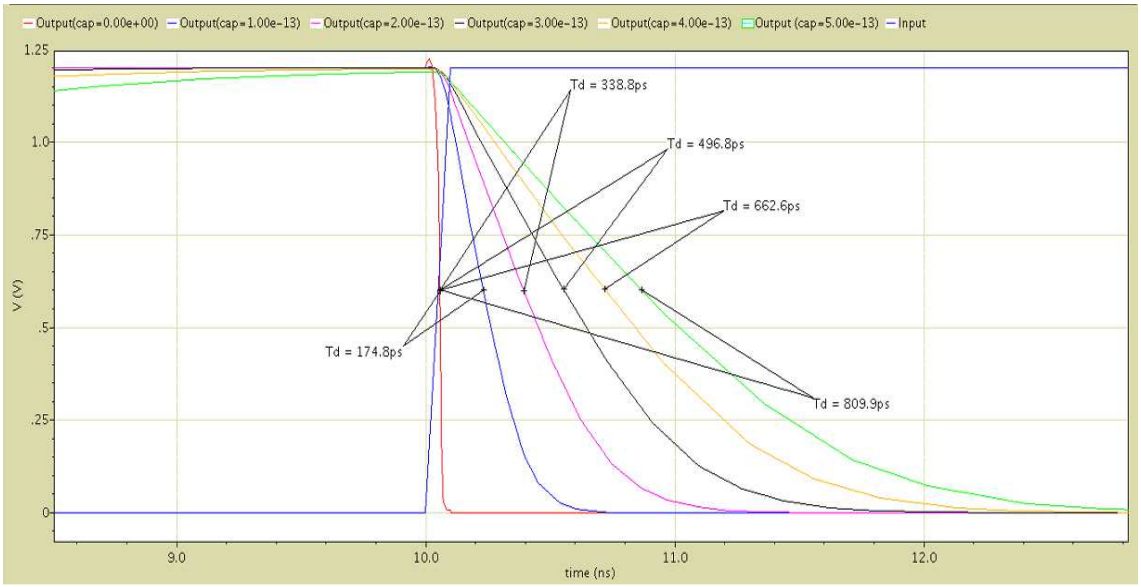


Figure 3.2: t_d for parametrical analysis between input and output nodes (100pF, 200pF, 300pF, 400pF, 500pF)

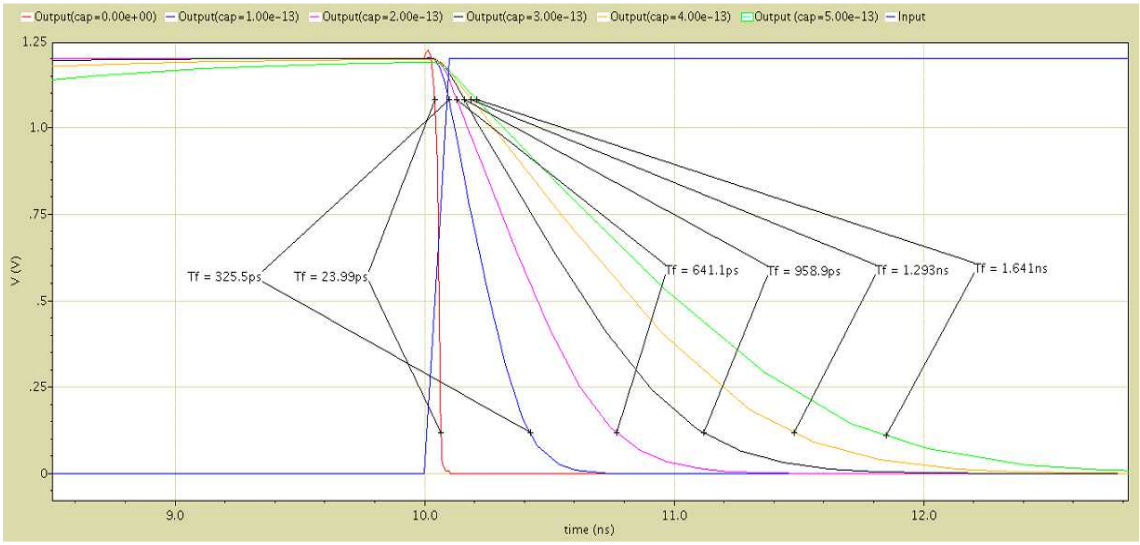


Figure 3.3: t_f for parametrical analysis between input and output nodes (0pF, 100pF, 200pF, 300pF,400pF, 500pF)

Both t_d and t_f are increasing as the load capacitor is raising its value as it can be seen in previously figures 3.2 and 3.3. The t_r is dual as t_f.

This feature does not allow connecting a lot of devices to one node since the response time of the device connected to them would be slower, rise and fall time as well. Input load has an important impact in the fine measurement design since a great accuracy in terms of delay is needed. Furthermore, the slopes can increase the probability to have failures as it can be seen in chapter 4 or section 3.2.3.

3.1.2. Mismatch and global process variation

There are two different process variations which can happen in a logic device:

- Global Process variation
- Mismatch variation

Global process variation makes reference at the process variations that can occur in the device when integrated circuits are fabricated in wafers, and even on different wafers. It is usually represented by corners (best, typical and worst case) and global montecarlo simulations. It should be noted that in 130 nm technology and above, it is usually assumed that all the devices work in the same corner.

Mismatch variation involves the local variation in attributes of transistors in one chip. In this work it is only considered mismatch variation since the TDC only involves one chip. It is important in nanotechnologies since the variation can become a relevant percentage in the device features which can involve a relevant variation of its performance. Mismatch variation can be measurable through statistical analysis by making a lot of simulations to analyze the behavior of the device in different situations. For that purpose, it is used local montecarlo simulations. Those simulations indicate the range of values for the attributes in the transistors.
Montecarlo simulations give two basic measures to characterize the device performance: mean and standard deviation.

For the purpose to make sure that the design meets the specifications several simulations will be done taking into account the different corners where the device can work and the mentioned montecarlo simulations to characterize each corner properly.

3.1.3. Bubble

A bubble effect is produced when two consecutive sampled bits are wrong in the delay line. Taking into account that we have pseudo-thermometer code at the output of the sampled stage is easy to be detected by signal post data processing if one bit is wrong. But if two consecutive bits are wrong, it can produce a significant variation in the pseudo-thermometer decoder. Furthermore, the wrong measure can be propagated since the sampling stage will be done by a shift register as it can be seen in section 3.3.

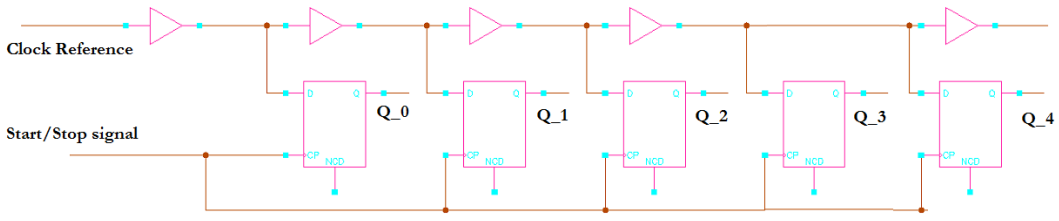


Figure 3.4: Bubble schematic example

Figure 3.4 shows five consecutive bits of the delay line. The clock reference is assumed to be between the third stage and the fourth stage having the correct sampled value as 1 1 1 0 0. The bits around the clock reference are assumed that they could be wrong, Q_2 and Q_3. It is not known if their values can be either 0 or 1. Therefore the following values can be sampled:

	Q_0	Q_1	Q_2	Q_3	Q_4	Output
Case 1:	1	1	0	0	0	2
Case 2:	1	1	0	1	0	Unknown
Case 3:	1	1	1	0	0	3
Case 4:	1	1	1	1	0	4

As it can be seen case 3 would be the right value to sample. Note that cases 1 and 4 only differs for right case in 1 bit; on the other hand, case 2 differs 2 bits in comparison with right case. Therefore, case 2 would be a bubble in the delay line since two consecutive bits are wrong sampled.

There are two main paths to reach a bubble:

- Metastability
- Sampling two stages of the delay line at the same time-interval due to mismatch variations and slow slope performance

In the design, bubble is not wanted and moreover it will be a restriction of the number of channels that the delay line can support as it will be seen in section 3.3. This feature can be noted as one reliable measure for the delay line.

3.1.3.1. Metastability

Metastability can lead the sampling flip-flop into an error as it can be seen in chapter 4. Therefore, it is necessary to check if at the time to do the sampling more than one flip-flop can be in metastable state as it can be seen in figure 3.5. To do so, it has to be checked if two consecutive slopes can be in the metastability window.

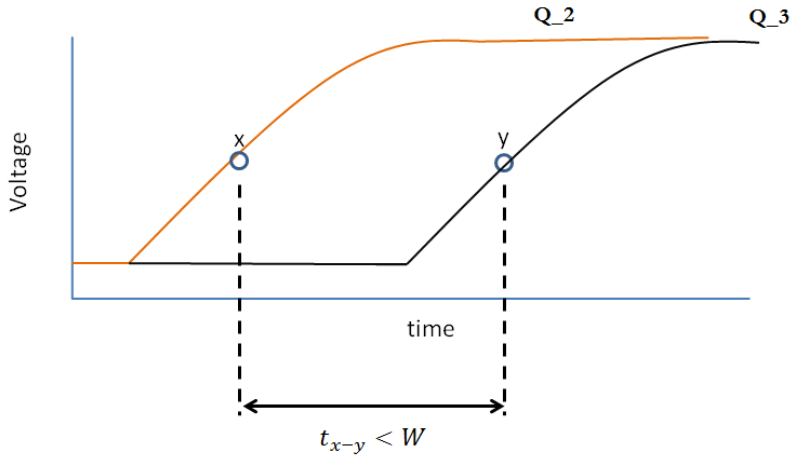


Figure 3.5: Time restriction due to metastability

If the time between two consecutive sampling of slopes, t_{x-y}, is less than the metastability window, W, it could mean that those flip-flops could be in metastable state at the time to sample the delay line. Note that points x and y in figure 3.5 represents the necessary mean voltage value at the data input of the flip-flop to change the output. As it is shown in section 4.2.3, the decision window will be the border to specify how many flip-flops may be entering metastability in one sampling stage.

3.1.3.2. Slow slope and mismatch variation

Flip-flop sampling time can vary due to mismatch variations. Even in the same chip two flip-flops can have different sampling times. As it was mentioned in section 3.2.2, there are two main parameters to determine this behavior: mean (μ) and standard deviation (σ). Taking figure 3.4 as a reference, we need to guarantee that two consecutive flip-flops are not overlapping its sampling time, Tb > Ta, as it can be seen figure 3.6. Three times standard deviation is considered as a restriction.

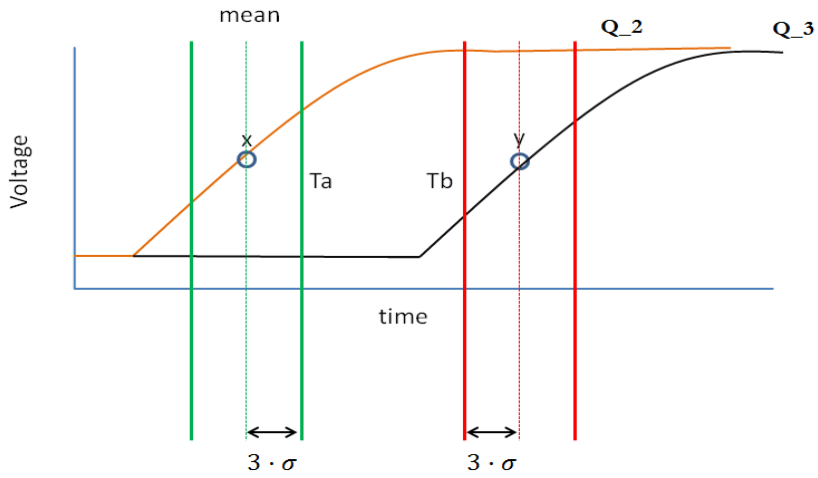


Figure 3.6: Time restrictions due to slow slope and mismatch variations

These time variations are produced by the different thresholds of the sampling flip-flops.

3.2. Schematic Design and guidelines

The different designs will be explained in this section in order to implement the delay line.

3.2.1. Basic delay line

The starting point of the design is a basic delay line consisting of two channels, which contains two start and stop signals. Then, it is thought that the sampling stage of the start pulses should be a shift register in order to reduce the output load of the delay line. The basic scheme of the delay line can be seen in figure 3.7 and 3.8. For the sake of simplicity, only one channel is shown in figure 3.8.

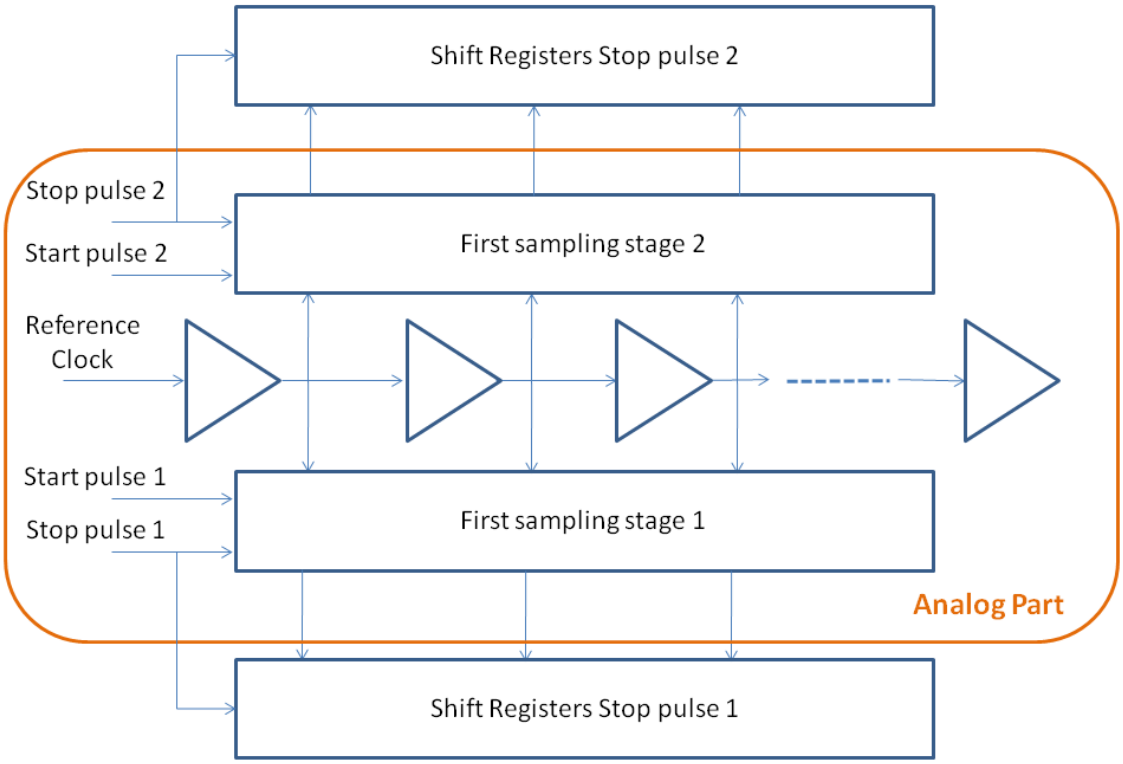


Figure 3.7: Basic delay line diagram

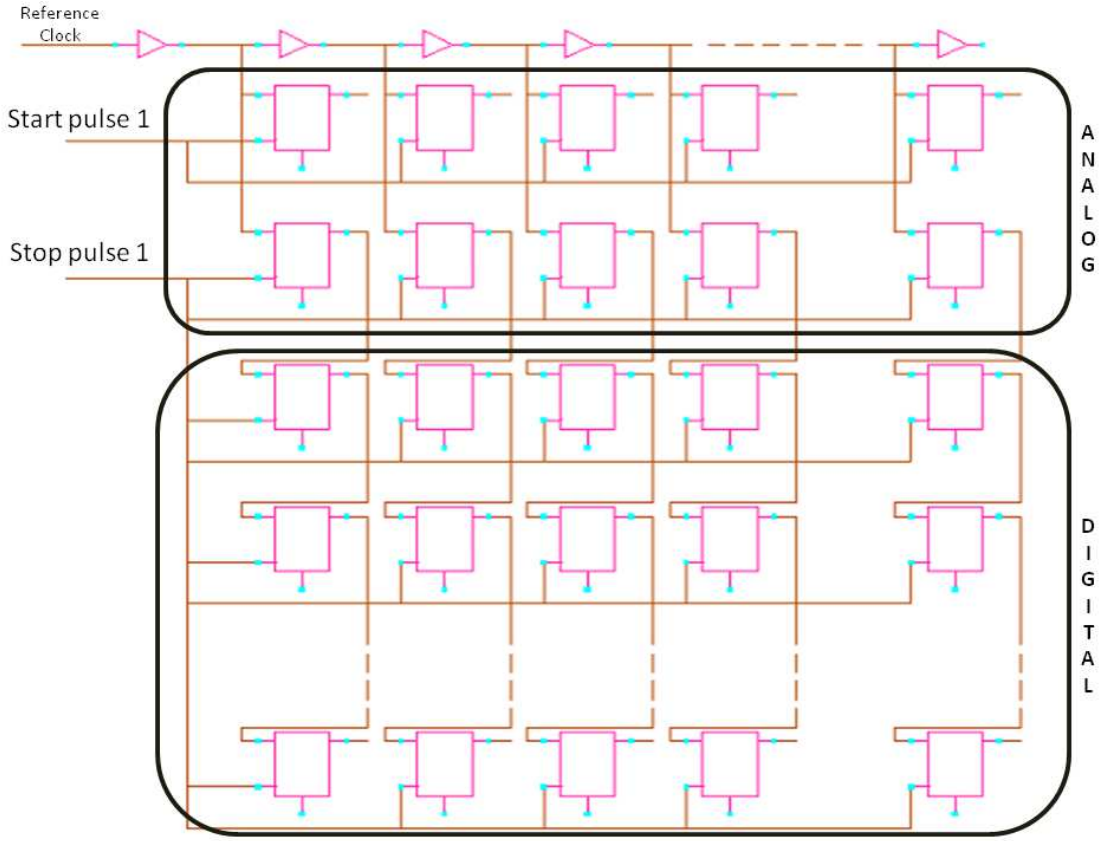


Figure 3.8: Basic fine measurement schematic

As figure 3.8 shows, it can be seen two different zones of the fine measurement part: analog and digital partition. Shift registers with digital design are decided to implement since it is more convenient in terms of chip development. Therefore, this work will be rather focused in the analog flow.
Analog flow consists mainly in the delay line and the first stage of sampling. As it was mentioned before, we have one start pulse and up to 10 stop pulses. Therefore, one single stage is necessary for detecting the start pulse and 10 stages to detect the stop pulse. The first stage of each signal will be developed in the analog as it can be seen in figure 3.8 and the remaining 9 stages of the shift registers will be designed in digital flow.
It is concluded that we have four loads connected to the delay line as each channel introduces two loads, start and stop sampling.

3.2.1.1. Basic delay line analysis

The delay element will be a simple buffer formed by two inverters of the same size. Relation between W_N and W_P of the inverters is wanted to maintain as equal as the technology provides. This step have been done in order to simplify the number of design variables and to keep the relation between widths. Therefore, W_P is decided to put in function of W_N.
Therefore, the width of the inverters will be multiple of a simple inverter.

The widths of the simple inverter are as follows:

$$W_N = 0{,}585\ \mu m \qquad W_P = 1{,}05\ \mu m$$

Thus, the relation between them is:

$$W_P = \frac{1{,}05\ \mu m}{0{,}585\ \mu m} \cdot W_N = 1{,}794 \cdot W_N \tag{3.5}$$

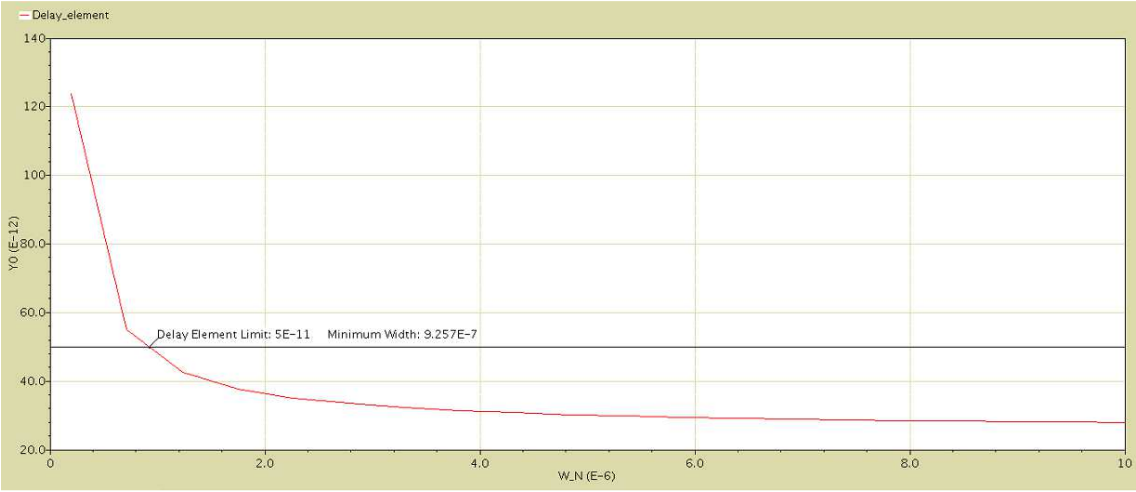


Figure 3.9: Delay element Vs transistor N width

Simulation varying the transistor size has been done in order to find the minimum necessary width to satisfy the requirement of 50 ps in the fine measurement with four loads connected to the delay line, two loads per channel. Figure 3.9 represents the delay element in front of the transistor size; then, the minimum width is $W_N = 0{,}925\ \mu m$ as it can be seen in figure 3.9.

Thus, the specification is fulfilled for almost any inverter width. We want to make the design suitable for more channels. Figure 3.10 shows a simulation taking into account more than 2 channels and thus the following widths for the inverter have been taken:

$$W_N = 2\ \mu m \qquad W_P = 3{,}59\ \mu m$$

These widths have been chosen in order to fulfill the specifications and to keep power consumption as less as possible. There is an important tradeoff between size and power consumption.

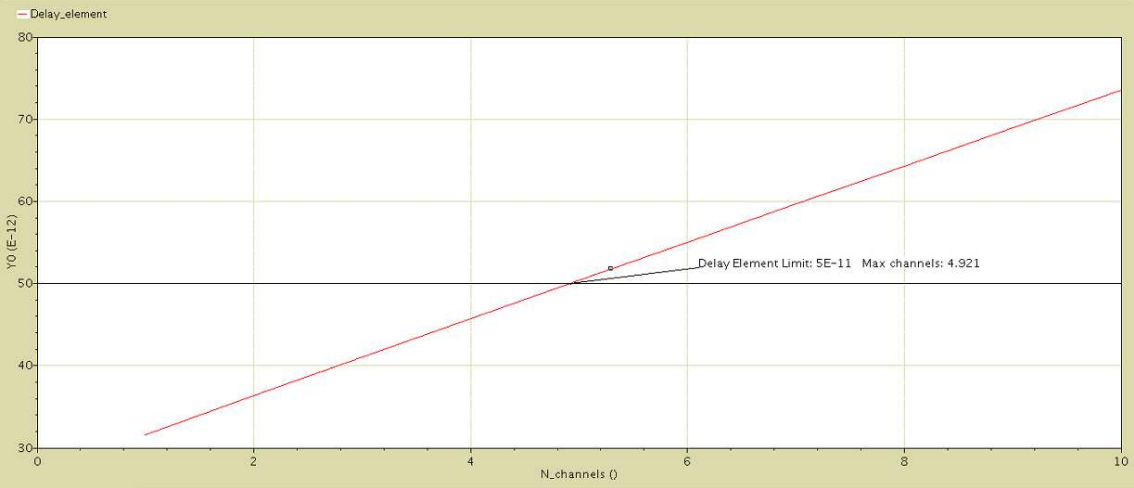


Figure 3.10: Delay element Vs number of channels

The delay increases as the number channels. Therefore there is a tight dependence between them. Different topologies have been considered in order to remove this correlation between delay element and number of channels and they are presented in the next section.
With this topology the maximum number of channels is $N_{CH} = 4{,}9$ as it can be seen in figure 3.10.

3.2.2. Proposed topology

The topology presented has the characteristic to remove correlation between delay element and number of channels. Thus, the design will fulfill the specifications in that work and in future works if more channels are needed.

The dependence between delay element and number of channels can be defined as output load dependence. As it was mentioned in 3.2.1, the time response of a device increases as the input capacitance in its output. Therefore, a path to split the delay elements of the channels is needed and it will keep the same input load in the delay line regardless the number of channels.
We have thought that by adding a decoupling inverter before the channels is a good way to separate delay element and number of channels. On the other hand if a decoupling inverter is added to the delay line it will increase the mismatch variation since another device is added to the design.
Same topology with different components has been thought and they are presented in the following sections.

3.2.2.1. Inverter with equal size topology

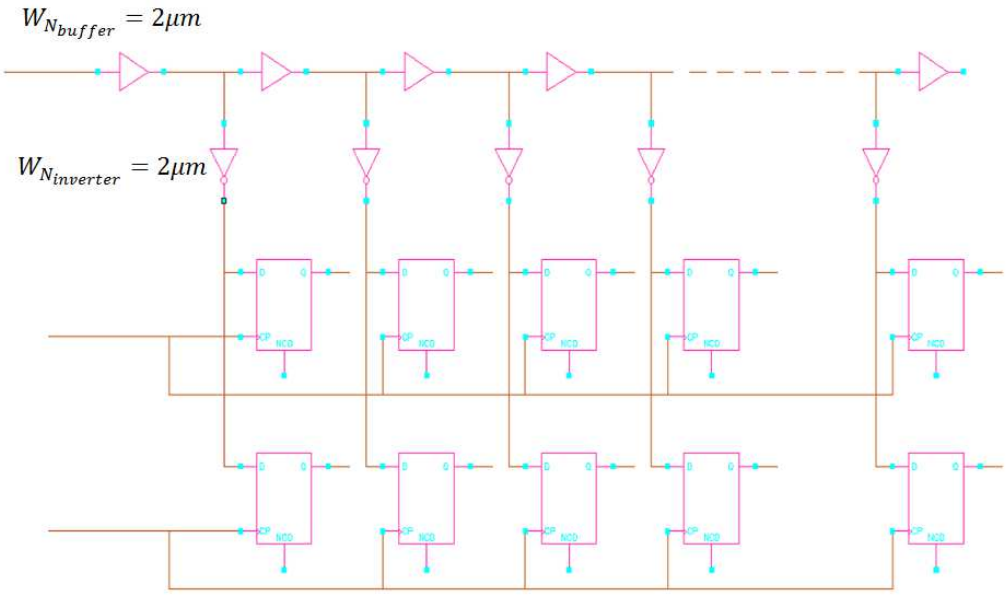


Figure 3.11: Topology with equal size inverters

This topology has been thought exclusively to remove the input load issue.

3.2.2.2. Inverter half size topology

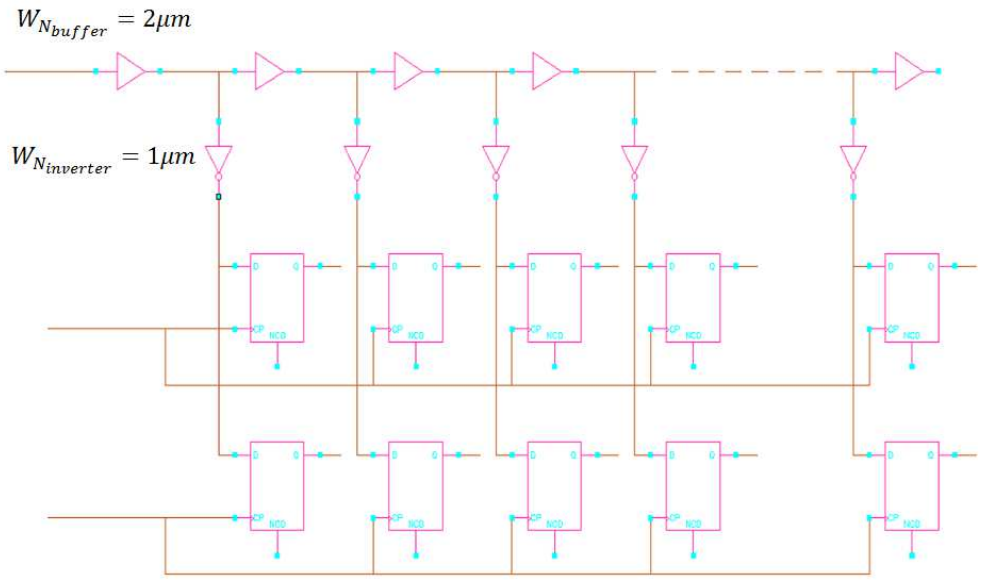


Figure 3.12: Topology with half size inverters

This topology has been done in order to reduce power consumption in comparison with the previous one. Nevertheless, some features can be degraded such as mismatch variations.

3.2.3. Topologies simulation overview

Montecarlo simulations have been done in order to characterize each topology as it can be seen in the next table.

					Montecarlo		
	Buffer		Stop	Channels	Delay_buffer (ps)	Delay_buffer (ps)	
	Wp	Wn			mean	st.deviation	%
No Inverters	3,59	2	0	1	31,55	0,43	1,37
	3,59	2	0	2	36,26	0,52	1,44
	3,59	2	0	4	45,58	0,71	1,56
	3,59	2	0	8	64,06	1,10	1,72

					Montecarlo		
	Buffer		Stop	Channels	Delay_buffer (ps)	Delay_buffer (ps)	
	Wp	Wn			mean	st.deviation	%
Inverters Equal size	3,59	2	0	1	32,76	0,48	1,48
	3,59	2	0	2	32,53	0,53	1,64
	3,59	2	0	4	32,32	0,66	2,04
	3,59	2	0	8	32,18	0,94	2,94

					Montecarlo		
	Buffer		Stop	Channels	Delay_buffer (ps)	Delay_buffer (ps)	
	Wp	Wn			mean	st.deviation	%
Inverters Half size	3,59	2	0	1	29,62	0,60	2,05
	3,59	2	0	2	29,50	0,82	2,79
	3,59	2	0	4	29,44	1,29	4,40
	3,59	2	0	8	29,36	2,32	7,93

Table 3.1: Features overview for three topologies

The purpose to remove correlation between delay element and number of channels is achieved by adding the decoupling inverter. Thus, the delay is kept without taking into account the number of channels. Therefore, it is clearly better option to choose the topology with a decoupling inverter rather than without an inverter. Besides, it will not be any restriction in the number of channels regarding the delay element, since the delay is kept quite steady with any number of channels. If the parameters are looked regarding the mismatch variations, it can be seen that the relation between mean and standard deviation is increased in case of the inverter half size as the channels increased. Furthermore, an issue regarding the trace of the slope at the output of the inverter can appear since the response time of the decoupling inverters depends on its output load (number of channels). Therefore, the behavior of the output slope in the inverter is needed to be studied for both components, half size and equal size decoupling inverter.

Mismatch variation and slow slope performance can lead into wrong sampling or increase the likelihood of metastability.

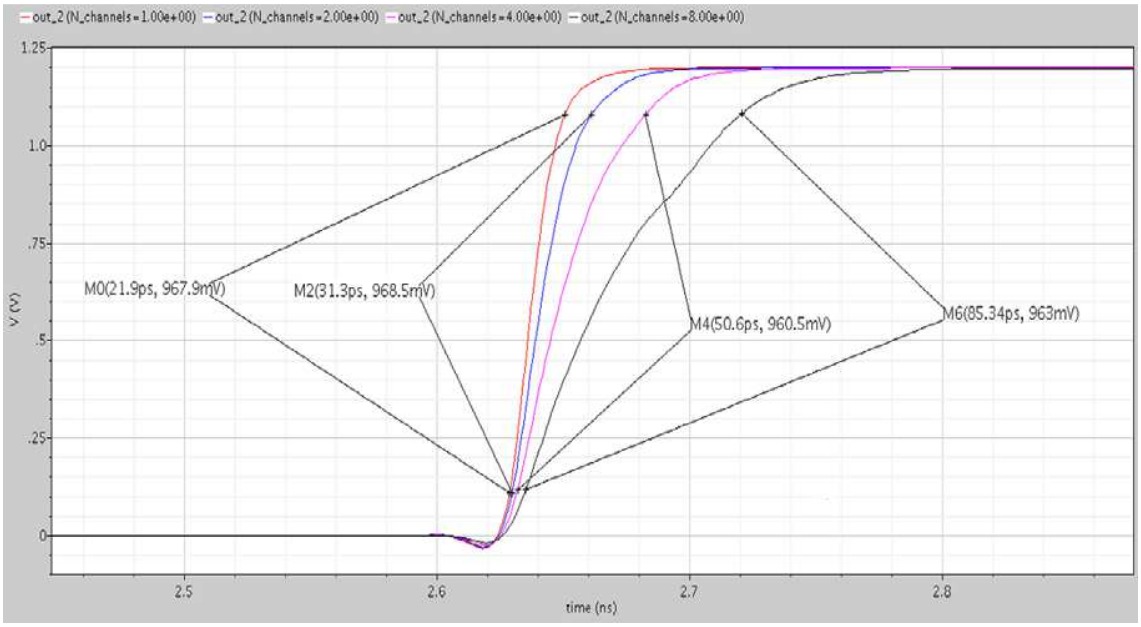


Figure 3.13: Output slope of the decoupling inverters with equal size for 1, 2, 4 and 8 channels

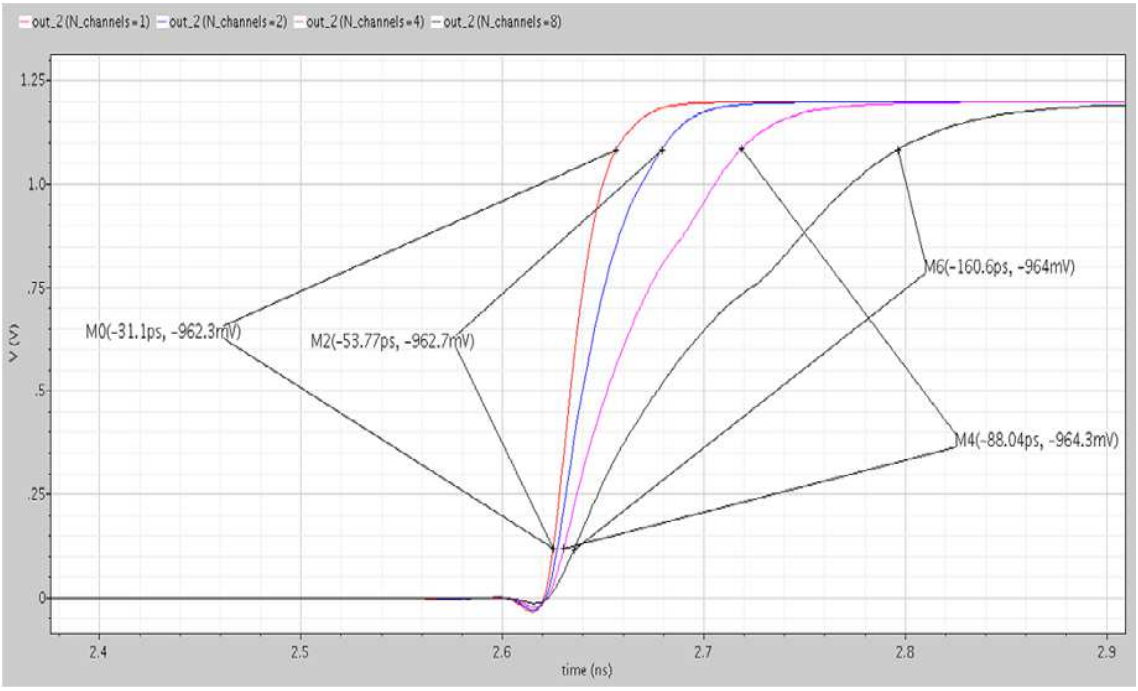


Figure 3.14: Output slope of the decoupling inverters with half size for 1, 2, 4 and 8 channels

Comparing the figures 3.13 and 3.14 it can be seen that the response time for the equal size inverters are better than the slope of the half size inverters which will improve the probability to enter into a metastable state as it will be explained in chapter 4.

It should be noted that there is a tradeoff among power consumption and performance of the topology features. In any case it has been chosen to give priority to the performance before the power consumption. Hence, the topology with the equal size decoupling inverter has been chosen to continue with the layout design.

3.3. Equal size inverter topology characterization

Main features of this topology are explained in this section. Proper simulations have been done in order to characterize it.

3.3.1. Output Slope

The response time of the decoupling inverter is important because it will be used to calculate metastability in chapter 4. This time requires calculating decision window (W) as well; and as it is shown in section 3.4.2, it will limit the maximum channels supported by the delay line.

Taking figure 3.13, the rising time of the decoupling inverter regarding two channels is $T_{slope} = 31{,}3\ ps$.

3.3.2. Flip-flop features

The features of the flip-flop FD2Q_SYNCHS have to be analyzed in order to know its behavior. The main features are:

- Minimum value in Data to switch Output
- Minimum value in clock to switch Data to Output

Those values are important in order to calculate its mismatch variation and other features such as metastability or bubble restrictions.

3.3.2.1. Minimum value in Data to switch Output

Figure 3.15 contains a montecarlo simulation about the minimum value at the data input of the flip-flop to change the output. Statistical values are extracted from the simulation as it is shown in figure 3.15.

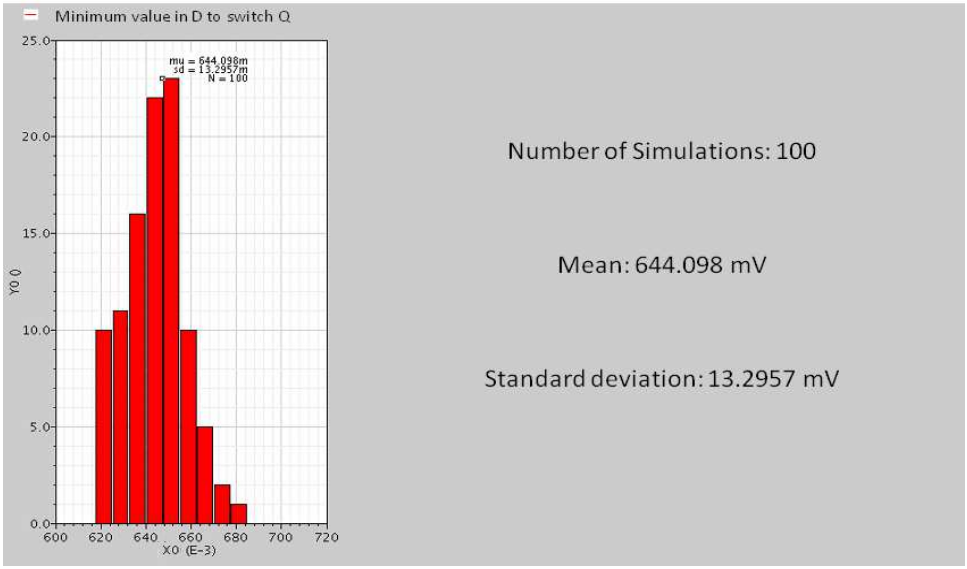


Figure 3.15: Statistical characterization for Data to switch Output

3.3.2.2. Minimum value in clock to switch Data to Output

Figure 3.16 shows the minimum value in the clock input of the flip-flop to change the output. Statistical values are shown in figure 3.16.

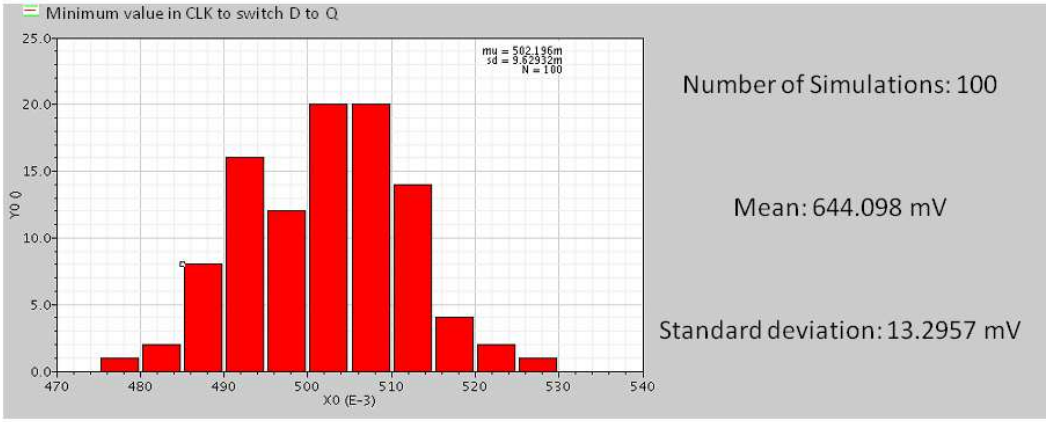


Figure 3.16: Statistical characterization for Clock to switch data to output

3.3.3. Bubble restrictions

As it was mentioned before there are two possible causes to reach a bubble: metastability or slow slope performance. In order to not have a bubble we need to fulfill the restrictions mentioned in sections 3.2.3.1 and 3.2.3.2.

Both are studied at the same time in the next figures where two consecutive inputs of the flip-flops are shown for different number of channels:

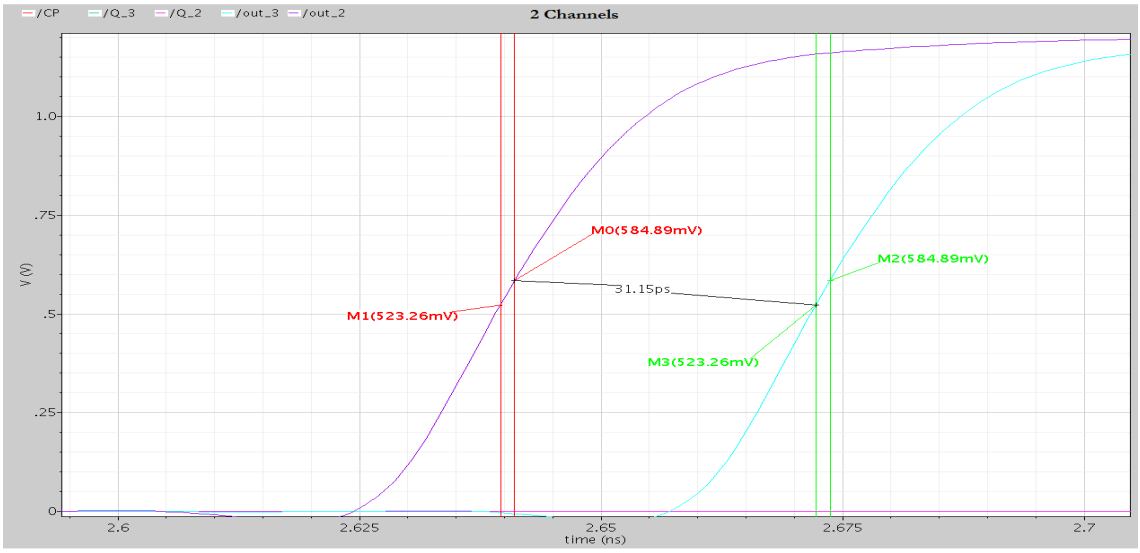


Figure 3.17: Bubble measurements for 2 channels

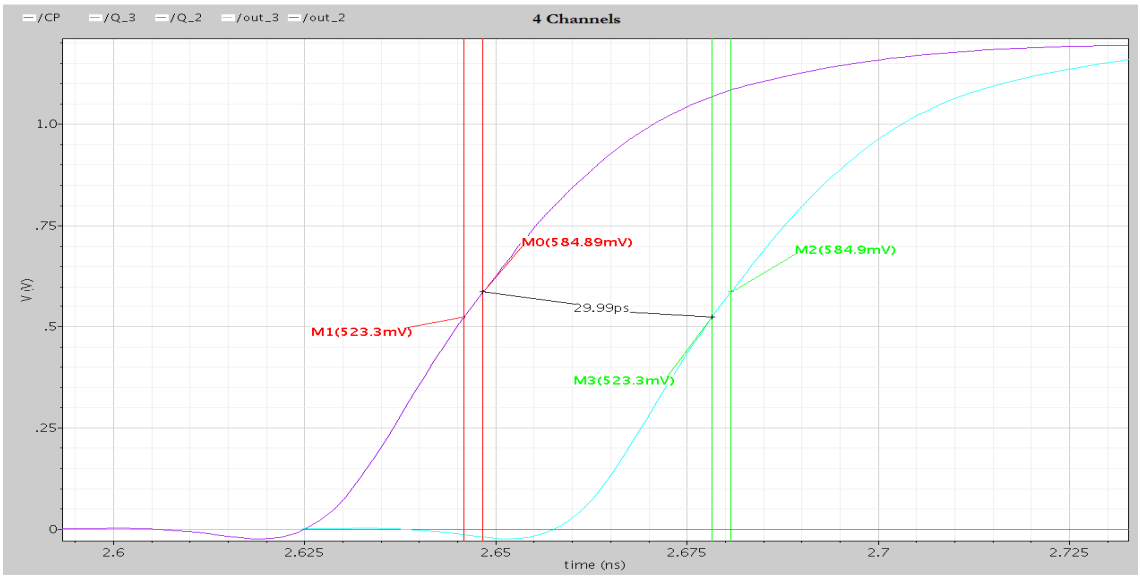


Figure 3.18: Bubble measurements for 4 channels

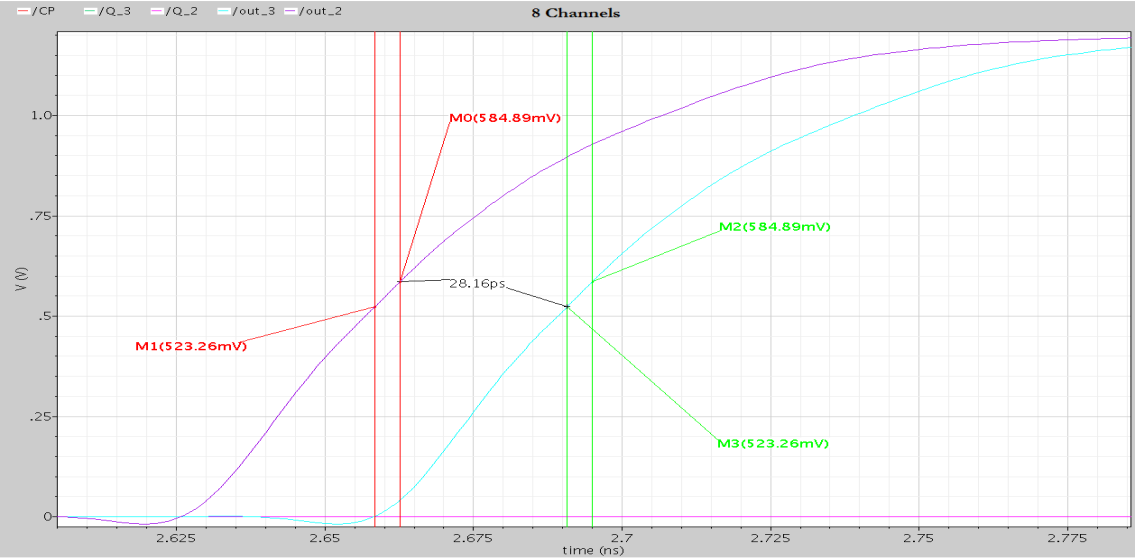


Figure 3.19: Bubble measurements for 8 channels

Red and green voltage values represent the $\mu \pm 3\sigma$ sampling voltage of the flip-flops regarding two consecutives slopes of the delay line. The worst case is considered for the metastability window taking as switching values the $\mu + 3\sigma$ and $\mu - 3\sigma$ of the first and second slope, respectively. Therefore, time between these voltage values limits the decision window restriction.

The slow slope constraint is accomplished widely since there is a wide distance before the slopes can overlap. The minimum decision window time required to not have bubble is 23,52 ps as it is shown in chapter 4. Any time fewer than 23,52 ps can lead into a bubble error.

We want to know how many channels are possible to implement without violating the window decision time constraint. A parametric simulation has been done comparing the available time between slopes against the number of channels implemented.

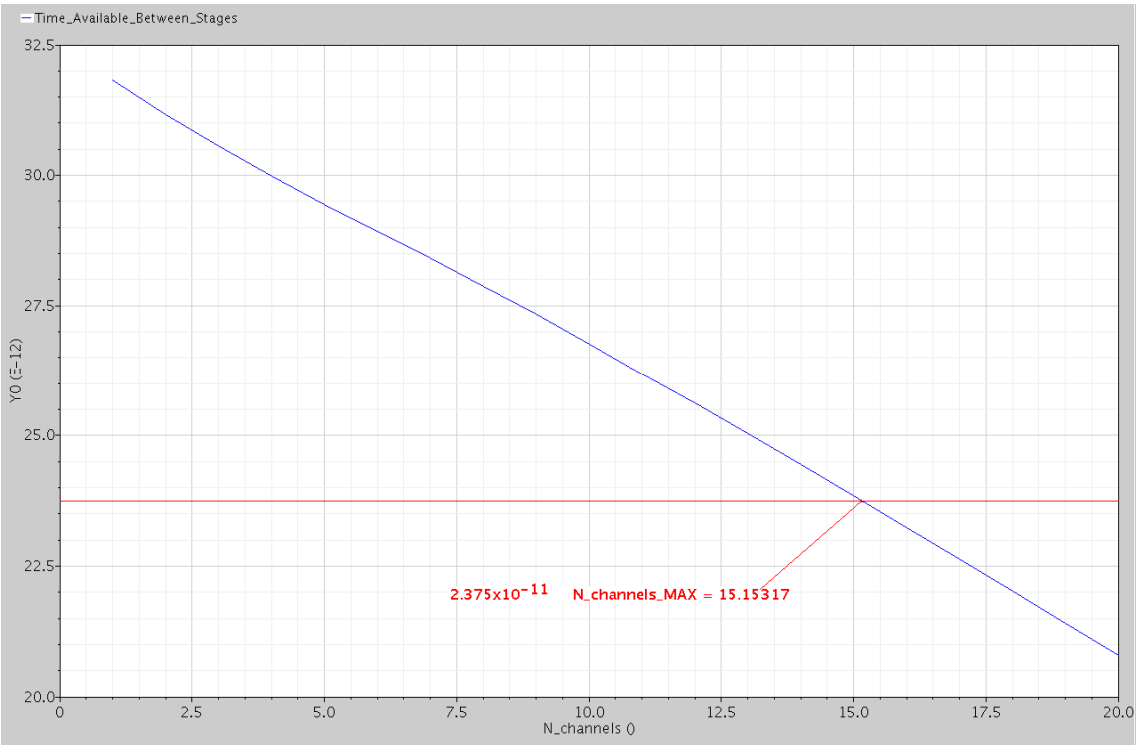


Figure 3.20: Window decision time available Vs number of channels

The maximum number of channels that can be implemented without having any chance to get a bubble error is 15. Hence, there is no chance to have bubble error in our system prototype since two channels are implemented and it can be safely extended up to 15 channels.

3.3.4. Delay element

Montecarlo simulations have been done in order to characterize better the delay element. Besides, this simulation will show if the delay element is still less than 35.35 ps in case of having worst corner and mismatch variations.

	Delay_buffer (ps)	Delay_buffer (ps)	
Case	mean	st.deviation	%
Best	28,51	0,46	1,63
Typical	32,65	0,57	1,76
Worst	37,21	0,69	1,86

Table 3.2: Delay element Montecarlo simulation

As it can be seen in table 3.2 in best and typical case is fulfill the requirement of 35.35 ps; however, in worst case it is not accomplished.

CHAPTER 4

4. METASTABILITY ISSUES

In this chapter, the concept of metastability is briefly introduced. The main objective of this chapter is to quantize the susceptibility of the flip-flop to reach metastable state. Simulations have been done through Cadence spectre simulator and characterization of the flip-flop FD2Q_SYNCHS is done regarding metastability.

4.1. Theoretical background

Metastable state in electronics means that the output remains in an uncertain state and the slightest disturbance will make the output high or low (figure 4.1); it normally happens when a feedback takes part of the circuitry. Regarding flip-flops or latches, it can be said that metastability means indecision in terms of the output; it could be either 1 or 0.

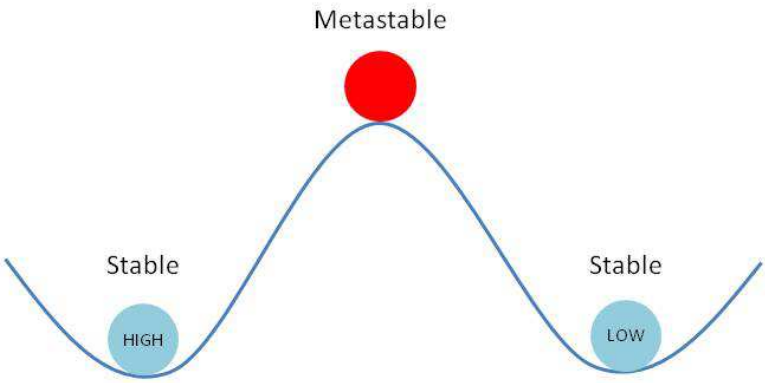


Figure 4.1: Mechanical metastability

Logic devices have to carry out the specifications regarding their timing constraints; thus, if the constraints are not satisfied the logic levels of the logic devices could be illegal. Furthermore, another symptom of metastability is the increase of the clock-to-output time and it can turn on a wrong behavior of the system.

The main objective is to quantize the susceptibility of the flip-flop to reach metastable state with a probabilistic equation. Hence, it will be known the likelihood to enter metastability and the circuit will be characterized [7].

In figure 4.2 is shown a theoretical single-stage of the metastability resolution time for a flip-flop. Also, the main concepts of the measurements are shown and they will be described afterwards.

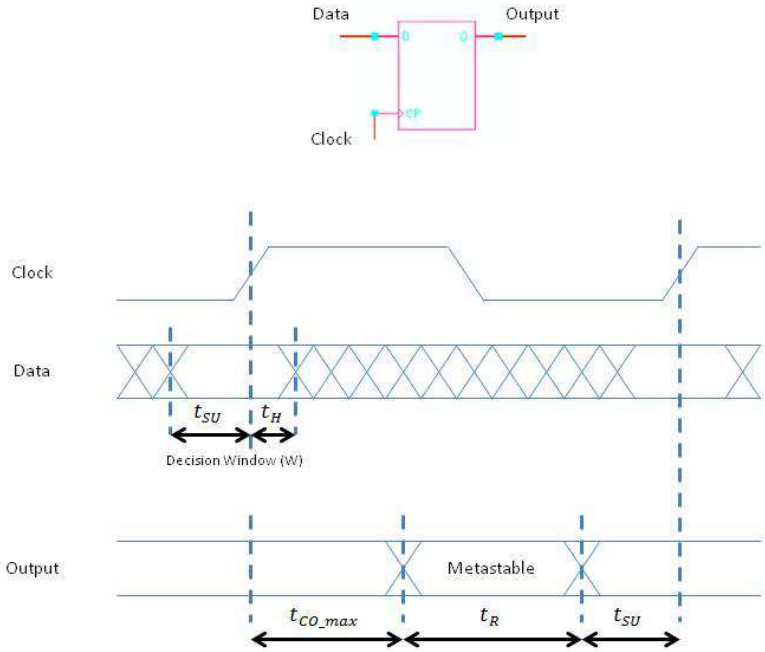


Figure 4.2: Mestability one-stage flip-flop

- t_{SU}: Data setup time
- t_H: Data hold time
- Decision window (W): Input data is asynchronous to the clock. Thus, the arrival time of data is not known
- t_{CO_max}: Maximum clock to output delay
- t_R: If the input data appears in W, the output could enter into a metastable state. This metastable state will remain until the device settles a logic value, either high or low. This time to resolve metastable state is called resolution time.

A simple example of real metastability simulation is shown in figure 4.3. As it can be seen a metastable state is reached, and also waveforms are shown. Simulation have been achieved by matching the change in the data with the clock switching; then, a parametrical simulation varying slightly the clock switching turns into metastable state in the output .It can be observed that during a certain period of time the output level

of the latch is between 1 and 0, until it goes to a legal level; thus, it takes some time until reach a legal voltage level and the clock-to-output time is increased.

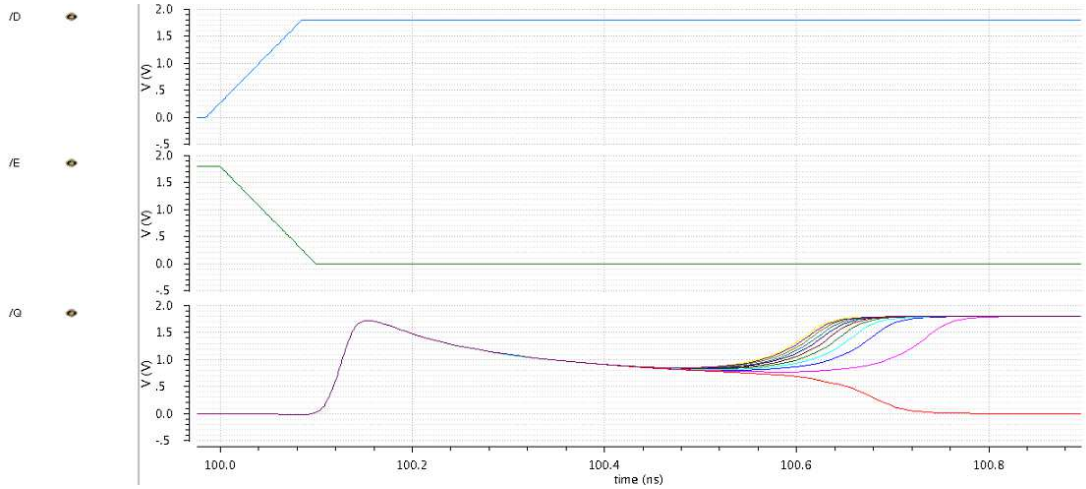


Figure 4.3: Metastability example

4.2. Metastability parameters

The measurements that have to be done for the purpose to characterize metastability are shown in this section; plus, the different metastability parameters will be explained step by step.

4.2.1. Resolution time (t_R)

The output of a flip-flop will be sampled on the next clock event, the maximum resolution time is:

$$t_R = T_{clock} - t_{CO\_max} - t_{SU} \tag{4.1}$$

Resolution time is the time that the output of a flip-flop has to recover into a legal value before the setup time of the next flip-flop sampling. The equation can be extracted from figure 4.2.

4.2.2. Resolving time constant (τ)

The expression that describes the likelihood of a metastable event lasting longer than some time t is:

$$P = e^{\frac{-t}{\tau}} \tag{4.2}$$

Several methods to find τ have been done through simulations [6] or with real test methods evolving signals generators and digitals oscilloscopes [8] [9].
In this work, method presented in [6] has been followed because the real device is not available to perform the measurements.

The path until reach metastability is described in [6] and the measures that have to be taken in order to estimate τ.

Figure 4.4 and 4.5 shows a simple example of feedback among inverters and its voltage versus time. As it can be seen the circuit starts in metastable state and a slightly difference of voltage (V_o) is applied after a certain time (t_1) to allow the circuit resolve and thus, exit metastability. However, the behavior of the circuit does not change when V_o is applied at t_1, but the voltage of the two nodes A and B requires a time until reach a legal level as figure 4.5 shows.

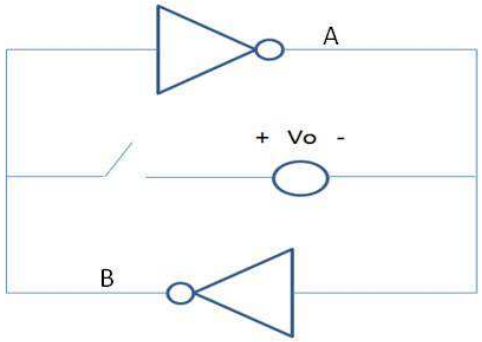


Figure 4.4: Circuit feedback of two inverters

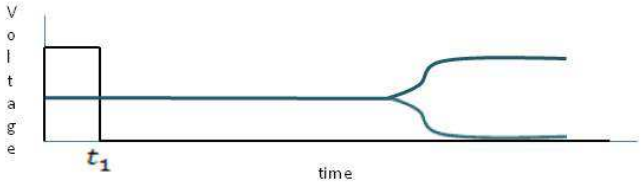


Figure 4.5: Voltage of the two nodes A and B

As it can be seen in figure 4.5 the voltage charts do not change really fast. Nevertheless, if the logarithm of the voltage difference between the two nodes A and B (figure 4.6) is plotted we can see an exponential growth of the voltage difference. Figure 4.6 allows a simple estimation of the resolving time constant τ.

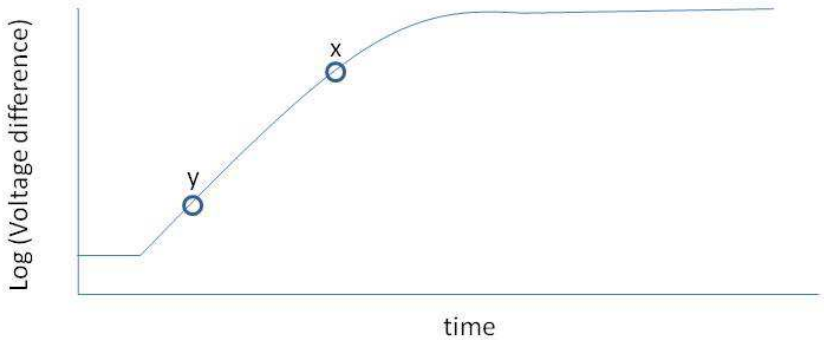


Figure 4.6: Log of the voltage difference of the nodes A and B

$$\tau = \frac{t_x - t_y}{\ln\left(\frac{V_x}{V_y}\right)} \tag{4.3}$$

Where t_x, t_y, V_x and V_y are taken of the logarithm graphic of the voltage different of the two nodes involved in the circuit feedback.

It should be noted that several factors affects at τ. Mismatch and process variations, low supply voltage or just temperature variation could vary the value of τ in some orders of magnitude.

4.2.3. Decision window (W)

The decision window is a time period where if the input D appears at the input, the flip-flop could sample it wrong. Also this time period is known as metastability window.
This wrong sampling entails an increasing of the clock to output delay (t_{CO}) as it is shown in figure 4.7.

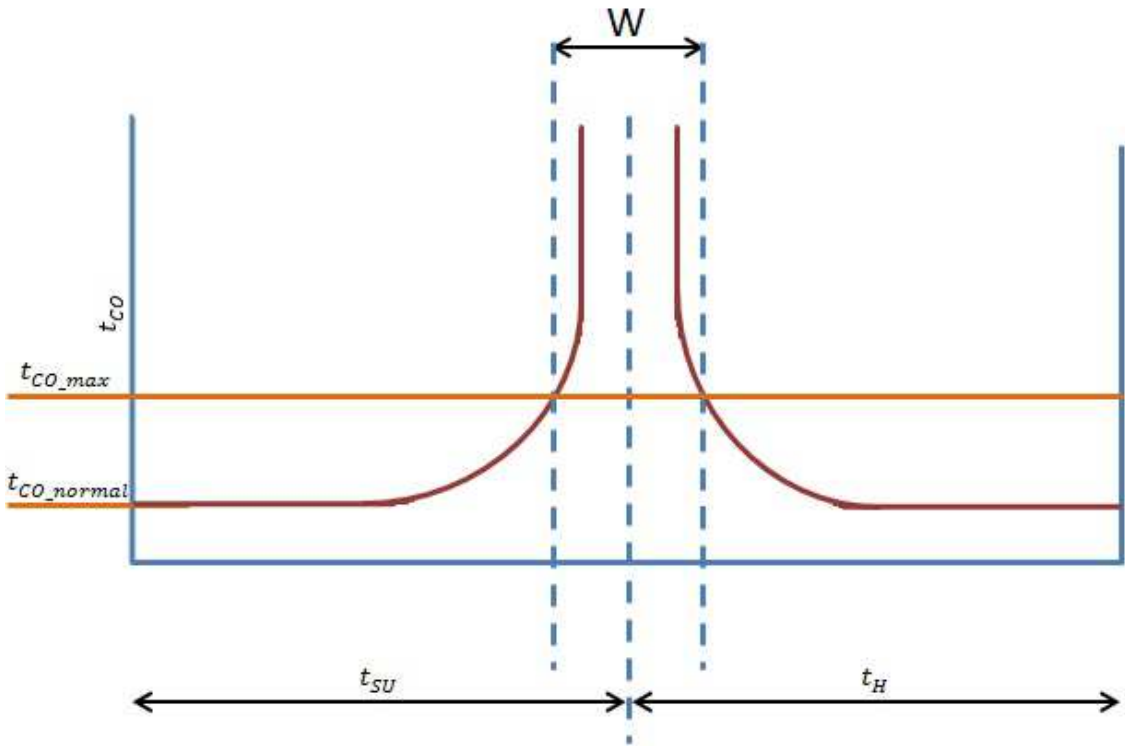


Figure 4.7: Decision Window

In figure 4.7 is measured the t_{CO} versus data to clock delay. As it was mentioned before, only when the input data violates the setup or hold time the flip-flop is entering in this decision window and it can be seen by measuring the t_{CO}. As far as the setup/hold time is violated, t_{CO} increases.
t_{CO_normal} makes reference at the clock to output delay time when the input data is sampled correctly. Therefore, when the t_{CO} measured is longer than t_{CO_max}, the flip-flop is considered to be in metastable state.

4.2.4. Mean time between failures (MTBF)

Once all the parameters shown in previous sections are known, the characterization of the metastability in the flip-flop can be done.

When the external data is uncorrelated with the clock, it is assumed the data comes uniformly over the clock period T. Then, the probability that data come inside the decision window in a clock period is:

$$P_M = W \cdot f_{clock} \tag{4.4}$$

If the input data arrives with a given frequency f_{data}, the probability per unit time becomes:

$$P_M = W \cdot f_{clock} \cdot f_{data} \tag{4.5}$$

The likelihood of a metastable event lasting longer than t_R is:

$$P = e^{\frac{-t_R}{\tau}} \tag{4.6}$$

The Metastability failure rate can be determined as follows:

$$Failure\ rate = P_M \cdot P = W \cdot f_{clock} \cdot f_{data} \cdot e^{\frac{-t_R}{\tau}} \tag{4.7}$$

Equation (4.8) defines the rate of a flip-flop to reach metastable state at a certain time after the clock.

This failure rate is commonly converted into mean time between failures (MTBF):

$$MTBF = \frac{1}{Failure\ rate} = \frac{e^{\frac{t_R}{\tau}}}{W \cdot f_{clock} \cdot f_{data}} \tag{4.8}$$

4.3. Simulations and results

Several simulations have been done to find the MTBF in this section. These simulations have been done for flip-flop FD2Q_SYNCHS belonging to ST (130 nm) which have been selected for the final architecture.

4.3.1. Resolution time (t_R)

The parameters to calculate $t_R$can be extracted from the data sheet of the flip-flop [10] and the clock frequency is the frequency of the stop pulses train:

$$t_R = 500\,ps - 128{,}36\,ps - 59ps = 312{,}64\,ps$$

Where t_{CO_max} and t_{SU} have been calculated from the following expressions:

FD2Q_SYNCHS Propagation Delay
nanoSeconds, as a function of C (load in pF) and Tr (input transition time in nS)

Path	Event	Best 1.32V -40C	Worst 1.08V 125C	Nominal 1.2V 25C
CP-Q	CP_Q (fall)	0.087 + 0.066*Tr + 1.089*C	0.204 + 0.085*Tr + 1.916*C	0.131 + 0.067*Tr + 1.358*C
CP-Q	CP_Q (rise)	0.076 + 0.076*Tr + 1.191*C	0.179 + 0.092*Tr + 2.746*C	0.113 + 0.075*Tr + 1.828*C
NCD-Q	NCD_Q (fall)	0.071 + 0.090*Tr + 1.102*C	0.160 + 0.112*Tr + 1.914*C	0.105 + 0.091*Tr + 1.355*C

FD2Q_SYNCHS Timing Constraints
nanoSeconds, as a function of Tr (input transition time in nS)

Constraint	Best 1.32V -40C	Worst 1.08V 125C	Nominal 1.2V 25C
D_CP_HOLD (fall)	0.017 + 0.055*Tr(CP)	0.027 + 0.074*Tr(CP)	0.005 + 0.060*Tr(CP)
D_CP_HOLD (rise)	0.005	0.003 + 0.007*Tr(CP)	0.005
D_CP_SETUP (fall)	0.022 - 0.055*Tr(CP) + 0.207*Tr(D)	0.045 - 0.070*Tr(CP) + 0.191*Tr(D)	0.066 - 0.062*Tr(CP) + 0.196*Tr(D)
D_CP_SETUP (rise)	0.030 - 0.020*Tr(CP) + 0.142*Tr(D)	0.079 - 0.041*Tr(CP) + 0.155*Tr(D)	0.058 - 0.032*Tr(CP) + 0.136*Tr(D)
NCD_CP_RECOVERY (fall)	0.006 + 0.332*Tr(NCD)	0.016 + 0.350*Tr(NCD)	0.003 + 0.345*Tr(NCD)
NCD_CP_REMOVAL (fall)	0.063 + 0.087*Tr(CP)	0.145 + 0.100*Tr(CP)	0.080 + 0.087*Tr(CP)
Pulse Width High CP	0.035	0.075	0.055
Pulse Width High NCD	0.045	0.240	0.150
Pulse Width Low CP	0.055	0.155	0.100

Figure 4.8: FD2Q_SYNCHS Datasheet

Where $T_R(CP)$ and $T_R(D)$ are the transition time for the clock and data input, respectively.

$T_R(CP) = 100$ ps

$T_R(D) = 31{,}3$ ps

Variable C makes reference at the load capacitance at the output of the flip-flop. Following the designed architecture, the output load capacitance is the capacitance presents in the data input of the next flip-flop. This value can be extracted also from the datasheet of the device:

Capacitance
picoFarads

Cell	Property	Best 1.32V -40C	Worst 1.08V 125C	Nominal 1.2V 25C
FD2Q_SYNCHS	NCD Input Cap.	0.0026	0.0023	0.0024
FD2Q_SYNCHS	CP Input Cap.	0.0049	0.0044	0.0046
FD2Q_SYNCHS	Q Max Load	0.160	0.160	0.160
FD2Q_SYNCHS	D Input Cap.	0.0046	0.0042	0.0043

Figure 4.9: Load capacitance in FD2Q_SYNCHS

Next equations from figure 4.8 show the calculation of t_{CO_max} and t_{SU} :

$$t_{CO\_max} = 0{,}113 + 0{,}075 \cdot \mathrm{T_R} + 1{,}828 \cdot \mathrm{C} = 0{,}113 + 0{,}075 \cdot 0{,}1 + 1{,}828 \cdot 0{,}0043 = 0{,}12836\ ns$$

$$t_{SU} = 0{,}058 - 0{,}032 \cdot \mathrm{T_{R\ clock}} + 0{,}136 \cdot \mathrm{T_{R\ Data}} = 0{,}058 - 0{,}032 * 0{,}1 + 0{,}136 * 0{,}0313 = 0{,}059\ ns$$

4.3.2. Resolving time constant (τ)

τ is calculated taking the two nodes involved in the internal feedback of the flip-flop regarding the master latch, as it was explained in section 4.2.2.
In a right performance of the flip-flop, these two nodes should be either high or low voltage levels; besides they are complementary, the two nodes cannot be the same level at the same time, except when the device has entered metastability.
Hence, the voltage difference of these two nodes can show how the latch resolves the metastability as it is shown in figures 4.10 and 4.11.

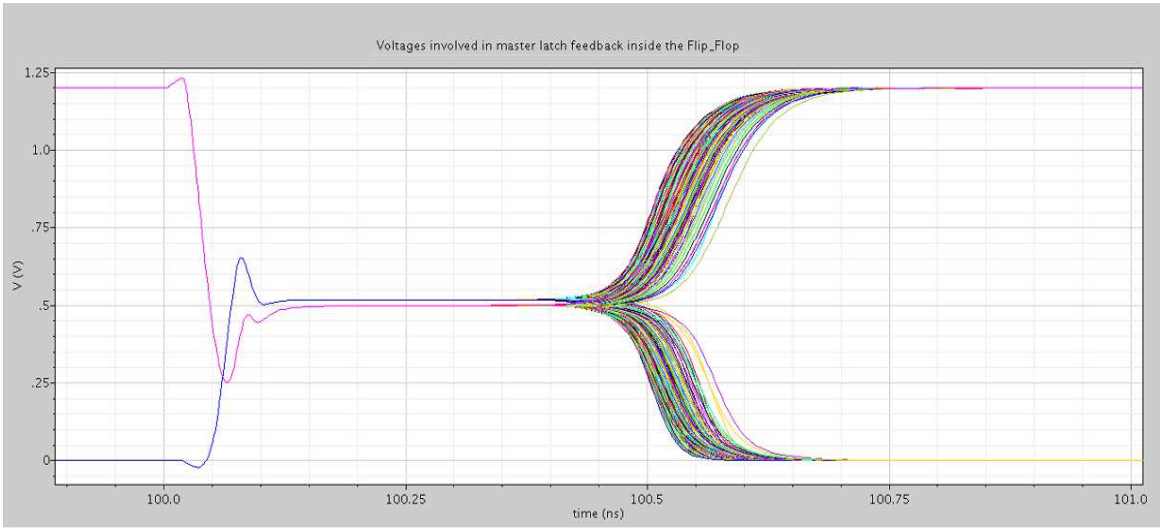


Figure 4.10: Voltage of the two nodes involved in FD2Q_SYNCHS. The flip-flop gets into metastable event until it resolves

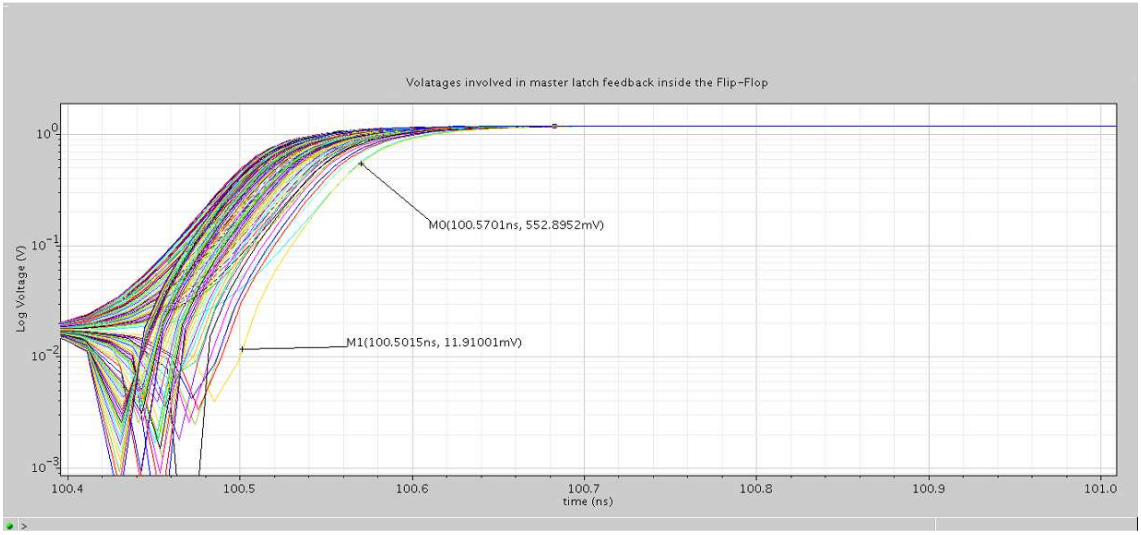


Figure 4.11: Voltage log difference of the two nodes involved in FD2Q_SYNCHS

Hence, the results of τ regarding the FD2Q_SYNCHS flip-flop in 130 nm are shown in table 4.1.

The calculation has been done following equation (4.3). Hence, τ of FD2Q_SYNCHS flip-flop is 17,87 ps

4.3.3. Standard flip-flop Vs FD2Q_SYNCHS flip-flop

The path until reach the metastability parameter for the standard flip-flop is analogous to the FD2Q_SYNCHS flip-flop [20]. Table 4.1 shows the comparison between them.

Features	Flip-Flop	
	Standard	FD2Q_SYNCHS
Load Capacitance(pF)	0,0022	0,0043
Maximum clock to output delay (ps)	123,45	128,36
Setup time (ps)	29,25	59,00
Resolution time(ps)	347,30	312,64
Resolving time constant (τ)(ps)	51,07	17,87
Area(μm^2)	28,24	42,36

Table 4.1: Comparison between standard and FD2Q_SYNCHS flip-flop

FD2Q_SYNCHS is better in terms of speed although its area is almost twice bigger than the standard flip-flop. Hence, FD2Q_SYNCHS is chosen for the application since its area can be afforded and it is worth due to its speed performance.

4.3.4. Decision window (W)

Simulations have been done in order to show the decision window for the FD2Q_SYNCHS.

Figure 4.12: Decision window for FD2Q_SYNCHS

As it can be seen in figure 4.12 the decision window is 23,52 ps.

4.3.5. Mean time between failures (MTBF)

Now that all the parameters are known the MTBF can be calculated from equation (4.8):

$$MTBF = \frac{e^{\frac{t_R}{\tau}}}{W \cdot f_{clock} \cdot f_{data}} = \frac{e^{\frac{312{,}64p}{17{,}8749p}}}{23{,}52p \cdot 2G \cdot 400M} = 2{,}096 \text{ seconds}$$

It should be noted that this value is for the first sampling stage of the shift register. In section 4.3.6 is shown the MTBF of the next stages involved in the design.

4.3.6. Mean time between failures (MTBF) in architecture

The shift register perform as a typical synchronization scheme and the MTBF of each flip-flop increases as the stage of the shift register increase. It can be seen the MTBF of all the FD2Q_SYNCHS flip-flops which composes the shift register in the followings calculations:

$$MTBF_1 = \ 2{,}076 \text{ seconds}$$

$$MTBF_2 = \frac{e^{\frac{t_R}{\tau}}}{W \cdot f_{clock}} \cdot MTBF_1 = \frac{e^{\frac{312{,}64p}{17{,}8749p}}}{23{,}52p \cdot 2G} \cdot 2{,}076 = 1{,}72 \cdot 10^9 \ sec = 54{,}66 \ years$$

$$MTBF_3 = \frac{e^{\frac{t_R}{\tau}}}{W \cdot f_{clock}} \cdot MTBF_2 = 1{,}428 \cdot 10^{18} \ seconds = 4{,}52 \cdot 10^{10} \ years$$

The values of $MTBF_2$ and $MTBF_3$ are quite safe since the universe is believed to be 10^{10} years old. Therefore, it is not worth to go further in the calculation of the $MTBF$ in the next shift register stages.

CHAPTER 5

5. LAYOUT DESIGN

Once the basic architecture of the delay is known, it is time to go into layout design and post layout simulation to implement the architecture to send the design to the foundry to be implemented. The layout step in the design is very important since it is adjusted more to reality than schematic simulations. Post layout simulation takes into account all the parasitic resistance and capacitors added by the wires, pins and other issues.
Guidelines for the post layout simulation are shown in this chapter. First the main features to take into account at the time to analyze the delay line in layout are briefly introduced. The second stage is to explain step by step the guideline that has been followed. It should be noted that there are several paths to implement the delay line through layout; thus, we want to show the evolution of the layout design and discuss all the steps that have been done until reach the final layout.

5.1. Quality of the Layout

There are several features to measure the reliability and quality of the time to digital converters. The common error sources [11] that can affect at the performance of the delay line are the followings:

- Stochastic errors
- Systematic errors

Stochastic errors make reference at the errors that can be characterized by statistical measures such as standard deviation. Stochastic errors are divided in two groups: noise effects and quantization errors.
Systematic errors mean errors that appear always at the same time with the same value during the measurements.

In this work is focused on systematic error in order to measure the error of the delay line. Besides, noise effects are irrelevant in front of quantization errors and it is out of this work scope.
Two mainly systematic errors have been studied to measure the features of the time to digital converter:

- Integral non-linearity (INL)
- Differential non-linearity (DNL)

They are mainly focused on the sampling part of the delay line and the analog digital conversion since the other important features are involved in the schematic design as it can be seen in chapter 3 and 4. INL and DNL will give us the systematic error produced by the layout design issues such as voltage drop or drive current in the metal stripes.
In order to understand INL and DNL, a theoretical background is introduced in the following sections.

It should be noted that there are several paths to minimize the effect of systematic errors [12] [13] but it requires complex data processing or specific circuit solutions to the TDC which can increase the chip size and hence, the price.

5.1.1. Integral Non-Linearity (INL)

Integral non linearity is the deviation of the transfer function values over a straight line. This straight line can be defined in several paths; nevertheless, the usual path is taking the first and the last point as a reference.
The difference between the ideal voltage levels at which code transitions happen and the actual voltage is the INL error.

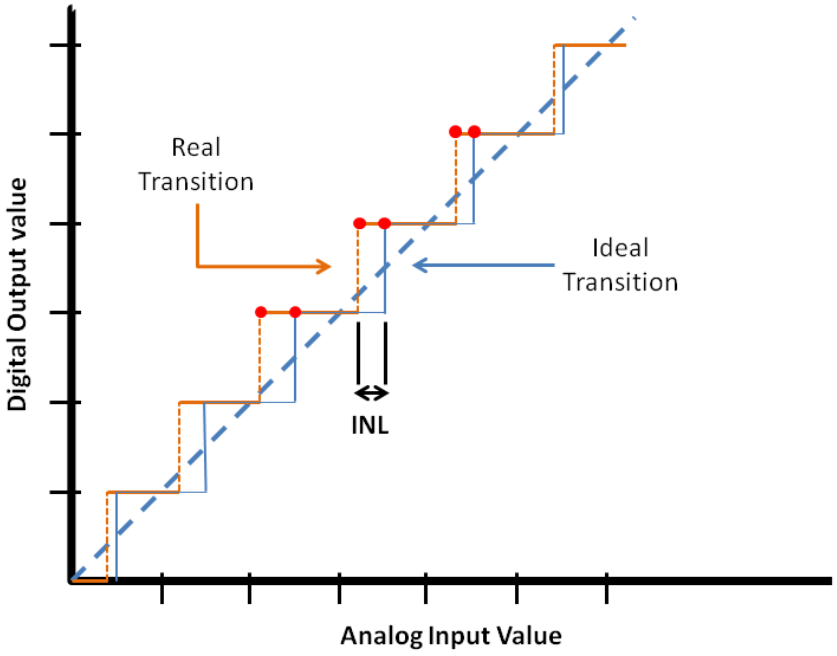


Figure 5.1: Integral non-linearity

As it can be seen in figure 5.1 the reference line (blue straight line) can be considered as the ideal transition value to have perfect performance. The ideal transition is not corresponding with the real transition and the difference between those two points is the integral non-linearity. It is measured in LSB (Least Significant bit).

5.1.2. Differential Non-Linearity (DNL)

Differential non-linearity is the difference between the nominal voltage to generate a bit change at the output and the real variation that must happen. The voltage difference between each code transition should be equal to one LSB as it is shown in figure 5.2. Thus, deviation of each code from an LSB is measured as DNL.

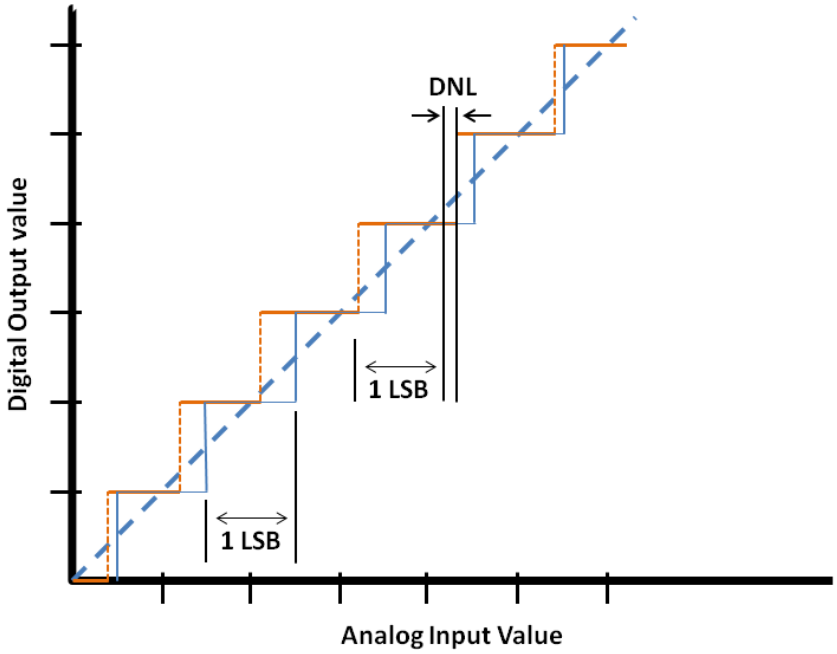


Figure 5.2: Differential non-linearity

The ideal case would be when a change at the input voltage means a change at the output digital as it is expected; otherwise, if the output digital changes within another input voltage, not being the expected one, it can result in differential non-linearity. At least this error should be less than 1 LSB to not generate possible unknown values at the output digital. As INL, DNL is measured in LSB as well.

5.2. Layout design and post layout simulation

The followed path until reach the final layout is shown in this section. It should be noted that not all the steps are commented in this section since during the design stage of the layout there were a lot of changes in the design. We want to show the main steps that have been done in order to achieve a final layout.

5.2.1. Number of stages in the delay line

We need to calculate how many delay elements are needed to implement the layout of the delay line. For the purpose to do that, the delay line can shift a whole period of the reference clock. It means that the sum of the delay elements has to be at least equal to the clock reference period.
Therefore, the delay element is necessary to calculate as much accurate as possible to determine the worst case of the delay line and thus implement the delay line with that number of stages.

A montecarlo simulation has been done in order to get the best, typical and worst case for the delay element. Once the delay element is known, the number of stages can be calculated following the next equation:

$$N_{stages} = \frac{T_{clock\ reference}}{Delay\ element} \tag{5.1}$$

Case	Delay_buffer (ps)	F_clock (MHz)	Stages
Best	31,31	400	79,85
Typical	36,08	400	69,29
Worst	41,85	400	59,74

Table 5.1: Number of stages for Reference clock 400MHz

Only the best case meet the specification of 35,35 ps as it can be seen in table 5.1, although the typical case is quite close to the goal. The results are the expected ones since layout adds parasitic capacitor and resistance. Therefore, the results have to be a little bit worst than the simulation which was done taking only into account the schematic in section 3.4.4.

The number of stages to be implemented will be 80. As many stages are included, more area occupied the chip will be; and we want to minimize the area occupied as much as possible. Hence, it is thought that decrease the number of stages is possible by increasing the clock reference frequency. The value of the clock reference has to be feasible in terms of implement it in full chip design. Therefore, it is decided to increase the clock reference to 433MHz.

In the next table are shown the number of stages that will be implanted in the layout:

Case	Delay_buffer (ps)	F_clock (MHz)	Stages
Best	31,31	433	73,76
Typical	36,08	433	64,01
Worst	41,85	433	55,18

Table 5.2: Number of stages for Reference clock 433MHz

Finally, the number of stages is $N_{stages} = 74$.

It should be noted that 6 delay elements is saved by increasing the clock reference frequency 33MHz.

5.2.2. Initial Layout

The main parts of the full-custom layout are shown in the next figure. We want to do a relation between schematic and layout to make the layout more understood.

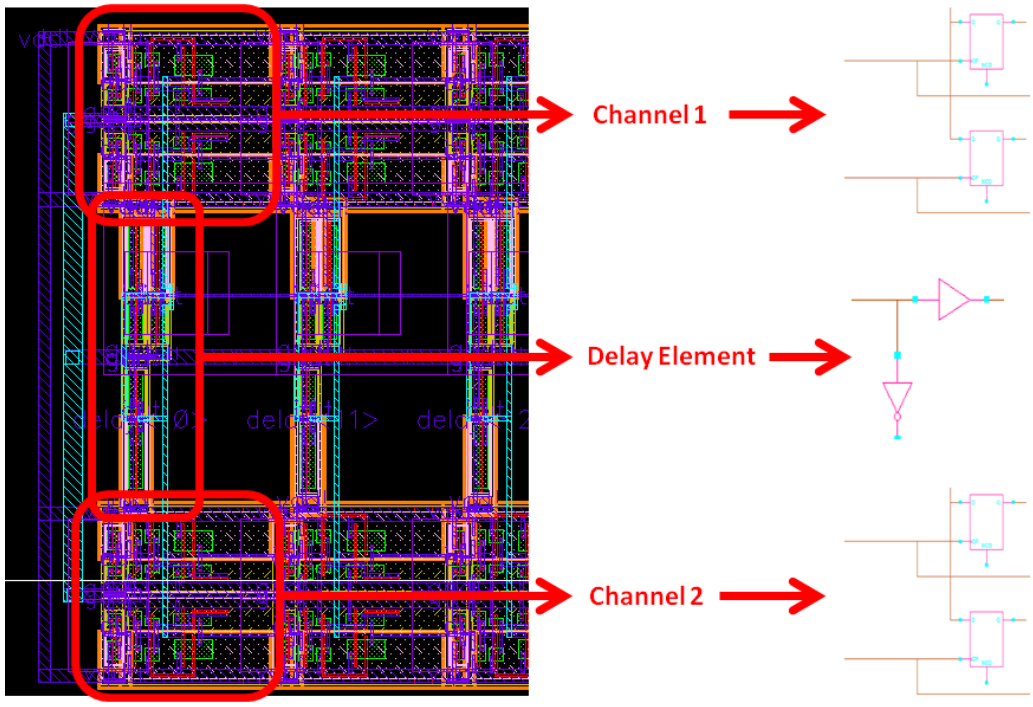


Figure 5.3: General layout delay line

There are only the two first stages in the delay line as it can be seen in figure 5.3. The rest of stages are straight forward repetition of one row. Besides, it can be seen the

interconnections between the different components by metal 1 and metal 2 at the left of figure 5.3. Those interconnections are connecting Vdd and Gnd for all devices.

The performance and errors got from this layout are the following:

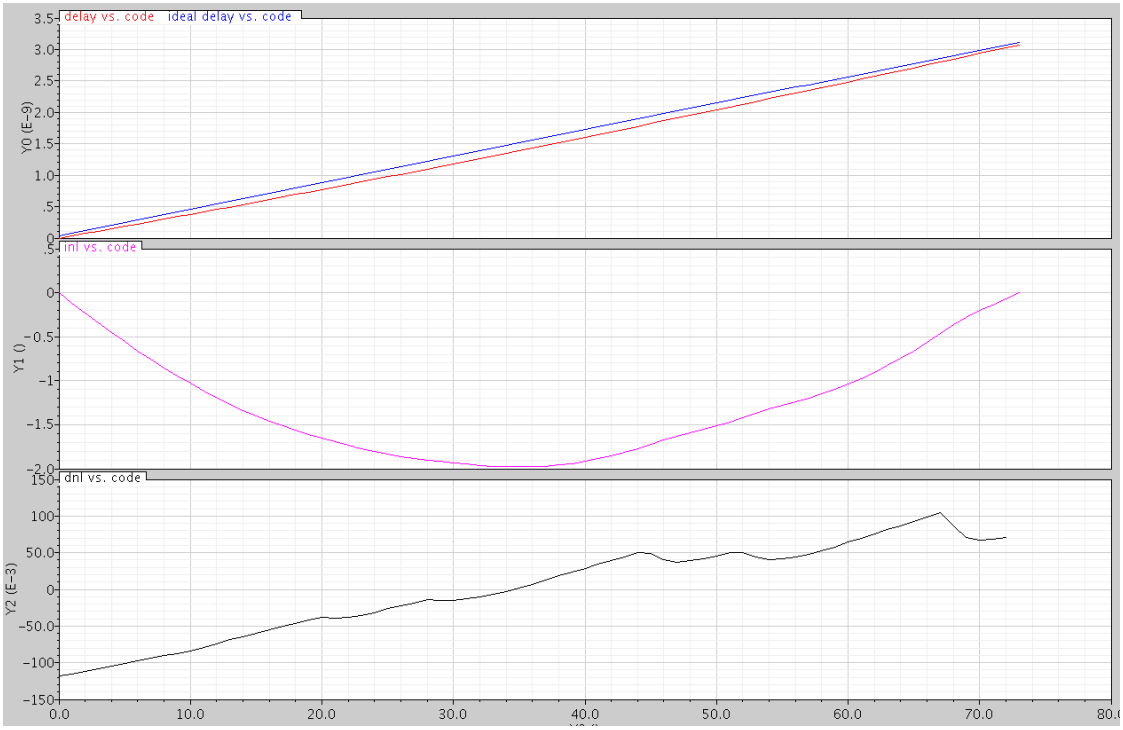


Figure 5.4: Delay, INL and DNL of initial layout

The delay element calculated in this layout is $\tau_{element_{inital}} = 36{,}75ps$ which is closer to the ideal delay calculated in previously sections.
Despite of the delay is still good; an error in terms of DNL and INL arises as it is shown in figure 5.4. There is an error of 2 LSB in INL and 0,2 LSB (peak to peak) in DNL. Those results are due to asymmetry of the parasitic, both capacitance and resistance. Those parameters can affect the delay as it can be seen in figure 5.4.

The purpose of the next changes in the layout is to improve the performance of the error keeping the value of the delay element as good as possible. Therefore, it is thought to implement a power ring supply in order to improve the current supply driven by the metals. This technique to feed the circuit by making a power ring is commonly used at the time to design layouts. Furthermore, metal 1 connecting all the devices in Vdd and Gnd has been made wider to let drive as much current as possible. Also, the decoupling inverter has been moved to the right side of the buffer. Thus, buffer and inverter are closer, saving area occupied; besides, less parasitic capacitance and resistance will be in the design since the metal connecting them will be shorter. Hence, the height of the layout is reduced the size of the decoupled inverter.

A big improvement is expected in terms of errors by adding the previously changes.

5.2.3. Layout version 1

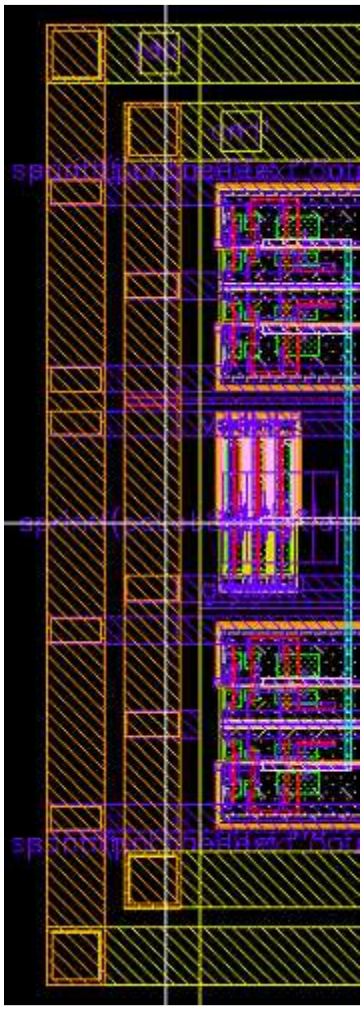


Figure 5.5: Layout delay line version 1

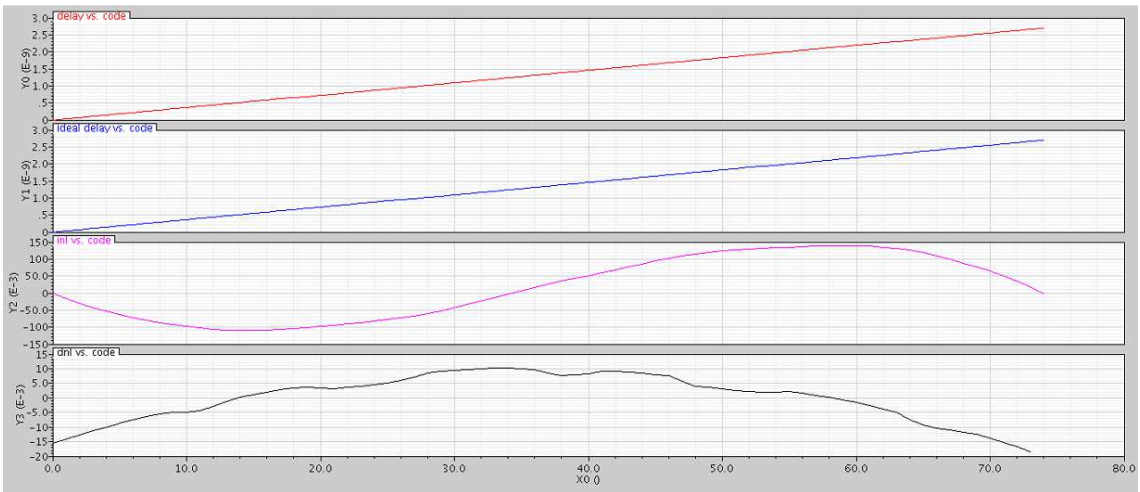


Figure 5.6: Delay, INL and DNL of layout version 1

The results obtained from the layout version 1 are shown in figure 5.6. As it can be seen the error of INL is 0,3 LSB peak to peak but it has a different shape in comparison with the INL in layout initial version. This is due to the symmetry of the parasitic along the delay line. It should be noted that the elements of the delay line are connected to the power ring supply only at the beginning and at the end. As it can be observed null error is just got in the middle of the delay line since the parasitic are the same either left or right regarding the power ring supply. The error is 0,025 LSB regarding the DNL since a change at the input, which switches the digital output, is closer to the ideal input voltage to get a change at the digital output. This improvement is due to make wider metal 1 and adding the power ring supply.

We want to see the effect of parasitic along the delay by adding two stripes of metal 4 to the power ring supply in stages 25 and 50. Less INL error is expected to get since the repartition of parasitic along the delay will be divided by 3.

A wide metal 4 stripes is added to the stages 25 and 50 to allow them to be connected to power ring supply as it can be seen in the next figure.

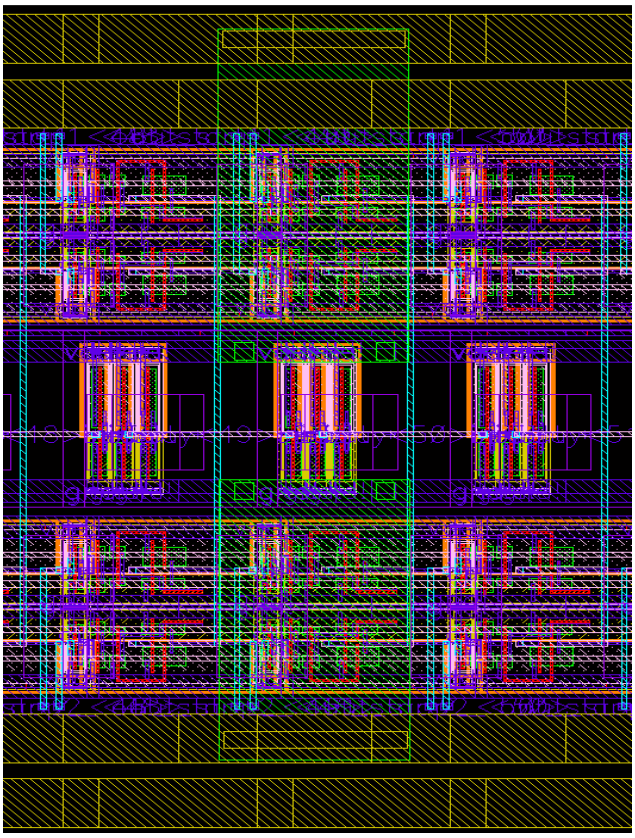


Figure 5.7: Layout version 1 with middle connection in 25 and 50 stages

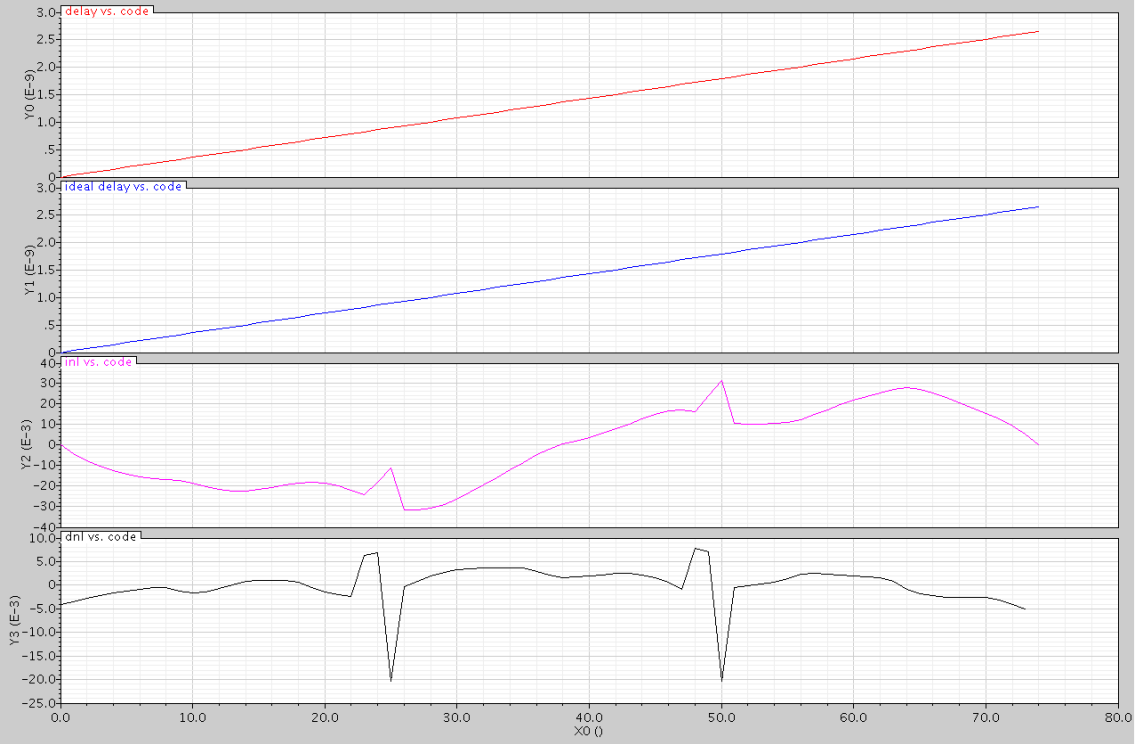


Figure 5.8: Delay, INL and DNL of layout version 1 with middle connections in 25 and 50 stages

Instead of the previous 0,3 LSB, we have now 0,06 LSB INL error. The improvement has been high. However, new results show some peaks at the stages where the big metal 4 stripe have been added and it makes poor performance of DNL. This is caused by the big capacitance introduced by the metal 4 stripe.

In order to get better performance of the delay line, we thought to minimize the effect of the parasitic capacitance introduced by the metal 4 by making short its stripes. Besides, the metal 4 stripes are added along the whole delay line to make the parasitic capacitance symmetric along the delay line.

5.2.4. Layout version 2

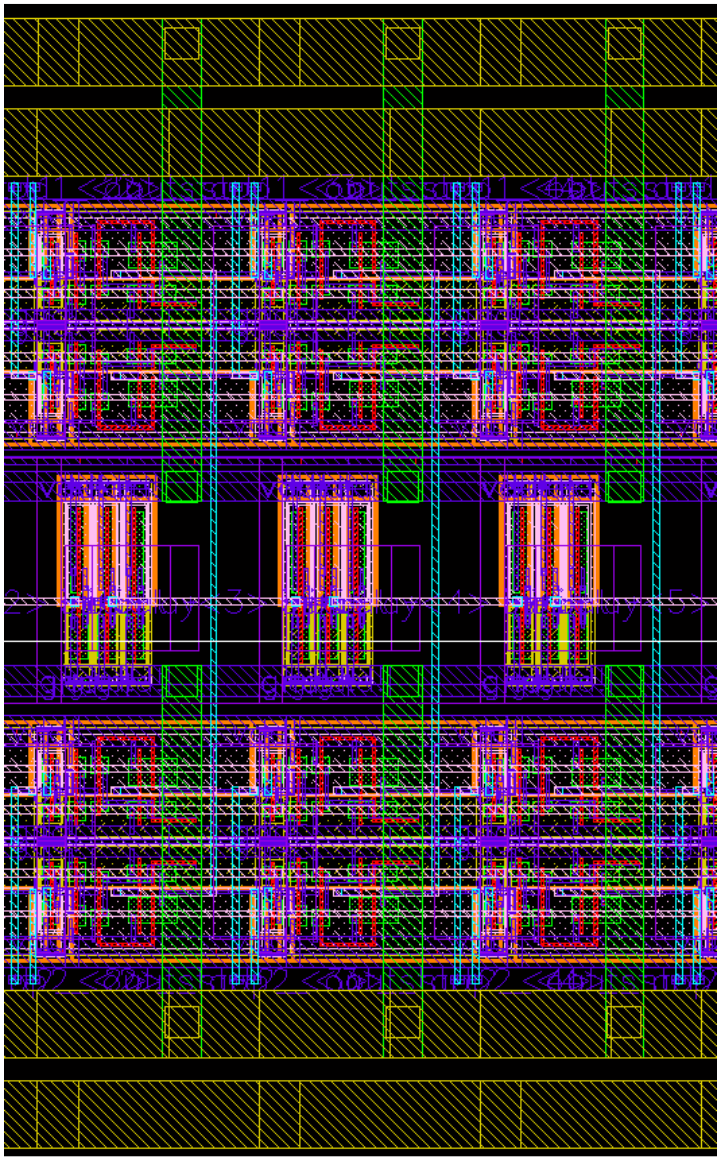


Figure 5.9: Layout version 2

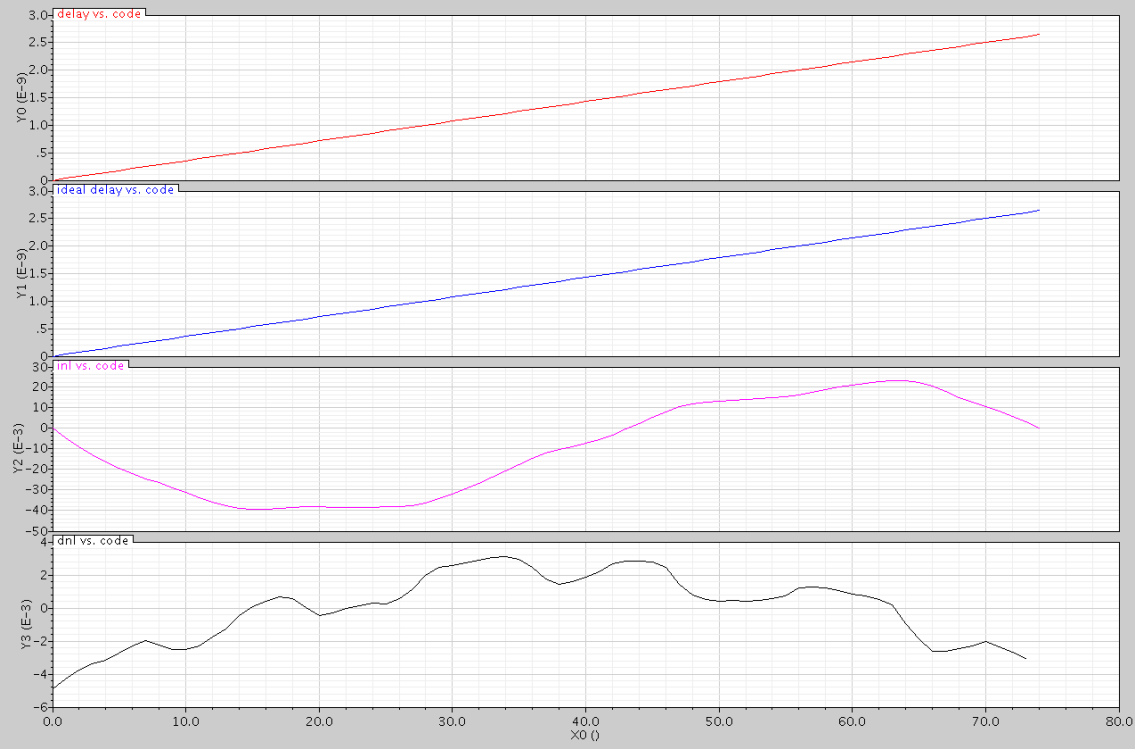


Figure 5.10: Performance of layout version 2

As it can be seen in the above figure, the INL is not modified at all since the connections between the power ring supply and the delay line are thin. Hence, INL is not possible to improve unless the metals that drive power supply will be wider. Nevertheless, the results obtained are equal good as in previously layouts. On the other hand, it can be seen an improvement of the DNL. The error of the DNL is around 0,007 LSB along the delay line. This is due to the parasitic capacitance are uniform along the delay line since the metal 4 is uniformly distributed.

There is less than one LSB DNL/INL errors along the delay line and it means that no code errors can be reached at the output. However, we want to minimize INL/DNL LSB errors as much as it is possible for the purpose to get better resolution. Besides, it is interesting in a theoretical framework since the layout techniques can be used in future layout developments to reduce INL/DNL LSB errors.

In order to improve the INL error, the power ring supply stripes are made wider and they will help to increase the current drive. The power ring stripes have to drive the main current generated by the flip-flops. If this current is higher than the current supported by the lines, it can cause voltage drop. Besides, the clock buffering stages has been added to the delay line layout structure as it can be seen in the next layout version. Three stages of clock buffering have been added to the layout with 4, 16 and 74 inverters per stage respectively.

It should be noted that the third stage of the clock buffering is directly incorporated to the layout, concretely, next to the flip-flops. Thus, each flip-flop has one inverter of the

third stage clock buffering as it is shown in figure 5.14. Therefore, 74 inverters per channels are needed in order to supply all the flip-flops.

Also, the next simulations will be done in the worst possible scenario; when high power consumption is got, as for example when a stop signal trigger the flip-flops. Since the power consumption and current can be high, it can lead to voltage drop in the metal stripes and then, decrease the delay line performance. Thus, it has to be checked that no voltage drop are caused by the high power consumption.

It should be noted that the worst scenario is considered in terms of power consumption. The two channels are working at the same time meaning that when a start/stop signal comes at the input, the equivalent load of 148 flip-flops switching at the same time.

5.2.5. Layout version 3

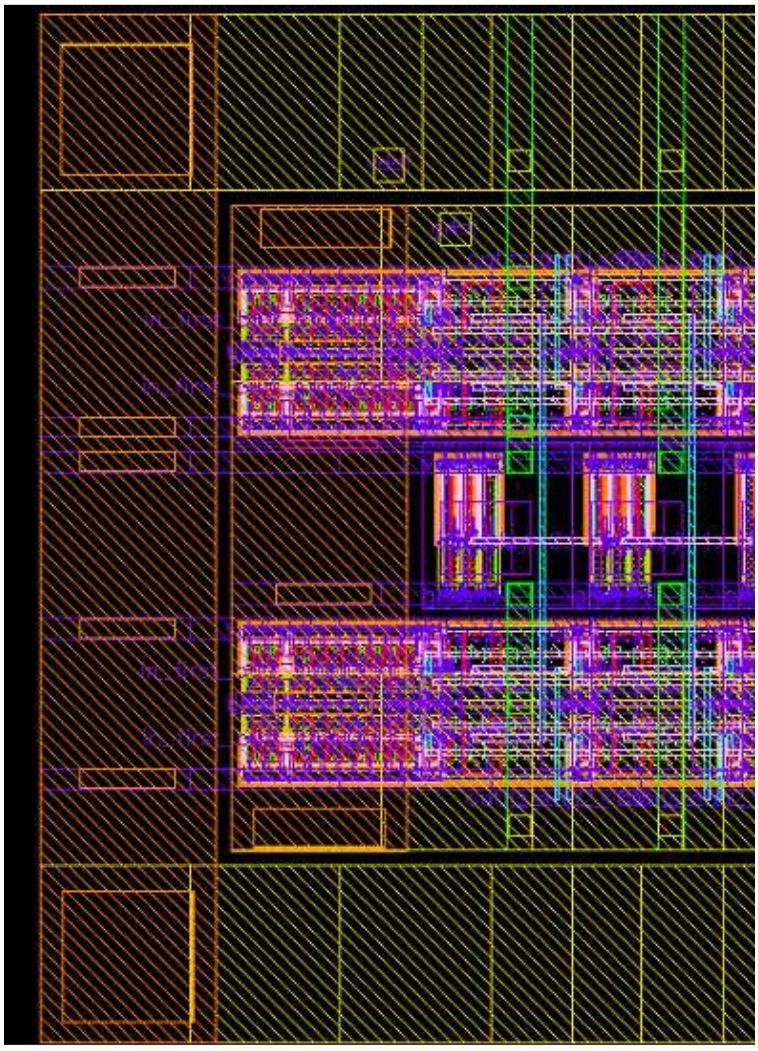


Figure 5.11: Layout version 3

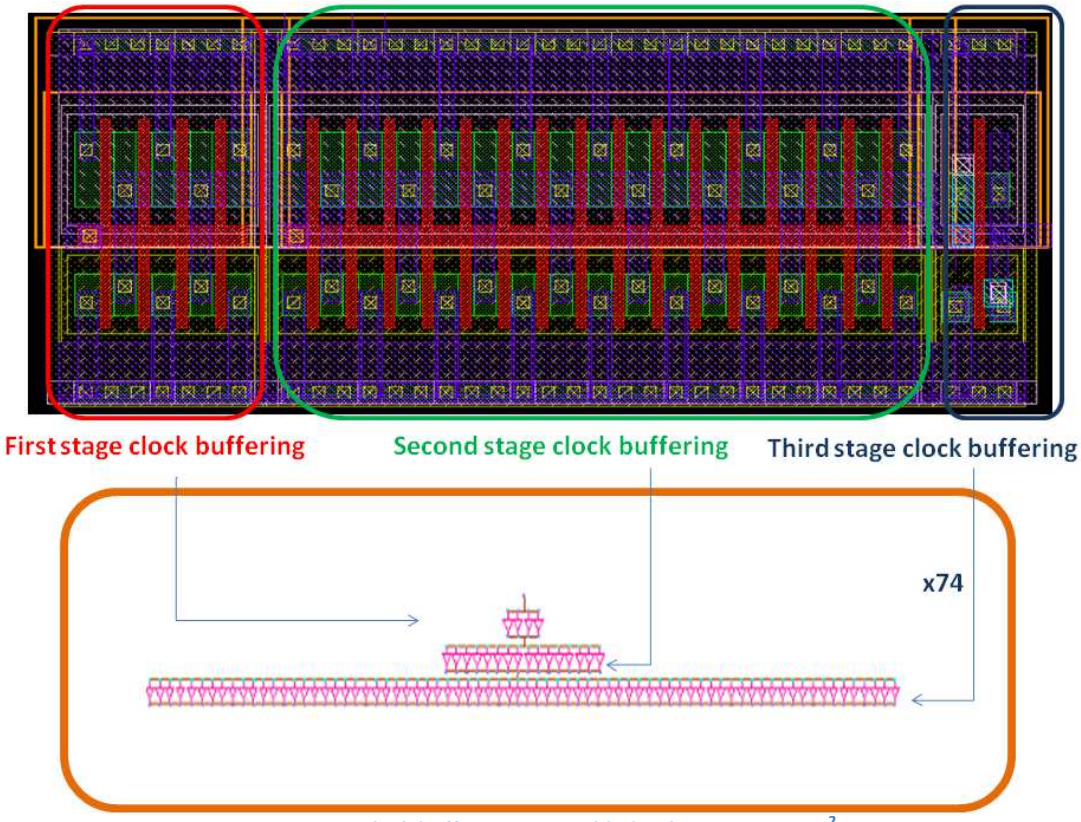


Figure 5.12: Clock buffering stage added to layout version 3[2]

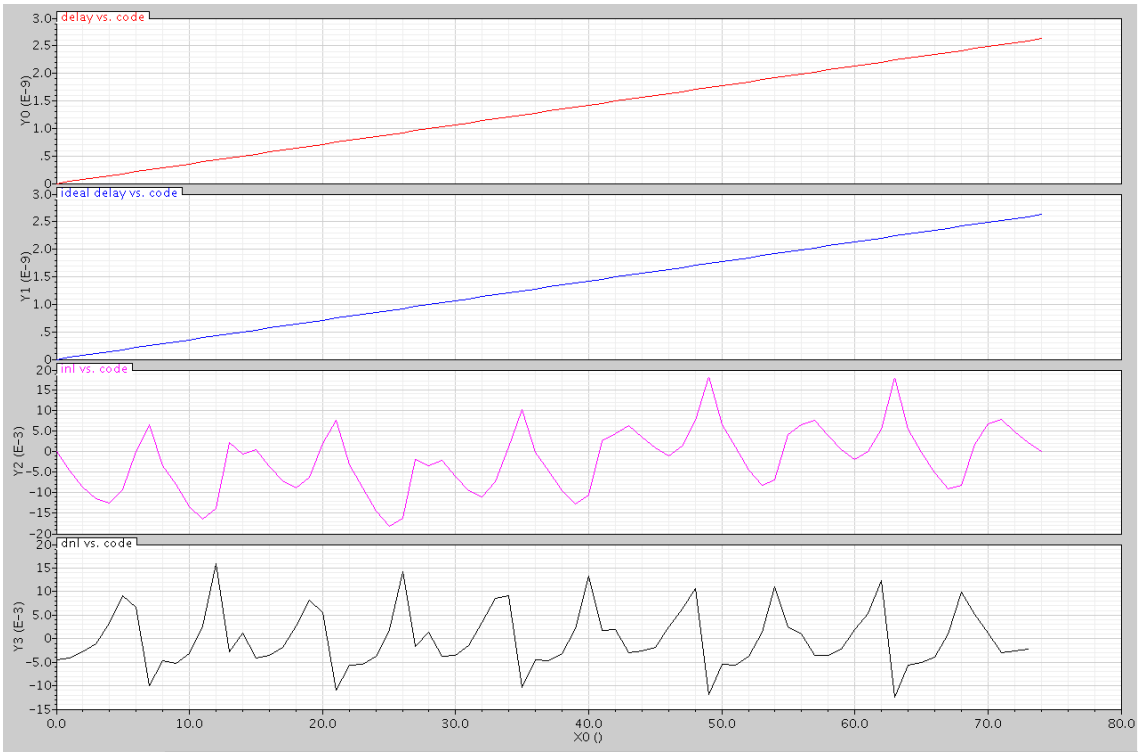


Figure 5.13: Performance of layout version 3

[2] Inverter of third stage clock buffering is repeated along the delay line, next to the 74 flip-flops.

The INL error is around 0,04 LSB as it can be seen in figure 5.13. This improvement is possible due to a wider power ring supply. Furthermore, it can be seen the spikes generated by the switching of the flip-flops; when the flip-flops switch, a voltage drop is created and that causes the DNL and INL spikes. As it can be in figure 5.14, stop/start signals causes big current consumption in comparison with the current consumption of the delay elements; this current consumption causes voltage drops in the delay line and voltage drops causes bad performance of the delay line which turns into the spikes in the INL/DNL. In previously simulations these spikes did not appear since the worst case was not considered.

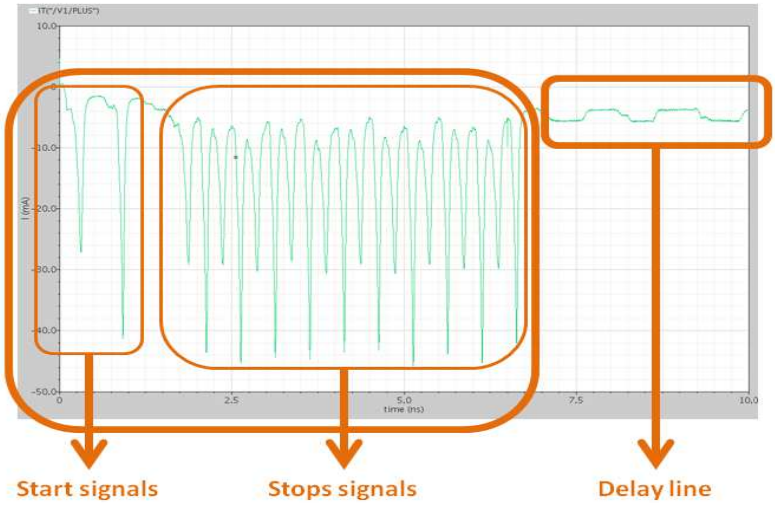


Figure 5.14: Current consumption layout version 3

The power consumption observed in the design, in the order of tens of watts, leads to a voltage drop issue. Therefore we want to have less power consumption in order to avoid voltage drop and preserve the performance of the design. As the delay resolution of each stage is not wanted to decrease, the delay element cannot be changed for others components with less power consumption since it also will decrease the performance. However, it could be done some minor changes either in the flip-flops or in the clock buffering. The flip-flops used in the circuit are the FD2Q_SYNCHS and they provide really good performance in terms of speed and metastability (see chapter 4). Hence, the part which is more susceptible to change is the clock buffering inverters (figure 5.14).

In particular, there are two ways to decrease the power consumption:

- Decrease the number of clock buffering inverters
- Decrease the dimensions of the clock buffering inverters

The first option is not suitable since then the input slope in the flip-flops will be less steep and it would have bigger error in the flip-flop sampling, increasing the metastability.

The second option has been chosen. Therefore, the input slope of the flip-flops will be still good. Though performance is lost in terms of delay between the signal of the first

flip-flop and the last one, it can be adopted because this parameter is less critical than the others mentioned before. The changes have affected to the dimension of the inverters in the third stage of the clock buffering and they will provide less power consumption in the sampling stages and thus, less voltage drops. Third stage has been chosen due to 74 inverters will be decreased. At the same time we thought if it is possible to decrease the power consumption.

It is realized that there is an empty space between delay elements and it can be filled by big capacitors which can help to keep voltage when there is high current consumption. These capacitors should help to soften the voltage drop and get better performance of INL.

5.2.6. Layout version 4

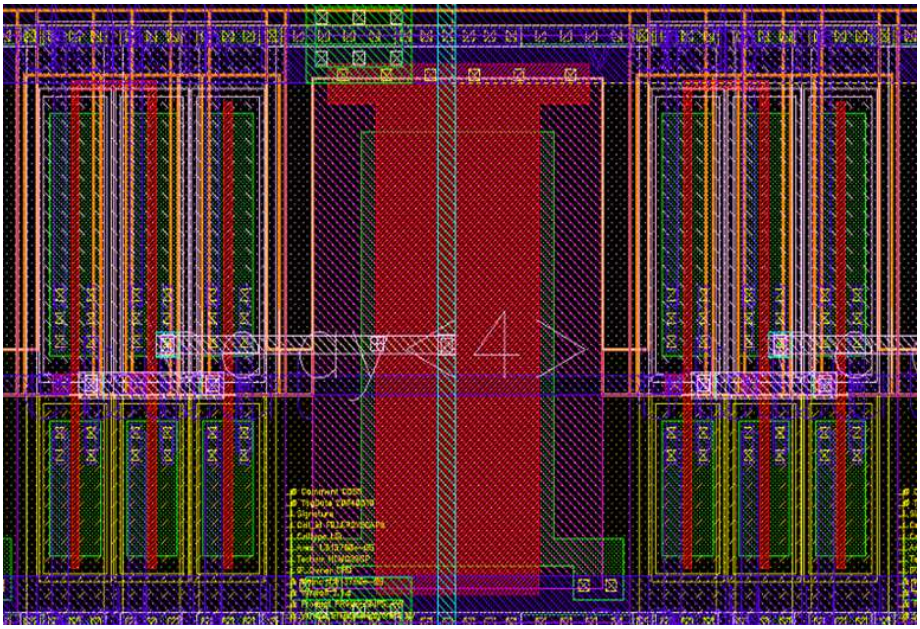


Figure 5.15: Layout version 4

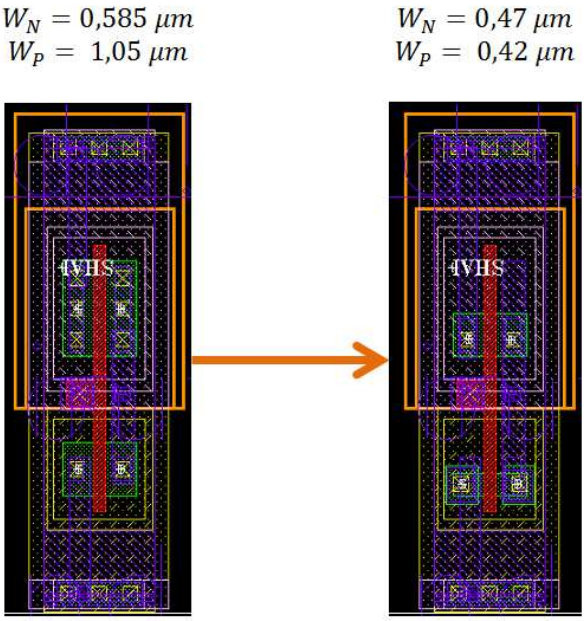


Figure 5.16: Third stage clock buffering size reduced

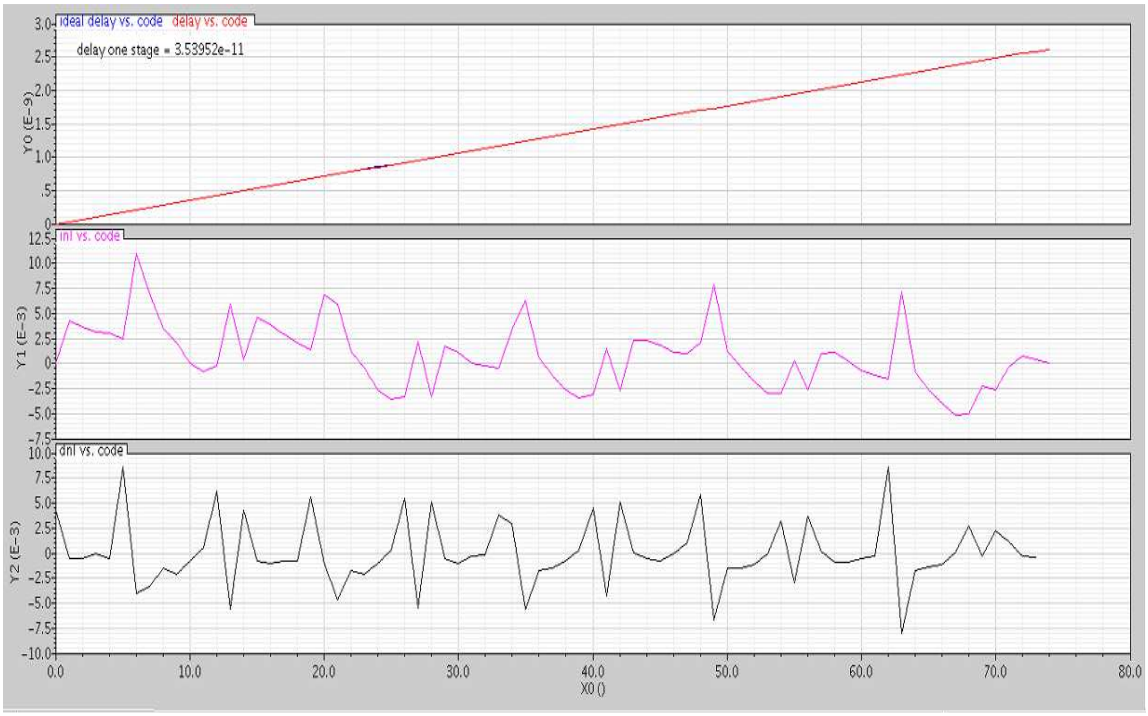


Figure 5.17: Performance of layout version 4

The dimension of the last inverter in the clock buffering has been decreased considerably regarding the one used in layout version 3 as it is shown in figure 5.16. Thus, it implies less power consumption. When the start/stop signals enter to the delay line, the flip-flops are triggered and the power current consumption will decrease. Due to the fact that the power consumption is smaller, the current consumption will decrease as well; therefore the voltage drop will be less also. That phenomenon can be seen in the performance of the INL and DNL in figure 5.17. Besides, the insertion of the capacitor between delay elements helps to make soft the voltage drop and it help to achieve better performance in INL and DNL. As it can be seen in the figure the DNL is 0,012 LSB and the INL is 0,010 LSB as well.

As previously results show the INL and DNL error are very low due to the last changes done. Thus, it is thought to try to decrease the height of the layout by making thinner the power ring supply. Performance will be worst but it can be up to 1 LSB to not compromise the digital output. At the same time, the power ring supply has been moved to the center of the layout since more area is possible to save.

5.2.7. Layout final version

The last changes have been applied to this layout version plus other changes in order to make it suitable to develop rightly the full implementation of the full chip taking into account the analog and digital flow.

The following changes have been done in the layout final version:

- Delete one stage of the clock buffering allowing flip-flops switching at the rising edge. Therefore, the stage number of the clock buffering has to be an even number. Hence, the first stage of the clock buffering has been removed. This results in increase the output load capacitance with a 4 factor; nevertheless, this loss of performance can be corrected with the digital flow in the full chip design regarding the placement and routing. It was not considered to add one more stage since the performance would have been the same and it would have increased the area of the device.
- One shield of metal 5 is added with connection with gnd in order allowing the placement and routing with the digital flow.
- All the output pins have been placement in the perimeter of the layout to make easy the interconnection between them and the digital flow.
- The interconnections between delay elements and flip-flops have been done directly with metal 2, avoiding the metal 1 stripe.
- The connections between power ring supply and the layout elements have been improved with new metal 4 interconnections along the delay line to keep symmetric the parasitic capacitance.

Figure 5.18 shows the final layout and figure 5.19 shows a diagram of the architecture in order to make the final layout more understandable.

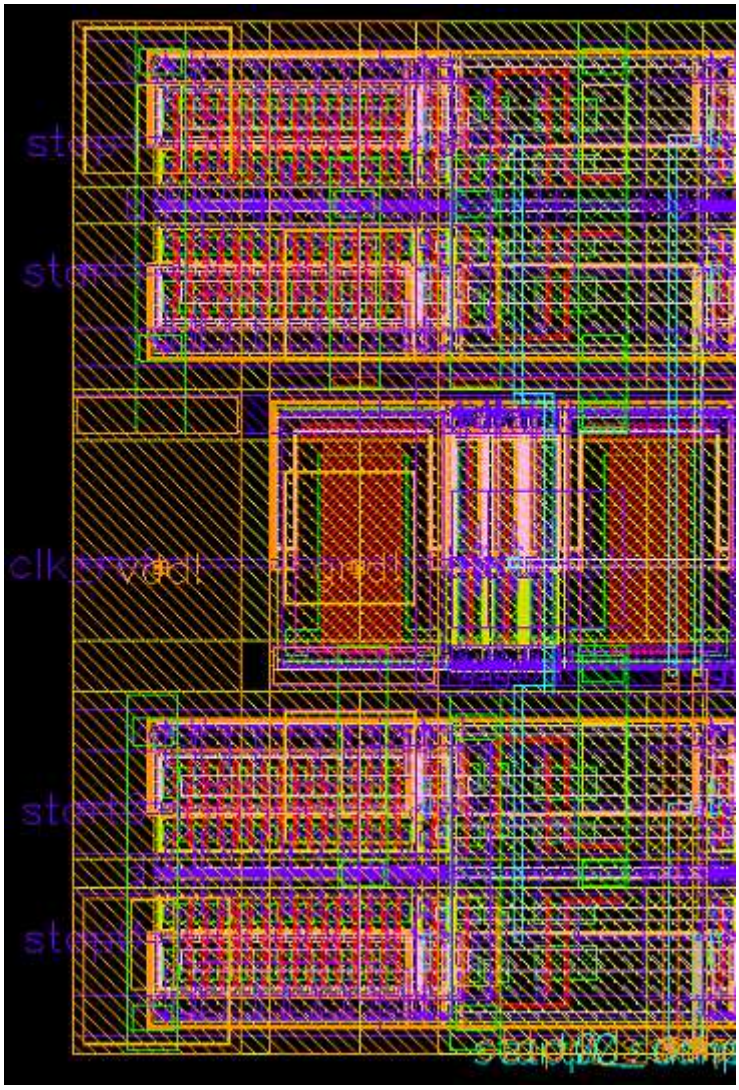


Figure 5.18: Layout final version

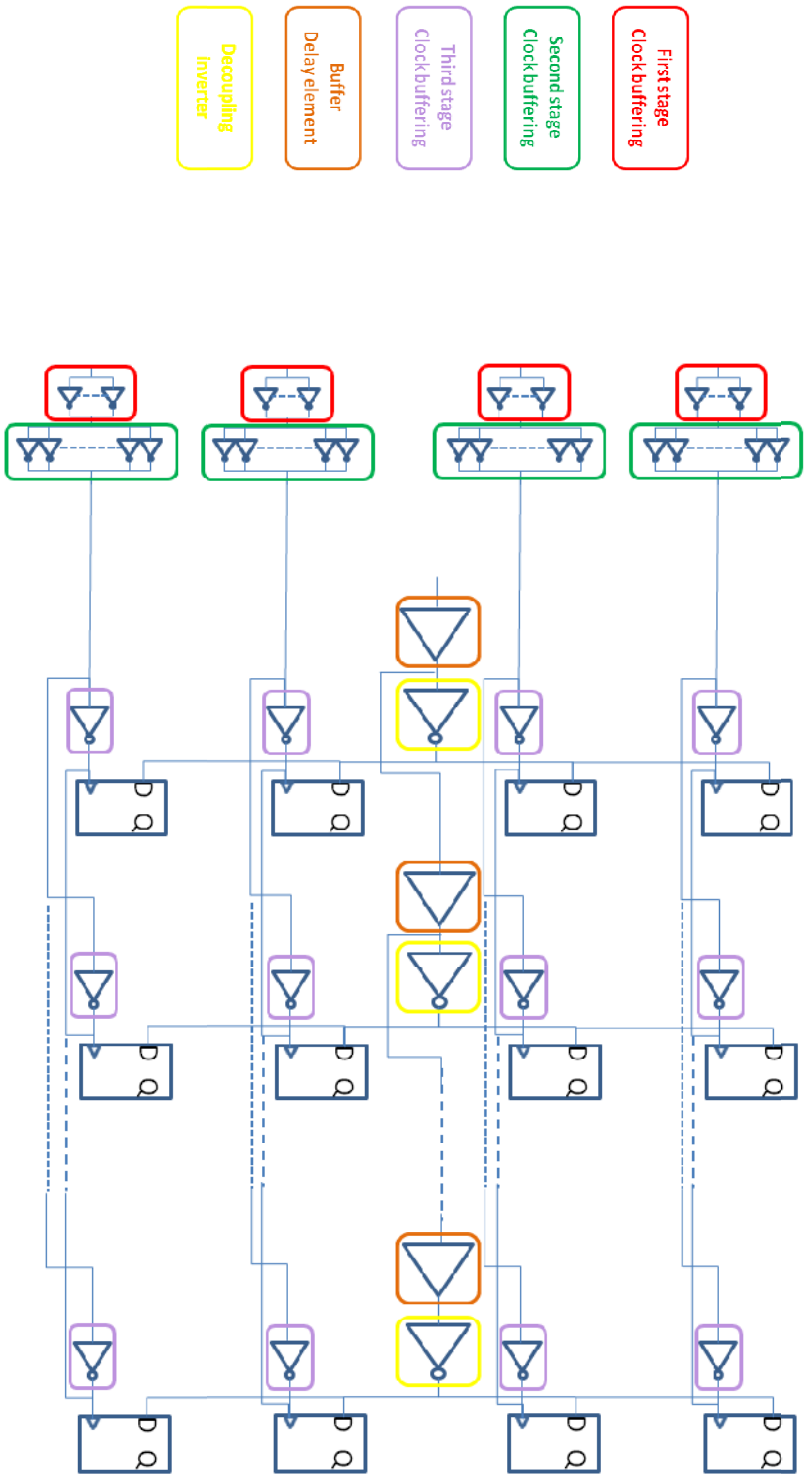


Figure 5.19: Schematic final layout diagram

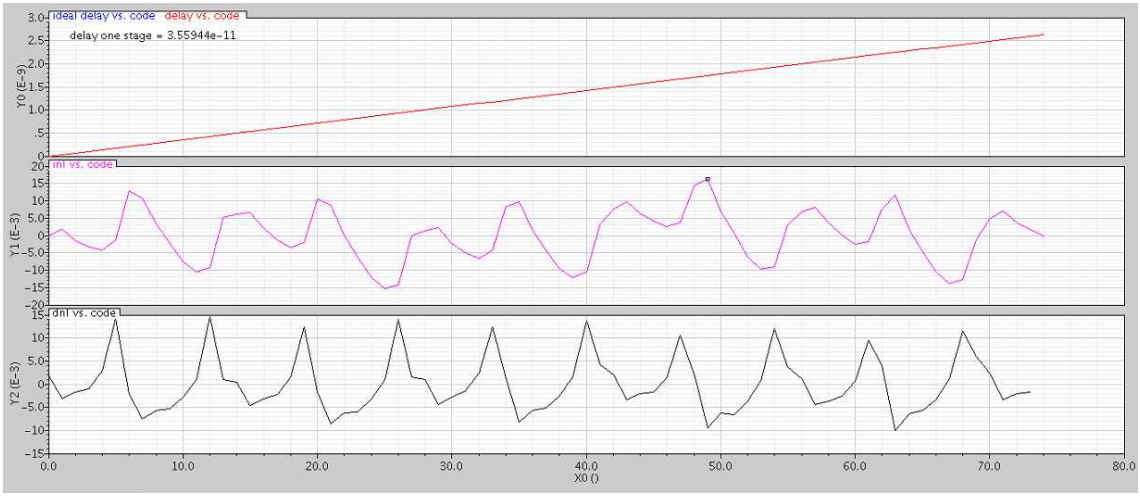


Figure 5.20: Performance of layout final version

As it can be seen in figure 5.20, the performance of INL is 0,03 LSB and it is worse than the layout version 4. Furthermore, DNL is also worse than previous layout being 0,025 LSB. This loss of performance is due to make thinner the power ring supply stripes but it can be perfectly accepted. Thus, loss of performance has meant saving area occupancy as it can be seen in section 5.3.
In the following section it is shown the main layout features in order to have it well characterized.

5.2.7.1. Montecarlo DNL – INL

Statistical simulation has been done in order to know better the main features of the layout final version. The purpose of this simulation is to see also the mismatch variation in INL/DNL error.

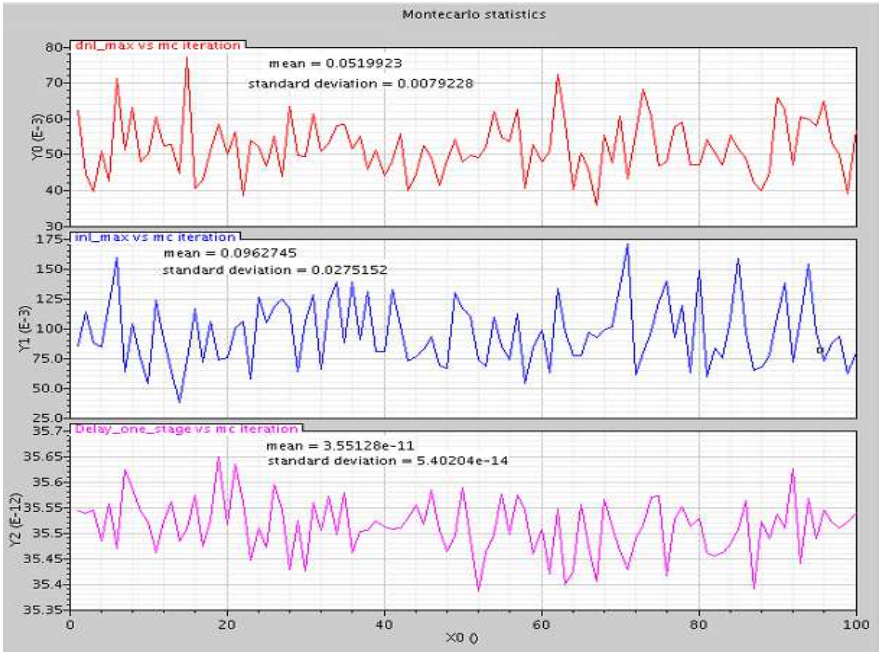


Figure 5.21: Montecarlo simulation of DNL – INL layout final version

The maximum value of DNL, INL and delay time for one simulation is represented in figure 5.21 against the montecarlo iteration; one hundred simulations have been done for this purpose.
Figure 5.21 shows a mean error of $0{,}09 \pm 0{,}02$ LSB and $0{,}05 \pm 0{,}007$ LSB for INL and DNL respectively. It should be noted that the error produced by mismatch variations in INL and DNL is bigger than the systematic error produced by the layout.
The worst case of INL is around 0,175 LSB and 0,077 LSB for DNL. Besides, the mean delay element obtained is 35,51 ps which it is slightly better than the one obtained in the case of theoretical results shown in section 5.2.1.

5.2.7.2. Power consumption

The quantification of power consumption has to be done between two consecutive start pulses. Among two start pulses, there are the 10 stop pulses and the rest of time there is the power consumption of the delay line. In fact, among start pulses, there are 4330 clock reference periods and only 10 stop pulses. Therefore, at the time to calculate the mean power consumption over one period, the power consumption of the stops signals are completely negligible in front of the power consumption of the delay line.

$$P_{total} \cong \frac{\int_{T_0}^{T_1} P_{FF} + \int_{T_1}^{T_2} P_{DL}}{T_{total}} \cong \frac{\int_{T_1}^{T_2} P_{DL}}{T_{1-2}}$$

Where $T_{total} = T_{0-1} + T_{1-2}$.

At any rate it is wanted to quantify the power consumption of the flip-flops and the clock buffering in the period where they are active as it can be seen in figure 5.22.

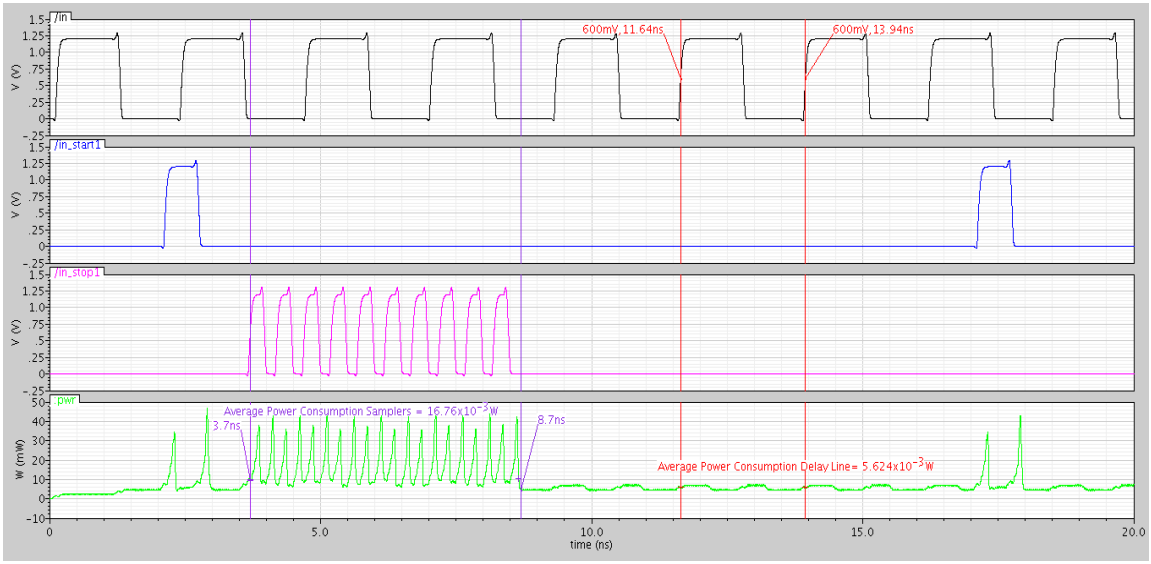


Figure 5.22: Power consumption layout final version

As figure 5.22 shows $P_{FF} = 16{,}76\ mW$ and $P_{DL_1\ period} = 5{,}624\ mW$.

The total power consumption of the line is $P_{total} \cong \frac{\int_{T_1}^{T_2} P_{DL}}{T_{1-2}} = 5{,}624\ mW$.

5.3. Overview Layout versions

Table 5.3 shows the main features of each layout developed. As it can be seen, the delay element has been decreased in the first layout designs until current consumption and area have been significant, in layout 4 and final version.
An improvement in INL/DNL has been done from the first layout adding the power ring supply and making the stripes wider afterwards, which have lead to increase the area of the layout. Nevertheless, area has been decreased in the final layout without compromise the other features.

	Layout Features			
Layout Version	Delay Element(ps)	INL (LSB)	DNL (LSB)	Size (length x height) (µm)
Initial Version	36,75	2	0,2	751,905 x 37,800
Version 1	36,16	0,3 - 0,06	0,025	763,860 x 50,205
Version 2	35,44	0,06	0,007	763,860 x 50,205
Version 3	35,12	0,04	0,025	797,860 x 67,185
Version 4	35,39	0,015	0,015	797,860 x 67,185
Final Version	35,51	0,09	0,05	763,660 x 35,540

Table 5.3: Overview main features for all layouts versions

CHAPTER 6

6. CONCLUSIONS

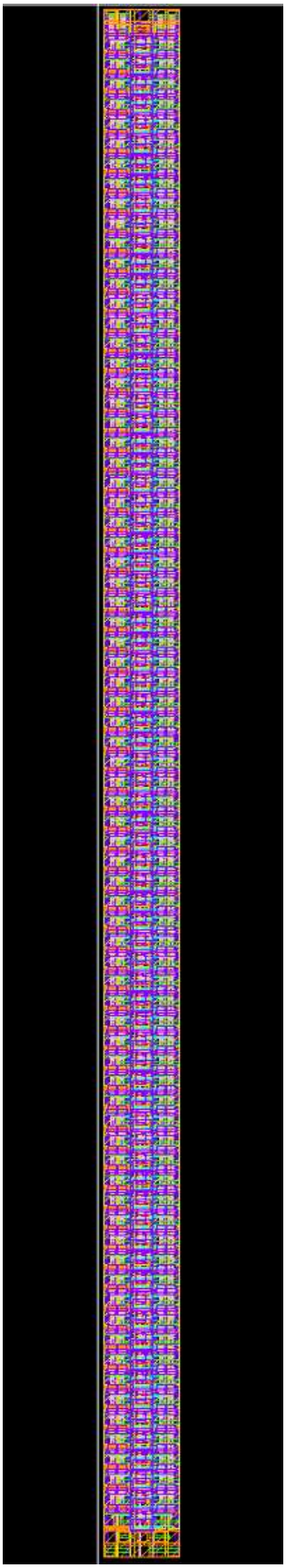
The goal of this project has been to find a topology to allow implement multi-channel multi-hit TDC to detect multiple stop hits and fulfill the specification to detect at least 50 ps time interval in fine measurement. Simulations have been done in order to demonstrate that it is possible to achieve 35,35 ps with 130 nm technology and buffers dimensions of $W_N = 2\ \mu m$ and $W_P = 3{,}59\ \mu m$ in a basic delay line with two channels. However, if we want to add more channels in the delay line, the time interval measure is increasing dramatically.

Schematic topology has been proposed in order to achieve the aim of increase the number of channels without compromise the performance. Basic delay line with decoupling inverter, equal size as buffers, has been explained and simulated properly. The results obtained in this work show that with decoupling inverter equal size is possible to achieve steady delay element in the delay line regardless the number of channels; otherwise, the delay element is increasing as the channels increase. Furthermore, mismatch variation is kept in equal size inverters topology in comparison with half size inverters. Simulations show that a time interval measurement of 37,21 ps is possible to achieve with standard deviation of 0,69 ps in the worst possible case.
The limitation of number of channels that can be implemented in the delay line is the metastability error, since it is more restricted than the slow slope performance. The maximum number of channels to not have bubble error in the sampling part of the fine measurement is 15. Furthermore, the probability to enter into a metastable state has been calculated in the different stages of the sampling stage being the results $MTBF_1 = 2{,}076$ seconds for the first sampling stage and $MTBF_2 = 54{,}66$ years for the second one. It should be noted that these failures rates applies only in one bit at each sampling stage. As it was mentioned before, with less than 15 channels is not possible to obtain two consecutive error bits.

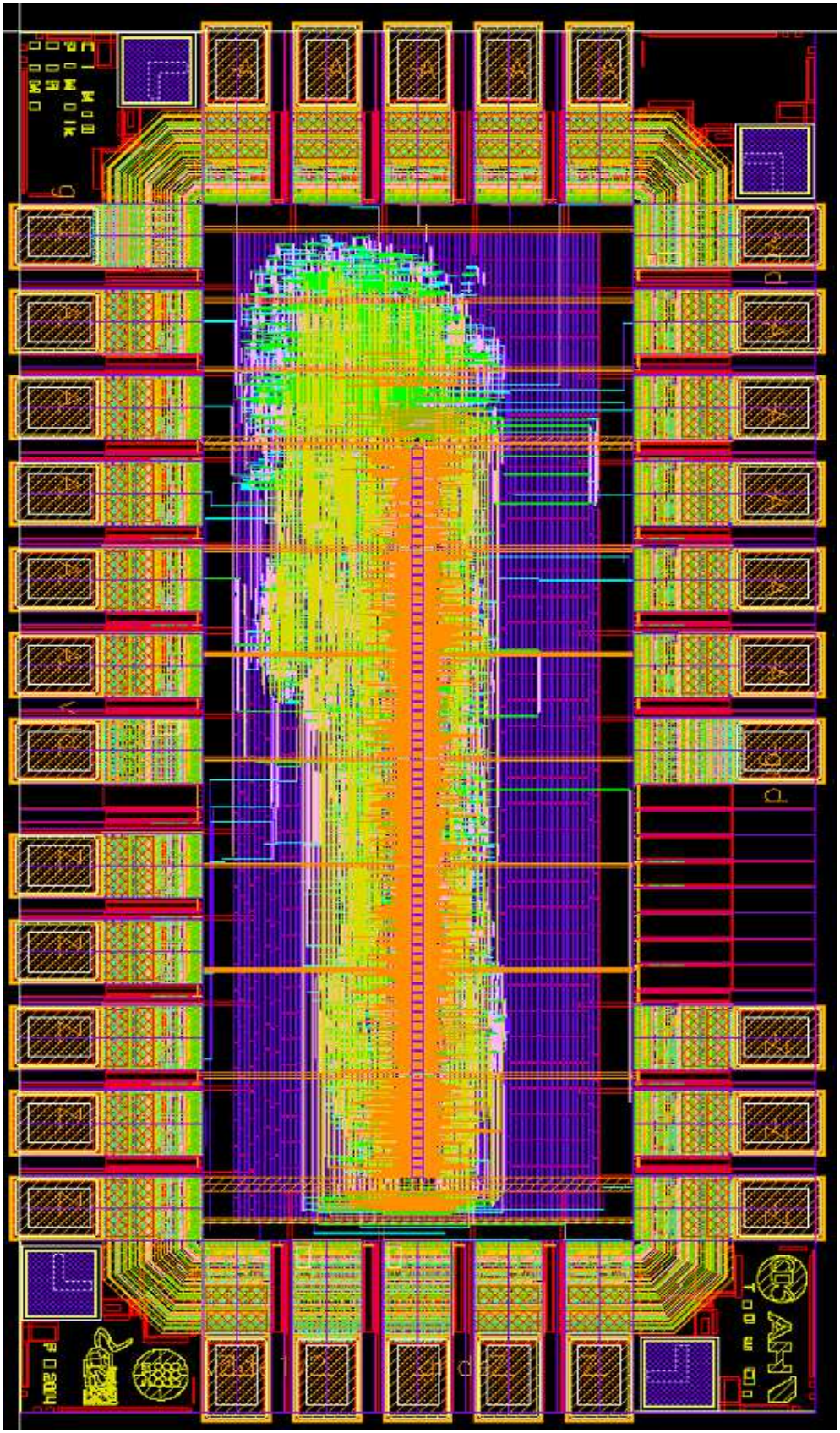
Full custom layout of decoupling equal size inverter scheme has been done in order to make it suitable for chip fabrication. Layout has been developed in order to achieve the best relation among size – performance – error. Those three factors are strongly linked and there is an important tradeoff between them. Hence, a layout of the delay line is achieved with 35,51 ps time interval measure, an error of 0,09 LSB and 0,05 LSB for INL and DNL, respectively. The final size of the layout is 763,66 µm length and 35,54 µm height.

The final delay line and the full chip layouts are shown in the Annexes. The chip is currently being manufactured.

ANNEX 1 – FULL DELAY LINE LAYOUT



ANNEX 2 – FULL CHIP LAYOUT



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