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Automatic DC Offset Cancellation in Built-in Differential Temperature Sensors

Thesis Submitted in partial fulfillment of the requirements for the degree of Master in Electronic Engineering.

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Preface

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1.Introduction

1.1. Antecedents:

The starting point in improvement of electronics technology based on solid-state semiconductor devices can be traced back to the late1940s. By that time, specifically in 1947, the first transistor wall demonstrated by two scientists called John Bardeen and Walter Brattain at AT&A's Bell Telephone Laboratories (USA). That moment was a new technological area for electronic technology. William Shockley, also at Bell Telephone Laboratories, worked over the next few months on the potential invention. He greatly expanded the knowledge of semiconductor and could be described as the father of the bipolar junction transistor of BJT. In 1956 Shockley, Bardeen, and Brattain received the Novel Prize in Physics "for their researches on semiconductors and their discovery of the transistor effect"[1].

As a matter of functionality the transistor provided the same functions as the vacuum tube but at a reduced cost, weight, size, and power consumption and with higher reliability. It can be said that the vacuum tube has been completely replaced by transistor in most of its applications. At the beginning transistors were made as individual electronic components and were connected to other electronic components (resistors, capacitors, inductors, diodes, etc) on boards to make more complex electronic circuits. However, it did not take long before the limits of this circuit construction technique were reached, e.g, large circuits, time delay which had to be considered while designing circuits.

The solution to the problem of large numbers of components was found in 1958 and 1959, by Jack Kilby and Robert Noyce at Texas Instruments (USA) and at Fairchild Camera (USA), respectively: "the integrated circuits"[2]; commonly referred to as an IC. Instead of making transistors one by one, several transistors could be made at the same time on the same piece of semiconductor. Not only transistors, but other electric components such as resistors, capacitors and diodes could be made by the same process with the same materials. For invention of the integrated circuit, the Nobel Prize in Physics 2000 was awarded to J.Kilby.

Since the invention of the integrated circuit in 1958, the number of transistors per unit area that can be placed inexpensively on an IC has been increasing exponentially, doubling approximately every two years. This trend was first observed by Gordon E. Moore in 1965 paper[3]; it is known as Moore's law. It has continued for almost half a century and it is not expected to stop for another decade at least[4].

Since the 1980s the predominant logic element has been the CMOS (complementary metal-oxide semiconductor) logic gate consisting of both p-channel and n-channel silicon MOS transistors (p-FETs and n-FETs), provoking a sudden increase in their performance and popularity. Other technologies competing with CMOS, such as bipolar and NMOS[5], were faster than CMOS but dissipated large amounts of power even when quiescent. At

first, CMOS was used only for special low-power application; but, as systems increased in size, and performance improved through scaling, the advantages of CMOS technology even among manufacturers of high performance mainframe computers. The MOS transistor, due to its characteristics and manufacturing process, results more appropriate for integration[6].

The integration of long and complex circuits in millimetric dimensions has been provided by this trend in integration and miniaturization. It also allowed dispensing with several discrete devices to perform the same function and incorporating all the electronic components, including analogue and interface circuitry, required to implement a system on a single chip. According to the Computer History Museum[7], in 1974, the first true system-on-a-chip or SoC appeared in a Microma watch when liquid crystal display's driver transistors as well as the timing functions were integrated onto a single Intel 5810 CMOS chip. Nevertheless, a number of challenges are also suggested by a very high level of integration.

The first challenge is to develop a procedure to establish the quality, performance and reliability of the IC before it is taken into widespread use. This is, in fact, the integrated circuit testing process. Due to the complexity of the problem and the impact on the quality and cost of the products, testing process has emerged as a functional pillar of electronics industry and technology.

1.2. Scope of this work:

The scope of this thesis is in the field of test and characterization of RF integrated circuits. Recently, a new technique has been developed that extracts figures of merit of RF circuits from temperature measurements. Therefore, temperature sensors is a key element in the feasibility and final cost of this technique.

The main goal of this thesis is to improve the state of the art of temperature sensors used in this technique, specifically, differential temperature sensors. The state of the art shows that prior measurements, these sensors need a calibration stage in order to correct the effects of global and local manufacturing variation which affect both the output common-mode voltage and sensor sensitivity with low area overhead.

In this thesis we are going to explain a new differential temperature sensor that completely cancel the above-mentioned limitations on the circuit, which controls the output behavior of the structure and compensate the output DC offset automatically.

To sum up, the general goal of this project is to improve the efficiency and reduce the errors of the global and local effects such as process variation and device mismatching, by using an automatic DC offset cancellation technique in differential temperature sensors.

1.3. Overview of thesis

This dissertation is compiled in seven chapters. The introduction in chapter 1 deals with the electronics technology antecedents as well as the scope and objectives of this work.

Chapter 2 reviews the current situation and trends of different testing methodologies and introducing temperature measurements as a nice way of testing and characterizing circuit under test behavior.

chapter 3 contains the introduction of temperature monitoring in ICs and temperature sensors and their applications. It also present the pros and cons of temperature sensors and different kinds of temperature sensors specifically introducing differential sensors and their structure, circuits and finally some limitations of this type is debated.

Chapter 4 specifically explains the DC offset error in differential temperature sensors and its resources. It describes the ways of quantifying this offset and possible approaches to overcome this problem and finally I present the conventional DC offset cancellation methods and their pros and cons.

Chapter 5 is completely included of the proposed technique for DC offset cancellation and after description of this method and its circuit topology, I explain all the components of this topology one by one separately using their structure.

Chapter 6 shows the experimental results of the temperature sensor before and after applying the proposed technique. Also some different analysis on the circuit are debated.

Chapter 7 is the final conclusion of the project, the overview of what has been done and what is going to be done in the future works around this topic.

1.4. References

[1] "Woliam B. Shockley - Nobel Lecture," Nobelprize.org, 12 Nov 2008. http://nobelprize.org?nobel_prizes/phusics/laureates/1956/shockley-lecture.html

[2] J.S. Killby, "The integrated circuits' early history," proceeding of the IEEE, vol.88, no. 1, pp.109-111,Jan. 2000.

[3] G.E.Moor, "Cramming more components onto integrated circuits, Reprinted from Electronics, volume 38, number 8, April 19, 1965, pp.114 ff", IEEE Solid-State Circuits Newsletter, vol. 20, no. 3, pp. 33-55, sept. 2006.

[4] "International Technology Roadmap for Semiconductors 2007 Edition," ITRS.net, 07 Dec 2008

[5] P.M. Solomon, "A comparison of semiconductor devices for high-speed logic,: Proceeding of IEEE, vol. 70, no. 5, 55. 489-509, May 1982

[6] Y.P.Tsividis, Operation and Modeling of the MOS Transistors, 2nd edition. New York: McGraw Hill, 1999.

[7] "1974 - Digital Watch is First System on Chip Integrated Circuit", Computer History Museum, 03 Dec 2008

2. Test and Characterization of Analog, Digital and RF ICs

2.1. Introduction

There have been several advantages from the advances in manufacturing technologies and higher integration densities in microelectronics and IC design. Such benefits include size reduction, higher reliability, and high speed while consumption less power. Besides these benefits, manufacturing defects and deviations of process parameters inherent to the complex and sophisticated manufacturing process used to fabricate IC are also presented [1]. The presence of these defects and deviations produces faults in the ICs. Catastrophic and parametric are two classifications of these faults.

Catastrophic fault is a kind of fault when the faulty element produces either a short circuit or an open circuit, which causes defects in the performance of the implemented circuit. The fault is called parametric when a characteristics of the faulty element deviates from its nominal value out of its tolerance range; so working out of the design specifications for the implemented circuit is the result.

The effect of the fault will be different according to the electrical domain of the circuit to be implemented. For example, in a digital circuit the presence of a catastrophic fault modifies its logic true table; while a parametric fault in this domain can affect the operating frequency or power consumption, but it does not necessarily affect the logic true table.

The impact of parametric faults in analog circuits is higher, as they can provoke a variation on the implemented function or can shift out their figures of merit from the required specifications. Furthermore, when a test process is being applied to a radio frequency analog integrated circuit (RFIC), the high frequencies of operation have also to be taken into consideration during the test bench setup to not modify the specifications of the circuit under test (CUT). These facts make that testing circuits in the RF analog domain requires special considerations, and makes it more complicated and expensive compared to the digital domain.

For their broad specifications and high sensitivity to process tolerance, these RFIC SoCs require very detailed and long performance tests. The features needed by the automatic test equipments (ATE)[2], i.e., dynamic range, bandwidth, low noise, etc., to verify these circuits make their cost unreachable. Furthermore, the in-use equipments are restricted to specific cases or relative simple circuits[3]. Therefore, because the time and resources implied, the test process is key contributor to the cost of manufacturing an RFIC packaged device.

On the other hand, nowadays the commercial wireless industry has driven a demand for inexpensive RFICs with low-cost packaging and manufacturing process[4]. This entire dilemma is due to a discrepancy between the development of new design paradigms and corresponding test practices. Eventually, since the last two decades, the International Technology Roadmap of Semiconductors (ITRS)[5] has identified the test of ICs as a serious bottleneck for the semiconductor industry as their complexity and level of integration

increase. While the design community had pushed the design envelope fat into the future, the test barriers have not kept pace with the test requirements of high speed, integrated wireless and wireless communication systems.

Taking the above-mentioned things into account, it is clear that one of the main needs of the semiconductor industry is the development of alternative RFIC's test strategies and techniques to meet the low-time and low-cost requirements for today's long and complex system on a single chip.

While debating of IC testing, several topics such as fault modeling, fault diagnosis, test stimulus generation, test characterization, design-for testability (DfT), built-in test (BiT), built-in self-test (BiST), concurrent error detection and the design of fault tolerant systems can be considered. This chapter presents a review of concepts, developments, and researches in the test-topics of analog, mixed-signal, and RF integrated circuits available in the literature.

2.2. Strategies of testing ICs

When it comes to testing an IC, determining the methodology and technique that covers the specific needs and requirements of the measurements is one of the most important things. For testing digital logic, the main purpose is to attempt the main test effort in terms of the logical input/output relationship of the IC. However, there will also be the need to attempt specific parametric (analogue) test.

Whatever the application and complexity of the design, digital logic testing is based on a number of core principles and, provided that the design can be suitably accessed, particular test stimuli applied and the results observed, the device test problem can be addressed.

In the analogue test environment signals will be required to be suitably generated, captured and analyzed. Analysis of signal characteristics resulting from a device under test (DUT) in both the time domain and frequency domain will contain information relevant to determining whether an analog circuit passes or fails a particular test.

Apart from classifying the ICs test strategies by the type of signal they use as stimulus, during production test environment the implemented strategies can be classified, according they are covering criteria, in two main categories: structural test strategy and functional test strategy[6, 7]. The next two sections will describe these test strategies in more detail.

2.2.1. Structural Test

There are two reasons why a manufactured circuit can fail in the objective or service it was designed and manufactured for: manufacturing defects and performance degradation due to process deviations. Manufacturing defects are lacks of structural integrity of the circuit due to the fabrication process or ageing. From a point of view of a whole integrated circuit or system, defects can be classified as extrinsic or intrinsic. Extrinsic defects affect the electric bonding connections and the heat dissipation path. Intrinsic defects affects the silicon piece itself.

Manufacturing defects and physical failures are collectively referred to as physical faults. These faults may produce an error in the expected service of the circuit to the global systems. The objective of test technology is the effective screening of manufactured circuits to detect the presence of faults.

The structural test strategy is based on covering criteria which are related to physical parts of the system. It makes no direct attempt to determine if the overall functionality of the circuit is correct, avoiding exhaustive test. Instead it verifies the chip structure to target manufacturing defects, and to attempt to ensure the manufacturing correctness of basic device structures such as wires, transistors, and gates[8]. It attempts to answer the question "was it manufactured correctly?". The condition is that if the structural testing has confirmed the correct assembly of the circuit elements, then the circuit should be functioning correctly.

In structural test the applied stimulus consist in test vectors or predetermined signals. Structural test vectors are extracted from the basis that fault models physically exist. These models identify defects and make possible their analysis through the experimental evaluation, i.e., realistic defect models.

Examples of realistic defects within a circuit include: a)process variation outside the normal process spread, e.g., an excessive change in transistor threshold (MOS) voltage value. b)Open circuits in metal interconnect. These will be resistive open circuits, the value of the resistance dependent on the physical nature of the open. c) Short circuits (bridges) between metal interconnect tracks. These will be resistive short circuits, the value of the resistance dependent on the physical nature of the short. d) Transistor stuck-open and stuck-short faults where the transistor is considered as a switch. e) Transistor (MOS) open/short circuits, e.g., defects in the gate oxide and resistive opens/shorts between nodes in the transistor. Using the right and realistic defect models is an important matter in ensuring high defect coverage.

Fault models are considered either logical or defect oriented. Logical fault models are translations of realistic defects into logic level models and potentially timing. Whereas defect oriented fault models are realistic defects based on the properties of the defect that created the fault. These are not simple digital (logical) models, but consider the electrical operation of the fault in terms on analog circuit primitives.

In the digital domain, depending on the test objectives, productivity, and final market of the semiconductor, the structural test strategy has[9]: a) reduced the time for developing test vector; b) allowed those vectors to obtain a greater fault coverage; c)allowed to generate deterministic vectors based on well-known fault models; d) shown a reduction in diagnosis and correction time for different types of faults and defects.

The reason for achieving these improvements is the existence of automatic test pattern generation (ATPG) techniques. ATPG is a process wherein the vectors or input patterns required to check a device for faults are automatically generated by a program[10]. Then, when they are applied to a digital circuit, enables testers to distinguish between the correct circuit behavior and the faulty circuit behavior caused by defects.

Fault testing of digital ICs using structural test strategy is a well-established and widely used mature methodology[7]. One of the attractive aspects of structural test is its ability to fit quickly and easily into the IC development process. However, even though there are some works that propose defect-based testing in the analog domain[11, 12], structural test is not as established as in the digital domain.

The application-specific nature of analog and RF circuit's behavior causes that the development of structural tests is not as straightforward to consider and automate as it is with digital circuits. There are no well established structural fault models that predict analog circuits' functionality and performance. This lack of analog fault/defect models and the complexity for generating them have been the main reason of the stoppage of structural testing in analog ICs, therefore, it is possible to consider the structural fault models practically missing in RF applications.

Also, the rapid progress in fabrication processes moving along the technology roadmap introduces additional problems given the introduction of new defect mechanisms that are unknown.

2.2.2. Functional Test

Another basic method in IC testing is the functional test strategy. As it can be seen from its name functional testing in meant to check devices functionality. The objective here is to ensure that correct results are obtained when good inputs are applied to the system, and when bad inputs are applied the system operates in a predictable way.

In digital circuits, functional test approach relies on the engineers' ability to write diagnostic programs that exercise all the possible functions in the target DUT. The functions that are not executed correctly will lead to externally visible behavior that allows detection of underlining defects. But there are no adequate models that can be

used to calibrate how well the functional test patterns cover the range of all potential defects.

For applying to complex digital circuits and systems, functional test patterns are more challenging because they tend to be too large and also because they require more elaborate test setups that require increased accuracy of signal timing[13].

However, functional test could be an alternative to cover those areas that are not covered adequately with the other existing approaches, i.e., structural test. In digital domain, functional testing executes at the true speed of the target devices and can be more effective in catching certain timing failures[10].

For testing analog circuits in the industry the applied techniques are based on functional test methods. Functional testing of analog ICs [7, 14] is still the preferred approach in order to identify and guarantee the wide range of required design specifications. In the context of the RFIC SoCs testing, to carry out the functional test of the system, the product is tested as it is used the end-user, and also, the product is specified in terms of a communications standard [6].

For example, a number of researchers have recommended to measure performance parameters, such as Bit Error Rate (BER) and (Route Mean Square) rms value of the Error Vector Magnitude (EVM), as the sole test metric [15-17]. A BER test compares a string of bits coming out of the DUT, against its corresponding golden sequence. BER is actually the ratio of the total number of errors to the total number of bits checked. BER tests are applied as modulated and control signals to the DUT such that it is possible to test parameters such as sensitivity, blocking signals, and other sort of channel interferences, BER requires long test times and is often quite difficult to measure correctly, as it is very sensitive to power level.

EVM is as measure of modulation or demodulation accuracy. The ideal modulation vector is compared to the resulting vector coming from the DUT. Error vector magnitude is the root mean squared value of error vector over time at the instant of the symbol clock transition. The ability to perform EVM measurements allows the device to be tested under conditions similar to its final use environment. However, functional test cannot be universally implemented to analog and RF devices, as in the case of structural test strategy to digital circuits.

It has been also identified that the future of analog and RF test has many parallels with digital circuit and system test. For instance, i) design styles: increasing complexity, use of designs with multiple threshold voltage (Vt) MOS transistors, ... ii) faster operation speed: higher signal frequencies, move into the nanotechnology domain, driven by communications applications, ... ; iii) higher levels of integration: newer failure mechanisms, i.e., limitations of existing fault models and need for models more representative of process defects; iv) lower operation voltages: aim to lower device power consumption, portable, battery operated circuits ..., and v) test equipment and

cost: need for reduced test time, which is reflected in test costs, need for reduced external ATE requirements and costs, i.e., simpler and less expensive ATE.

2.3. ICs built-in hardware testing techniques

Once the integrated component to be tested and the strategy that covers the specific requirements of the test have been identified, it is necessary to establish a well-suited test technique to be performed. The basic steps to perform a methodology to test a device consist in the generation of a satisfactory test stimulus at the input of the Device Under Test (DUT).

At the same time the response of the DUT should be measured, either in steady state or transient-state, or in time domain or frequency domain, and so the desired parameters (usually called test observables [19] selected, e.g., current, voltage, frequency, temperature. Finally, the proceeding and analysis of the selected parameters can be made in order to decide if the circuit works according to the specifications (e.g., gain, frequency, response, etc.).

As today's ICs are becoming much more complex and sophisticated with every technology, performing these steps associated with the verification of modern RFIC SoCs is not trivial task. test problems associated with these high-density integrated circuits, such as controllability, observabillity, and accessibility of internal nodes, need to be addressed. Design-for-testability (DfT) should be applied to overcome these issues [20].

The goal of the DfT solution is to ensure that the testability of the end product is competently and sufficiently developed during the product design process. A suitable test technique is developed during this stage in order to improve the level of testability by an external Automatic Test Equipment (ATE). The load-board itself is a perfect candidate. Here, the test functions are migrated from the external tester to the additional circuitry built around the DUT. The ability to apply stimulus to the DUT and capture the high speed test response is held by the additional circuitry. Otherwise, this information is degraded by cable parasitic of the low-bandwidth external ATE [21] (32). This solution is called Built-off test (BoT) [22].

The other alternative, known as built-in test (BiT) [23, 24], moves some part of all of the workload away from the ATE and places specific test circuitry into the DUT wherever possible. In this approach the device is modified to incorporate some additional functions within the chip by using dedicated test circuitry and by re-using components already available at the system level.

This allows for enhanced external test access to the internal nodes via the IC package pins. When the BiT approaches uses both on-chip signal generation, on-chip result

acquisition, and on-chip analysis to provide local tester resources, BiT becomes autonomous, leading to the built-in self-test (BiST) approach with little or no external test control.

Different strategies of BiT are, i) To reuse part of your circuit to test another one. ii) Just to include the test stimulus. iii) To include sensors and province to the ATE low frequency or, a DC digital signature of the high frequency performance.

Today, there is still lack of standardization in BiT/BiST for analogue ICs, and solutions will tend to be ad-hoc, on a device-by-device basis and requiring robust designs [25]. However, towards this end, BiT/BiST techniques are potentially useful and an open research area, even though their implementation becomes especially difficult for RFIC SoC designs. A variety of novel designs have been proposed as BiT/BiST methods in analogue, mixed-signal and RF ICs. Some of these potential integration in the use of BiS/BiST techniques are "DSP and ADC/DAC", "Alternate test", "Loop-back", "Current testing", "Oscillation-based BiST".

On the other hand, other BiT methodologies are the ones which employ built-in sensor to RF analogue circuit and they are more present every day. previous researches have shown that embedded RF sensors can generate significant information about analogue and RF circuit performance. Generally these electrical sensors generate a dc voltage proportional to the power [26], rms amplitude [27], envelope [28], or peak amplitude [29]. This test approaches place the embedded sensors for test response data acquisition from different points along the RF signal path.

The best sensors to use are those that have the least impact on RF DUT performance, while generating the maximum amount of test information. Despite small finite input impedance of the electrical RF sensors, they still degrade the performance of the system. Furthermore, with increasing operating frequencies, their parasitic input capacitances have a worse impact on the system. This is the same for all the other BiS/BuST methodologies.

In order to overcome these inconvenience, theoretical implementation concepts for analogue and RF thermal BiT have been explored in [29, 30]. Those works discussed the use of the temperature increase due to the power dissipation in the device under test as a test observable. A new testing technique environment based on the measurement of the temperature of the surface of the silicon or the packaging systems and the identification of faulty circuits on this basis, is introduced. The temperature is monitored using built-in temperature sensors [31], whose output signals proportional to the sensed temperature. In this method, the difference between the temperature of two different parts of the circuit is measured. This thermal testing method can be applied off-chip after manufacturing and especially on-line if sensors are integrated in the chip.

One of the main advantages of thermal measuring method is that the sensors do not load the input or the output of the DUT as the electrical sensors so. This fact makes thermal

BiT approach potentially attractive to be used as an alternative method to RFIC SoCs conventional test techniques.

2.4. Thermal Testing Approach

This section is devoted to describing that temperature measurement is used for test application, and some advantages of temperature as a measuring parameter is explained. The temperature of the Circuit Under Test (CUT) has been used as a monitoring parameter for failure analysis and failure prevention. Generally the temperature measurement in Built-in Test applications can; i) Identify gross failures that affect the power dissipation in bias circuitry, ii) measure the signal power along processing paths, and, iii) Design self-calibration schemes that can adapt to temporary thermal hot spots occurring near a sensitive circuit.

For instance, in the radio frequency (RF) circuits such as RF receivers chain, monitoring performance of individual blocks could be done by temperature measurements. Thermal coupling through the semiconductor substrate generates a rise in temperature in the vicinity of a circuit/device that depends on the device's power dissipation. This thermal coupling can be utilized for IC testing purposes. Using on-chip temperature gradients as test observables to measure power dissipation is advantageous because temperature gradients become more critical to both analog and digital system performance as the integration levels of modern single-chip systems increase.

Temperature is a magnitude that affects semiconductor devices in many ways:

i) The performance and safe margin of semiconductor devices are significantly affected by their operating or running temperature. One typical example is the decrease in the speed of a microprocessor as the temperature increases.

ii) It is also known that as the temperature increases, the reliability of a semiconductor device decreases. For modeling the relationship between steady-state temperature and mean time-to-failure for each failure mechanism, as applicable, the Arrhenius law is used. In addition, stresses due to temperature changes, temperature rate of change, and spatial temperature gradients are considered, as applicable [32].

iii) The information of the circuit can be extracted from temperature measurement. Since the temperature is a source of information about the state of the different elements involved in the heat transfer process throughout the IC structure, measuring the temperature of the operating circuits has had an important amount of effort. Besides, it has been used as a parametric test observable in different scenarios, such as reliability improvement [33], failure analysis [34], and screening structural defects either in the chip package [35] or in microelectronic circuits [36]. The set of procedures oriented to

develop the temperature monitoring in all of these scenarios is generally called thermal testing approach.

The advantages that temperature can offer as a test observable are; i) There is no electrical loading of the CUT. Thermal coupling is the link between the CUT and the monitoring circuit. ii) Both on-line and off-line tests are possible. iii) Temperature measurements provide diagnosis capabilities.

The thermal gradient information can be processed to generate a detailed thermal analysis, for thermal testing purposes. Then, by comparing the reference gradient with those with different levels from the nominal ones, it is possible to recognize a faulty device [37]. Furthermore, it allows the possibility to the electrical characterization of analogue and RF circuits, which is actually the scope of the present dissertation.

The criteria to select the appropriate method for thermal testing applications depend on the specific needs and measurement requirements. For example, precise knowledge of the thermal map, packed or unpacked chip availability, high sensitivity and high resolution, bandwidth capability, lab setup complexity, applicability, measuring time, silicon overhead, and experience and personal expectations.

Although thermal testing has some drawbacks such as slowing down the test application rate (as the magnitude of the temperature increases depend on the activation time of the heat sources), the overall conclusions represents that it is applicable for many testing applications. In the next chapter thermal monitoring in ICs is discussed, leading to introduction of Built-in Temperature sensors.

2.5. References

[1] S. M. Sze, Semiconductor devices, physics and technology. New York: John Wiley and Sons, 1985.

[2] D.A. Gahagan, RF (gigahertz) ATE production testing on wafer: options and tradeoffs, "proceedings of International Test Conference, pp. 388-395, 28-30 Sept 1999.

[3] P. Nigh, "SIA Roadmap: Test Must Not Limit Future Technology. " Proceeding of the International Test Conference, pp. 1152, 18-23 Oct. 1998.

[4] J.Ferrario, R. Wolf, S. Moss. and M. Slamani, "A low-cost test solution for wireless phone RFICs," IEEE Communications magazine, vol. 41, no. 9, pp. 82-88, Sept. 2003.

[5] "International Technology Roadmap for Semiconductors 2007 Edition," ITRS.net 07 Dec 2008.

[6] A kafton, Wireless SOC testing: Can RF testing costs be reduced?" Proceedings of Internatiional Test Conference, pp. 1226, 2002.

[7] I.A. Grout, Integrated Circuit Test Engineering: Modern Techniques. London: Spronger-Verlag, 2005.

[8] A. A. Joseph, S. Heuvelmans, G . J. Gerritsma, and H. G. Kerkoff, "Test structures and their application in structural testing of digital RSFQ circuits, "Physica C: Superconductivity, Vol. 403, no. 1-2, pp. 103, 2004.

[9] A. L. Crouch, Design-for-Test for digital IC's and Embedded Core Systems. Saddle River, NJ: Prentice Hall, 1999.

[10] P. Maxwell, I. Hartanto, and L. Bentz, "Comparing functional and structural tests." Proceeding of International Test Conference, pp. 400-407, 2000.

[11] S.J. Spinks, C. D. Chalk, I. M. Bell and M. Zwolinski , "Generation and Verification of tests for analog circuits subject to process parameter deviations, "proceeding of IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems, pp. 100-108, 1997.

[12] E. Acar and S. Ozev , Defect-based RF testing using a new catastrophic fault model. " Proceeding of International IEEE Test Conference, pp. 1-9, 8-8, Nov. 2005.

[13] L. Shen and S. Y. H. Su, "A functional testing method for microprocessors, "IEEE Transactions on Computers, vol. 37, no. 10, pp. 1288-1293, 1988.

[14] J. Spaandonk and T.A. M. Kevenaar , "Selecting measurements to test the functional behavior of analogue circuits, "journal of Electronic TEsting, vol. 9, pp.9-18, 1996.

[15] A. Halder and A. Chatterjee, "Low-cost alternate EVM test for wireless receiver systems," Proceeding of 23rd IEEE VLSI Test Symposium, pp.. 255-260, 1-5 May 2005.

[16] J. Dabrowski and J. G. Bayon "Techniques for sensitizing RF path under SER test," IEEE International Symposium on Circuits and Systems. ISCAS 2005, 00. 4843-484, 23-26 May 2005.

[17] S. Bhattacharya, R. Senguttuvan, and A. Chatterjee,"Production test technique for measuring BER of ultra-wideband (UWB) devices, "IEEE Transactions on Microwave Theory and techniques, vol. 53, no. 11, pp. 3474-3481, Nov. 2005

[18] M. G. Mendez-Rivera, A. Valdes-Gracia, J. Silva-Martinez, and E.Sanchez-Sinencio, " An On-Chip Spectrum Analyzer for Analogue Built-in Testing, " Journal of Electonic Testing, vol. 21. no. 3, pp. 205-209, 2005.

[19] K. Suenaga, S. Bota, R. Picos, E. Isern, M. Roca, and E. Gracia-Moreno, "Predictive Test Technique for dignosis of RF CMOS receivers," Processing of the 27th IEEE VLSI Sypposium, pp. 129-133, 2009.

[20] I. L Huertas, Test and Design'for'Testability in Mixed'Signal Integrated Circuits. Dordrecht Kluwer Academic, 2004.

[21] M. Burns and D. Roberts, An Introduction to Mixed Signal IC Test and Measurement. new York: Oxford University Press, 2001.
[22] S. S. Akbay "low-cost test of embedded RF/analog/mixed signal circuits in SOPs," IEEE Transaction on Advanced Packaging., vol. 27, no. 2, pp. 352-363, may 2004

[23] A. Richardson, A. Lechner, "Design for testability strategies for mixed & analogue desigs-from layout to system," IEEE Internation Conference on Electronis, Circuits and Systems, pp. 425-432, 1988.

[24] K. Arabi, "Mixed-Signal BIST: fact or fiction," Proceedings of International Test Conference, pp.1204, 2002.

[25] I. Pineda DeGyvez, "RF Best Test Practice," Proceedings of the design, Automation and Test in Europe Conference & Exhibition, pp. 7, 16-20 Feb. 2004

[26] J. Altet, A. Ivanov, and A. Rubio, "Structural RFIC device testing through built-in thermal monitoring, " IEEE Communications magazine, vol, 24, no. 9, pp. 98-104, Sept 2003

[27] Q. Yin, W.R. Eisenstadt, R.M Fox, and Z. Tao, "A translinear RMS detector for embeddd test of RF ICs," IEEE Transactions on Instrumentation and Measurement., vol. 54, no. 5, pp. 1708-1714, 2005

[28] D. Han, "Built-in RF transceiver test and diagnosis using transient envelope detection and sampling," Proceedings of the IEEE International Mixed-Signal Testing Workshop, Edingburgh, UK, pp. 250-257, 2006

[29] V. Natarajan, R. Senguttuvan, S. Sen, and A. Chatterjee, "Built-in Test Enables Diagnosis and Tuning of RF Transmitter Systems," VLSI Design, vol. 2008, no. 418165, 2008.

[30] J. Altet, A. Ivanov, and A. Wong, ¨thermal Testing of Analogue Integrated Circuits: A case study.¨Journal of Electronic Testing, vol. 19, no.3, pp. 353-357, 2003

[31]J. Altet, A. Rubio, ¨BiCMOS thermal sensor circuit for built-in test purposes," Electronic Letters, vol. 34, no 13, pp. 1307-1309, 1998.

[32] P. Lall, M. Pecht, and E. Hakim, Influence of Temperature on Microelectronics System Reliability: A Physics of Failure Approach. Boca Raton, FL: CRC Press, 1997.

[33] Y. Chengamo and A. Orailoglu, ¨Processor reliability enhancement through compiler'directed register file peak temperature reduction,¨IEEE-IFIP International Conference on Dependable Systems / Netwroks, pp. 468'477, 2009.

[34] L. jinglong, M. Motohiko, W. Wong, "failure analysis of Digital-analog mixed integrated circuit at high temperature," proceedings of 16th IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits, pp. 381-384, 2009

[35] V. Szekely, S. Ress, "New approaches in the transient thermal measurements," Microelectronics Journal, vol, 31, no. 9-10, pp. 727-737, 2000

[36] S. Lopez-Buedo, J. Garrido, and E. Boemo, "Thermal tetsing on reconfigubale Computers," IEEE Design and Test of Computers, vol 17, no1, pp. 84-91, 2000.

[37] D.L. Blackburn, "Temperature measurements semiconductor devices - a review, "Twentieth Annul IEEE semiconductor thermal measurement and management symposium, SEMI_THERM, pp.70-802004

3.Temperature Monitoring in ICs

3.1. Introduction

Nowadays, there are so many temperature measuring techniques for ICs, which shows how useful the temperature is. Some of the reasons of measuring temperature in ICs are the reliability, controllability, observability of the thermal measurement.

Knowing the circuit performance and reliability is the main purpose of measuring the temperature generated by a device or circuit under operation in an IC. In such process, an image or estimation of the surface thermal gradient is obtained. This gradient can be either spatially distributed on the total surface or only on a specific region.

It is said that the measurement of the thermal gradient is continuous, if it has a given spatial and thermal resolution. If it has temperature at finite and specific number of points of the surface , then the thermal gradient is discrete. Moreover thermal gradient can be static or dynamic (DC or AC) with a given bandwidth.

The main goal of monitoring the temperature in Integrated Circuits is to obtain an image of the thermal map (the spatial distribution of temperature) of its surface which can cover the entire surface or merely a region of that. This map can be continuous (with a given spatial and thermal resolution) or discrete (temperatures at a finite and specific number of points on the surface). It also could be statistic DC or dynamic AC with a given bandwidth.

For semiconductor devices or circuits a wide range of mature sensing strategies are available for measuring and predicting their operating temperature [1]. The temperature measurement methods can be divided into three general categories: mechanical methods, optical methods and electrical methods (Built-in temperature sensors). Mostly the methods of measuring are evaluated by laboratory experiments on real ICs.

Optical method is based on measurements of characteristics of light, either generated or reflected by the surface of the CUT. In optical method, depending on if we use contact or non-contact method, the tools are different. In contact method, a device or film must be applied to the surface to be measured, while, in non-contact method, this surface treatment is not needed, direct observation of the surface is sufficient.

Mechanical method on mechanical contact between sensors and the surface to be measured. Mechanical method obtains thermal imaging using an atomic force microscope (AFM). These two types of strategies are not the main topic in this thesis so we skip explaining them in details. These methods could be studied with some examples and calculations in the works. [2-13]

In this chapter, Built-in temperature sensors are introduced as the third method for measuring temperature, and then two types of Absolute temperature sensors and Differential temperature sensors will explained with some examples.

3.2. Built-in Temperature Sensors

All the methods discussed so far require direct visual access to the silicon die or a specially prepared laboratory to perform the measurements, or both.

Incorporation of a temperature sensor into the same die as the circuit under test provides flexibility for the test procedure and allows both laboratory testing and in-field testing. Neither direct visual access to the silicon die nor a laboratory environment are required. Direct thermal coupling measurements can be taken, without them being affected by any layer applied to the silicon. This temperature-sensing strategy is based on on-chip or built-in temperature sensors.

There are two major drawbacks to this strategy: first, there is a silicon area overhead, as space is needed for the temperature sensor/s in addition to that required for the circuit. Second, the temperature monitoring points are restricted to the placement sites of the temperature sensitive devices.

The output signal of built-in temperature sensors can be proportional either to absolute temperature or to the difference in temperature at two points on the silicon surface. This leads to the categorization of temperature sensors into two groups: absolute and differential. The electrical output signal of a sensor can be respectively written for two categories as:

$$Signal_{out} = S_A . T + C$$

$$Signal_{out} = S_D . (T_2 - T_1)$$

(3-1)

where S_A is the absolute sensitivity of the absolute temperature sensor, S_D is the differential sensitivity of the differential temperature sensor, C is an offset constant that may be zero and T_2 , T_1 are temperatures at different points on the silicon surface.

Absolute temperature sensors are used to monitor the working temperature of the circuit under test and eventually correct its operating point if it is working beyond its reliability limit. Another application of absolute temperature sensors is the thermal testing of packages.

Differential temperature sensors are used to detect alterations of the thermal map of the silicon due to changes in the power dissipated by its devices. They are insensitive to temperature increases that may offset the thermal map of the silicon surface, e.g., ambient temperature changes or leakage current increases in CMOS circuits.

3.2.1 Absolute Temperature Sensors

The first Solid state temperature sensors were linear circuits manufactured with bipolar technology, whose temperature-sensitive device was a forward-biased PN junction: a diode or bipolar transistor. These devices were used because their electrical nature is acutely sensitive to temperature, in a highly predictable and repeatable way. In [14], temperature sensors based on transistors are classified into three groups, depending on the number of transistors used as a temperature transducer.

In Single-transistor temperature sensor, the base-emitter voltage drop of a single transistor is used as a temperature-sensitive parameter. The sensor that feature two transistors as temperature transducers are also called PTAT: proportional to absolute temperature. In these sensors, the difference between the base-emitter voltages of two bipolar transistors is used as a temperature-dependent parameter. The temperature sensors that include three transistors as temperature transducers are called sensors with an intrinsic reference. Usually, sensors with an intrinsic reference have extra circuitry to compensate the non-linear behavior of transistor 3, which can be either built-in digital processing [15], or consist of different biasing strategies [16].

Temperature sensors for thermal testing and thermal monitoring must be as simple as possible in order to keep area overhead as low as possible. Examples of the use of p-n junctions to monitor the working temperature of digital microprocessors are featured in [17] and [18]. In both, when the temperature reaches the maximum value allowed, the manufacturer recommends a reduction of the clock rate to reduce power consumption.

CMOS temperature sensors have been gaining popularity due to the lower cost of this technology. CMOS temperature sensors can be classified as linear circuits and temperature-depended oscillators.

Linear circuits use either parasitic bipolar transistors or MOS transistors as temperature-dependent devices. Parasitic bipolar transistors can be obtained in a CMOS process if the diffusion-well layers or the diffusion well-substrate layers of this process are combined to obtain n-p-n or p-n-p junctions. Although the electrical performance of these bipolar transistors are inferior to those that can be obtained in a bipolar process, they have been used to design temperature sensors. Examples can be found in [19], [20].

MOS transistors have been used as temperature transducers, either biased in a sub threshold region or biased in strong inversion as a threshold voltage reference [21].

The main drawback of linear temperature sensors based on MOS transistors is that their sensitivity depends on process-dependent parameters, such as threshold voltage, and not on physical constants, as is the case with bipolar transistors. This makes this type of sensors process-dependent.

References [22] , [23],are based on ting oscillators. Figure 3-1 shows the basic topology of this circuit: a chain of an odd number of feedback inverters makes for logic instability at

the output node of the sensor. The working principle of this circuit is as follow: the value of v_{ref} is much higher than the threshold voltage of M1. Thus, if there is a temperature change, the temperature dependence of the carrier mobility on the drain current predominates over the threshold voltage temperature dependency. Transistor M1 behaves like a temperature-controlled tap, regulating the current available in the inverter chain to charge and discharge the gate capacitances. The output signal of this sensor is usually the clock input of a counter that is activated for a fixed time interval.

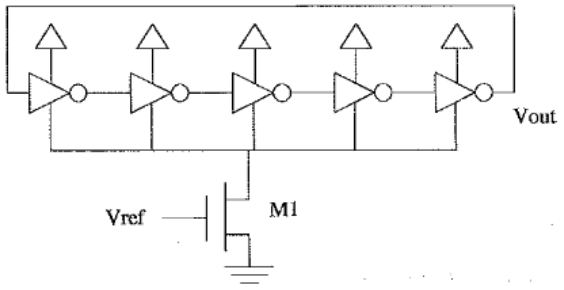

fig 3-1. Example of a temperature sensor based on ring oscillators [205, 217]

This sensor was implemented in [24] where the sensitivity of the output frequency was 10 kHz/°C (Vdd = 5 V). In [25], [26], this sensing strategy was used to perform thermal testing of FPGAs, and the circuit temperature affects the carrier mobility in all the inverters, the propagating delay increasing as the temperature increases.

The main advantage of this sensor topology are its simplicity and linearity. The main drawback is its high sensitivity to supply voltage changes.

Another example of a temperature-dependence oscillator is featured in [27], in which a combination of oscillators are used to drive two counters. Linearization and correction for process variations are carried out on chips with an EPROM and digital correction circuits.

In the next section, differential temperature sensors are discussed and explained in details.

3.2.2 Differential Temperature Sensors

Differential temperature sensors are used to measure the temperature increases generated by internal defects acting as heat sources, insensitive to changes in the offset of the thermal map. Fig 3-2 shows a simplified schematic of a BiCMOS of this type of sensor. The circuit has the same structure as a differential voltage amplifier. However, in this case, the two branches of the differential structure are destabilized by the temperature differential between the two bipolar transistors, rather than by the base-

emitter voltage differential. Therefore, the temperature transducers of the circuit are the two bipolar transistors Q1 and Q2, the temperatures of which are T_1, T_2, respectively.

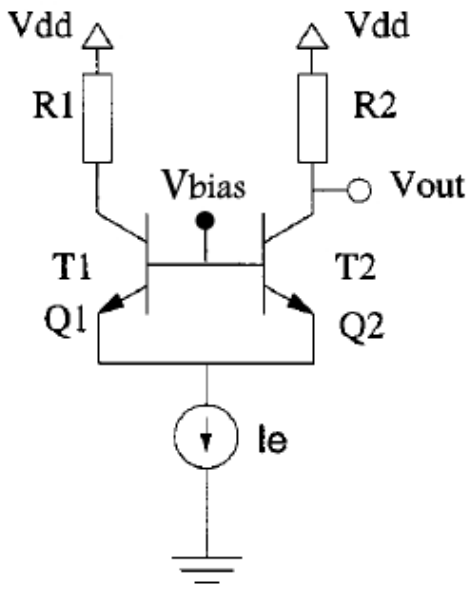

fig. 3-2 : Simplified schematic of the built-in differential temperature sensor.

The analysis of this circuit is based on a combination of the classical analysis of differential voltage of the sensor and the calculation of thermal feedback in operational amplifiers [28].

Ideally, the output voltage of the sensor circuit is only sensitive to the temperature differential of the transducer. Nonetheless, the output voltage of the sensor can be shown as:

$$\Delta V_{out} = S_{dT}\,(T_1 - T_2) + \frac{S_{cT}(T_1 + T_2)}{2}$$

$$(3-2)$$

where S_{dT} is the sensitivity to temperature differential and S_{cT} is the sensitivity to common-mode temperature.

If we assume that the surface temperature of the silicon is *T* , if a heat source is activated, the temperature of the bipolar transistors will increase, and will be:

$$T_1 = T + \Delta T_1$$

$$T_2 = T + \Delta T_2$$

$$(3-3)$$

thus, 3-2 can be written as:

$$\Delta V_{out} = S_{dT}\,(\Delta T_1 - \Delta T_2) + S_{cT}\left(T + \frac{(\Delta T_1 + \Delta T_2)}{2}\right)$$

$$(3-4)$$

If a differential temperature sensor is used for built-in testing purposes, its common sensitivity must be as low as possible, whereas its differential sensitivity must be as high as possible. Thus, it will only be sensitive to temperature increases generated by the activation of a device to test. The location of the temperature transducers inside the silicon die must provide a value other than zero for the term $(\Delta T_1 \pm \Delta T_2)$ when internal heat sources are activated.

Fig. 3-3, shows the electro-thermal small-signal model of the bipolar transistor shown. This analysis can be used to obtain analytical values of S_{dT} and S_{cT}. In the figure, the sensitivity parameter S_T is defined as:

$$S_T = \frac{\partial I_C}{\partial T}$$

$$(3-5)$$

Where I_C is the collector current of the bipolar transistor and T is the absolute temperature. *gm* is the small-signal transconductance of the bipolar transistor, $r\pi$ is the equivalent small signal resistance of the base-emitter diode and *r o* is the small-signal collector-emitter resistance of the bipolar transistor. ΔT, is the temperature increase over the device operating temperature. The use of this model assumes that self-heating can be neglected.

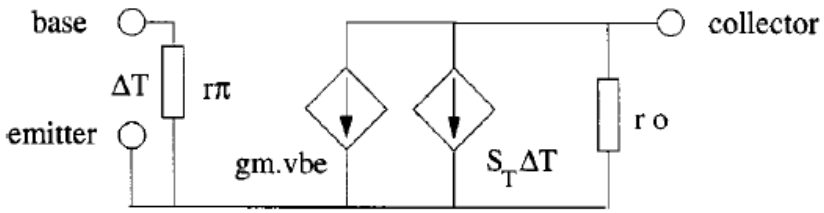

fig. 3-3 : Small signal electro-thermal model of the bipolar transistors.[ketab]

Fig. 3-4 shows the schematic of two built-in differential temperature sensors [29]. These two sensors are just two realizations of differential temperature sensors. This work characterize the static and dynamic performance of two differential temperature sensors. The complete analysis of these two sample sensors are given in [29] . Devices MR1 to MR4 in sensor 1 and Mo1 and Mo2 in sensor 2 are used to provide a high-output impedance and therefore, high-differential sensitivity.

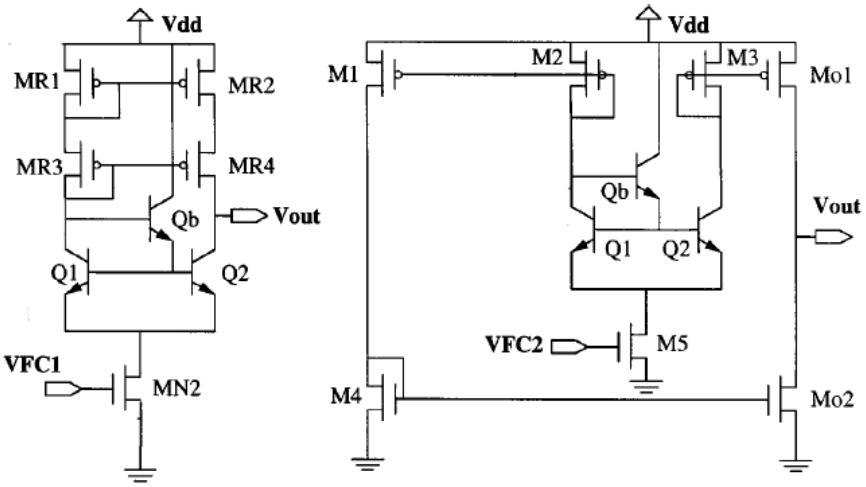

Fig. 3-4. Schematic of two BiCMOS built-in differential temperature sensors.
Left: Sensor 1 , Right: Sensor 2

3.3. Conclusion

In this chapter we discussed that a differential sensing strategy can be used to detect temperature increases generated by the activation of unexpected internal heat sources. Results point out that the temperature differences measured at several points of the silicon surface can be used as a test observable. In addition to the detection capability that this testing technique provides, due to the diffusion nature of the thermal transfer through the silicon die, simple signal processing of the temperature waveform sensed at the monitoring point can provide the distance between the heat source and the monitoring point. So by multiple temperature measurements the exact location of the heat source can be calculated. In a test environment, this information can be used to diagnose which part of the circuit is dissipating extra power.

In defective ICs, some devices may dissipate extra power, changing the silicon surface thermal map. Built-in differential temperature sensor can monitor these temperature increase [30]. In the next chapter, the global and local issues that may affect the performance of the Built-in differential temperature sensors, are discussed particularly.

3.4. References

[1] J. Altet, A. Rubio, "Thermal Testing of Integrated Circuits," Published by Kluwer Academic Publisher, ISBN 1-4020-7076-4

[2] Szekely, v. and Rencz, M., "Image processing procedures for the thermal measurements," "IEEE Transaction on Components and Packaging Technology, vol. 22, no. 2, June 1999, pp. 259-265

[3] Hiatt, J., "A method of detecting hot spots on semiconductors using liquid crystals" Proc. Int. Rel. Phys, Sym, Apr. 1981, pp. 130-133

[4] Szekely,V. "Tracing the thermal behavior of ICs" IEEE design and test of computers, 1998.

[5] Kolodner, p. and Tyson, J.A., "Remote thermal imaging with .7-mm spatial resolution using temperature-dependent fluoresent thin film", January 1983, pp. 117-119

[6] Kolodner, p. and Tyson, J.A., "Microscopic fluorescent imaging of surface temperature profiles with 0.01 C resolution", May 1982, pp. 782-784

[7] Claeys, W., Dilhaire, S., Jorez, S. and Patino Lopez, L.D., "Laser probes for the thermal and thermomechanical characterization of microelectronic devices." Microelectronics Journal, vol. 32, no. 10-11, Elsevier, pp. 891-898, 2001.

[8] Ju, Y.S., Kading, O.W., Leuing, Y.K., Wong, S.S., Goodson, K.E., "short-timescale Thermal Mapping off Semiconductor Devices", IEEE Electron Devices letters, Vol. 18, no. 5, May 1997 pp. 169-171

[9] Jorez, S. "development d'instrumentation et de methodologies pour la caracterisation thermique et thermomecanique de composants elecroniques," Ph.D thesis 2001

[10] Dilhaire, S. "Thermal stress analysis of Thermoelectric Devices Studies by Specklee Interferometry". Proc. Therminic 2001. pp. 24-27

[11] Altet, J., Dilhaire, S., Volz, S., "Four Different Approaches for the Measurement of the IC Surface Temperature: Application to Thermal Testing, " Proc. 7th Therminic Workshop, 2001, pp. 233-238

[12] Dilhaire, S., Jorez, S., "Thermal stress analysis of thermoelectric devices studied by Speckle Interferometry" Proc. Therminic 2001. pp. 24-27

[13] lai, J.. Chandreachood, and Carrejo, J.P., "Thermal Detection of Devices Failure By Atomic Force Micfoscopy", IEEE Electron device Letters, vol. 16, no. 7, July 1995, pp. 312-315

[14] Meijer, G.C.M., "Thermal Sensors Based on Transistors," Sensors and Actuators, vol. A 10m 1986, pp. 103-125.

[15] Krummenacher, p. and Oguey, H. "Smart Temperature Sensor in CMOS Technology", Sensors and Actuators, A21-A23 1990, pp. 636-638

[16] Micheda, J. and Kim, S.K., "A Precision CMOS Bandgap Reference," IEEE Journal of Solid State Circuits, vol. sc-19, no. 6, Dec, 1984, pp.1014-1021

[17] "Pentium III processor Active Thermal Management Techniques," Order # 273405-001, August 2000. http://www.intel.com

[18] "Intel Pentium 4 Processor in the 423-pin package, Thermal Design Guidelines," Order # 249203-001. November, 2000.

[19] Bianchi, R.A. Karam, "CMOS-compatible temperature sensor with digital output for wide temperature range applications", Microelectronics Journal 31, 2000, pp. 803-810

[20] Mejir, G.C.M "Temperature Sensors and Voltage Refereces Implemented in CMOS Technology, "IEEE Sensors Journal, Vol, 1. no. 3, Oct. 2001, pp. 225-234

[21] Kolling. A. "Design of a CMOS Temperature Sensors with current output", Sensors and Actuators A21-23, 1990

[22] Boyle, S.R. and Heald, R.A. "A CMOS Circuit for real-time Chip Temperature Measurement," Spring COMPCON 94, pp. 286-291, 1994

[23] Lopez-Buedo, S., Garrido, J. and Boemo, E., "Measurement of FPGA DieTemperature Using Run-Time Configuration, "7th Therminic Workshop, 2001, pp. 168-173

[25] Lopez-Buedo, "Thermal testing On Reconfigurable Computers, " IEEE Design and Test of Computers, Jan. - Mar. 2000, pp. 84-91

[26] Lopez-Buedo, S., Garrido, J. and Boemo, E., "Measurement of FPGA DieTemperature Using Run-Time Configuration, "7th Therminic Workshop, 2001, pp. 168-173

[27] Rasmussen, W., Zhu, J., Richard, S., and cheeke, D., "CMOS Intelligent Temperature Sensors," 33rd Midwest Symp. Circuit and Systems, 1990, pp. 849-852

[28] Solomon, J.E., "The Monolothic Op Amp: A tutorial Study", IEEEJournal of Solid-State Circuits, vol. SC-9, no. 6, pp. 314-332, December 1974

[29] J. Altet, A. Rurio, E. Schaub, "Thermal Coupling in Integrated Circuits: Application to Thermal Testing" IEEE Journal of Solid State Circuits, vol.36, no, 1, January 2001

4. DC Offset in Temperature Sensor

4.1. Introduction

In the previous chapter a differential temperature sensors were introduced and their working principles and output signals were discussed. In this chapter we are going to introduce the issues that can affect the operation of the differential temperature sensors and the result of them, which is output DC offset. For doing that, firstly we present a very simple differential sensor structure in order to discuss about the differential sensitivity and desired output. Afterwards, some sources of output DC offset will be introduced with some examples. Then, we compare the desired output voltage with the undesired one and difference between these two values and the importance of controlling this difference, with some examples. Finally the state of the art of offset compensation and the conventional methods will be introduced.

4.2. DC offset and its sources

In this section, in order to introduce the meaning of DC offset in the differential temperature sensors, a simple CMOS structure of differential temperature sensor is considered in fig 4-1.

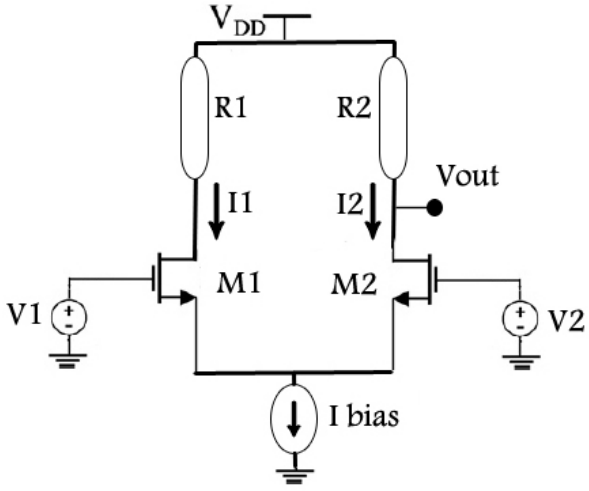

Fig. 4-1. Simple differential temperature sensor structure.

where M_1 and M_2 are differential pair, V_1, V_2 are the biasing voltages and I_1, I_2 are the MOS currents and R_1, R_2 are the equal output loads respectively.

This structure is used to measure the temperature increases which could be generated by a kind of internal defect which acts as heat source. In this situation, when there is a heat

source next to either of the MOS transistors, that increases the temperature of that MOSFET, the temperature change is seen in the output of the circuit.

When both Biasing voltages are the same and there is no external issue effecting the structure, I_{bias} is divided into half and $I_1 = I_2 = I_{bias}/2$. This is balancing case for the sensor and the output voltage varies in respect to the voltage differences between input pair. The output voltage can be written as:

$$\Delta Signal_{out} = S_D . (T_2 - T_1)$$

$$(4 - 1)$$

where S_D is the differential sensitivity and T_1 and T_2 are the temperature of M_1 and M_2 respectively. So the absolute value of the output voltage is:

$$Signal_{out} = S_D . (T_2 - T_1) + V_{Desired}$$

$$(4 - 2)$$

where $V_{Desired}$ is the desired value of the output when both temperatures are the same.

The desired output voltage diagram as a function of $T_2 - T_1$, without any global or local issue effecting the operation of the circuit is shown in fig 4-2. In this application, when the ambient temperature of M_1 and M_2 are the same, the output will be the desired value of vdd/2. (1.65 in this simulating).

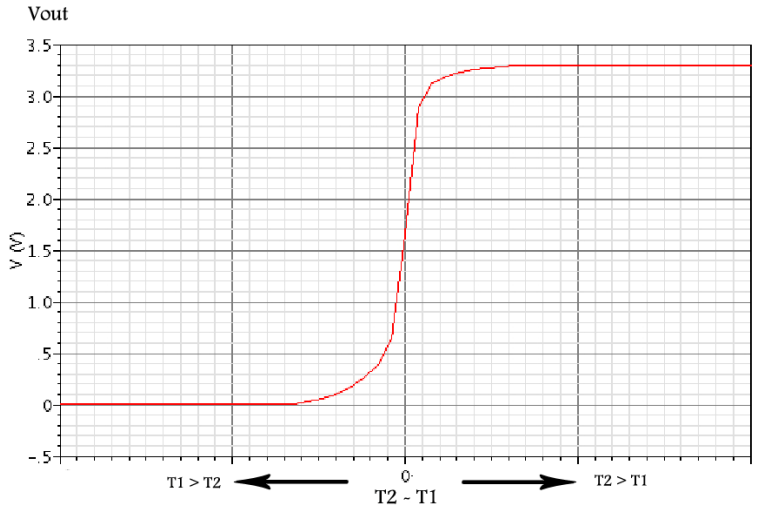

Fig. 4-2. Desired output diagram of the temperature sensor

On the other hand, Transfer functions of the temperature sensors experience some change in different fabrications because of some undesirable features effecting the

operation of the circuits. These issues could be global (process) and local (mismatching) manufacturing variations that affect both input and common-mode voltage and sensor sensitivity.

I) One of the most important limitations of implementing an integrated circuit of temperature sensor is a phenomena called process variation. Process variation is the naturally occurring variation the attributes of transistors (length, width, oxide thickness) when integrated circuits are fabricated. As the variation becomes a larger percentage of the full length or width of the device and as the feature sizes approach the fundamental dimensions, process variation becomes important specially at smaller process nodes. As a result of process variation, measurable and predictable variance in the output performance of all circuits is released, particularly in analog circuits due to mismatch. When this variance causes the measured or simulated performance of a particular output metric (bandwidth, gain, rise time, etc.) to fall below or rise above the specification for the particular circuit or device, it reduces the overall yield for that set of devices [1-4].

We assume that in the schematic of fig. 4-1 the width of the transistors are designed to be 10.45 um, in order to achieve the desired output value shown in the diagram of fig 4-2. As a matter of process variation, after fabrication, the mentioned width becomes 10.40 um for one and 10.45 um for the other one. This will cause an undesired changes in the circuit operation which finally affects the output voltage and shift the diagram of fig. 4-2 to right or left. This shifting phenomenon, which is called DC offset, is shown in fig 4-3.

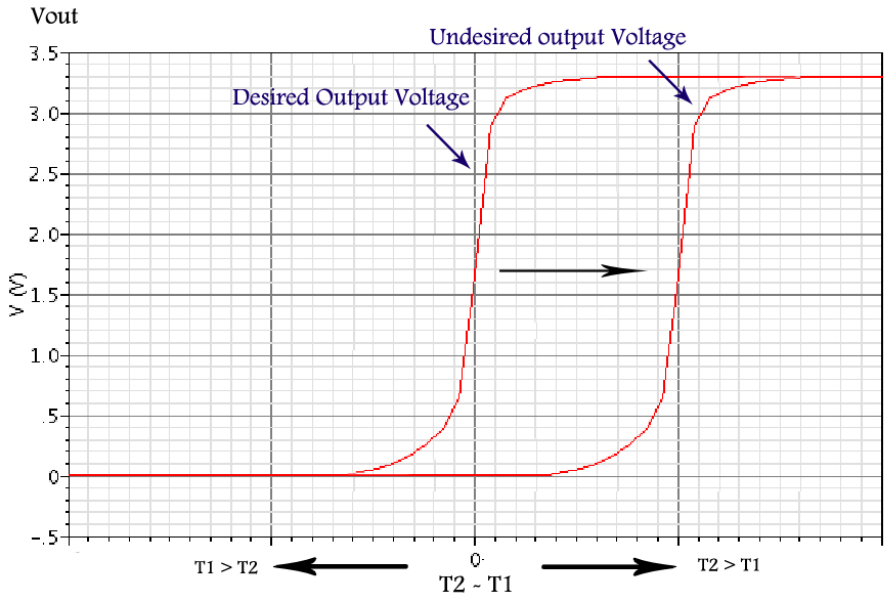

Fig 4-3. Output shifting as a result of process variation.

II) Beside process variation, there is another issue of concern which locally effects the temperature sensor operation which is device mismatching in the differential temperature sensors as a result of activation of other devices or circuits, different from the one under test, that are in the same silicon die and dissipate power. This power dissipation provokes that when the CUT does not dissipate any power, T2 is already different from T1. As a sensor is closer to the heat source, its influence on the closest sensor is higher. Eventually this changes in the temperature of different branches of the circuit causes mismatch and offset in voltage, current or temperature. As we had before,

$$Signal_{out} = S_D . (T_2 - T_1) + V_{Desired}$$

but as a matter of temperature changes in the transistors, let's assume:

$$M_1 : T_1 + \Delta T_1$$

$$M_2 : T_2 + \Delta T_2$$

$$(4-3)$$

where T_1 and T_2 are the temperatures of M1 and M2, that are sum of ambient temperatures and the temperature increase generated by the power dissipated by this device and ΔT_1 and ΔT_2 are the temperature increases at the temperature transducers' location caused by the activation of an internal heat source.

$$Signal'_{out} = S_D . (\Delta T_2 - \Delta T_1) + V_{Offset}$$

$$(4-4)$$

in which

$$V_{Offset} = V_{Desired} + S_D . (T_2 - T_1)$$

$$(4-5)$$

So by defining new definitions for transistors temperatures, we may finally end up with the following equation, which expresses the new output voltage in the existence of ambient temperature increase caused by the activation of an internal heat source.

$$V_{out} = S_D . (T_2 - T_1) + V_{offset}$$

$$(4-6)$$

The above-mentioned offset which is added to the desirable output voltage value can be shown exactly like the diagram of fig 4-3, in which the output voltage has shifted to the right or left.

III) Another issue of concern, that can affect the output DC voltage is the biasing voltage changes. If either of the biasing DC voltages changes, the differential pair gets unbalanced and mismatched which eventually causes DC offset at the output.

4.3. Quantifying the DC offset

A very important issue of concern is to control the DC offset in the Differential temperature sensors, because by controlling that, the dynamic range of the sensor can be adjusted. In the circuit analysis, for adjusting the dynamic range of the sensor and generally for doing the ac analysis, we need to work on the DC operation point of the circuit, in which the output voltage has to be adjusted and the DC offset has to be compensated.

Before compensating the DC offset, this offset has to be quantified and measured accurately. In this thesis, we chose activation of other devices in the same silicon die, that are dissipating power and cause ambient temperature changes between M1 and M2, as a source of DC offset to compensate it. Therefore, the purpose of this section is to quantify the DC offset occurred as a matter of thermal gradient in the sensor. For that, we have to add a heating source close to one the input differential pair MOS transistors, in order to change its temperature. By increasing the temperature of this MOS transistor, we are actually unbalancing the circuit manually. The DC offset that appears in the output is written as:

$$V_{offset} = V_{real} - V_{desired}$$

$$(4-7)$$

Actually, V_{offset} is the amount of voltage that needs to be added to or subtracted from the real output, in order to reach the desired output value.

In order to do the analysis, the differential temperature sensor of fig 4-1 is considered, in which M1 and M2 are MOSFET measuring sensors and V1 and V2 are the biasing sources of the sensors.

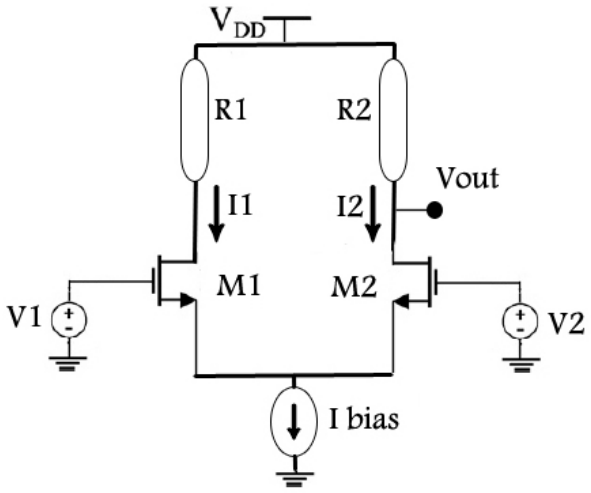

Fig. 4-1. CMOS Differential Temperature sensor schematic

We imagine that there is a power dissipating element next to M2 and its temperature increase is in respect to the amount of heat that the heating source produces. We consider this temperature variation to be from 30°C to 100°C. Although this is a big range of temperature variation, this is just a sample in order to cover a complete range of thermal changes.

In order to unbalance the circuit, the best way is to apply different temperatures for two sensors of the circuit so that by changing the applied temperature to two same transistors the output current of each of them will change respectively which eventually affects the balance of the whole circuit and causes mismatching. This temperature variation is exactly what happen as an existence of a heating source next to either of the measuring sensors (M1 or M2).

While changing temperature in two transistors of the input stage (sensors) of the circuit a problem came up which was the limitation of the Cadence software. In this software the ambient temperature of the circuit could be changed but only for all the elements of the circuit not for each of them separately and differently. As a result of this limitation the two input sensors of the circuit will always have the same temperature which does not cause any unbalance and changes in desired output voltage.

For solving this problem, we have to emulate the temperature changes with some other parameters of the circuit. As it is obvious the temperature variation in the sensor circuit directly affects the collector current of each transistors, so by knowing the parameters on which the collector current is depended, temperature changes can be emulated by that.

The collector current of the MOSFET transistor is depended on two parameters of temperature and gate-source voltage (biasing voltage):

$$\Delta I_d = \frac{\partial I_D}{\partial T} . (T - T_{nominal}) + \frac{\partial I_D}{\partial V_{gs}} . (V_{gs} - V_{gs,nominal})$$

$$(4-8)$$

from (3-5), we have:

$$S_T = \frac{\partial I_C}{\partial T}$$

and also,

$$\frac{\partial I_D}{\partial V_{gs}} = g_m$$

$$(4-9)$$

Therefore,

$$\Delta T = \frac{g_m}{S_T} . \Delta V_{gs}$$

$$(4-10)$$

Taking 4-9 into account, we can see that, there is a direct relationship between temperature changes in a MOS transistor and biasing voltage of it and also by changing the ambient temperature, the differential sensitivity changes. Thus, according to 4-9 the temperature changes in the circuit could be emulated by gate voltage changes of each transistor.

In order to observe the exact amount of temperature changes and hence current changes, in respect to the biasing voltage variation, the following procedure was chosen.

Firstly, a simple MOSFET was biased by a constant DC voltage source of Vbias, Fig. 4-5. By sweeping the ambient temperature of the circuit from 0°C to 100 °C, the output current changes was measured. The graph fig. 4-6 shows the output current changes by sweeping the ambient temperature of the circuit. In this case Vbias was always constant (Vbias=1 V).

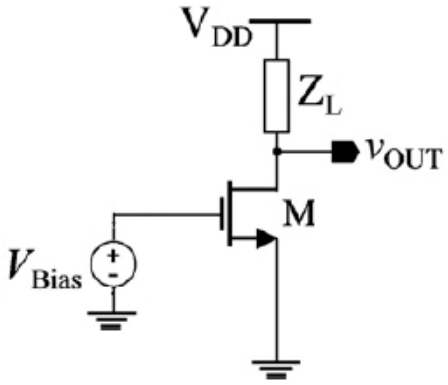

Fig. 4-5. Biasing a MOSFET

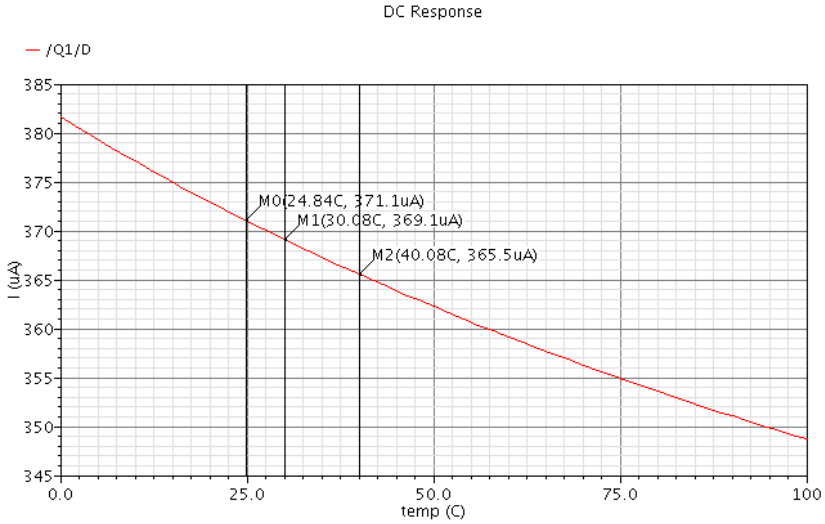

Fig. 4-6. Output current in respect to temperature changes

Although the current graph is not linear, for making the calculations easier I considered the current changes linear between the temperatures of 30°C to 40°C (in this range of temperature changes, the output current could be estimated by linear variation). So as it is shown in the fig. 4-6, the current difference in this temperature changes is measured:

$$T = 30°C \rightarrow I = 370\,\mu A$$

$$T = 40°C \rightarrow I = 365\,\mu A$$

$$(4-11)$$

So for each 10°C, temperature increase, there is 5 μA current decrease.

$$\Delta T = 10°C \rightarrow \quad \Delta I = 5\mu A$$

$$(4-12)$$

Secondly, by sweeping Vbias from 0 V to 3.3 V (Vdd), output current was measured. In this case temperature was constant as $T = 30°C$. After simulating this circuit with these features, fig. 4-7 was seen.

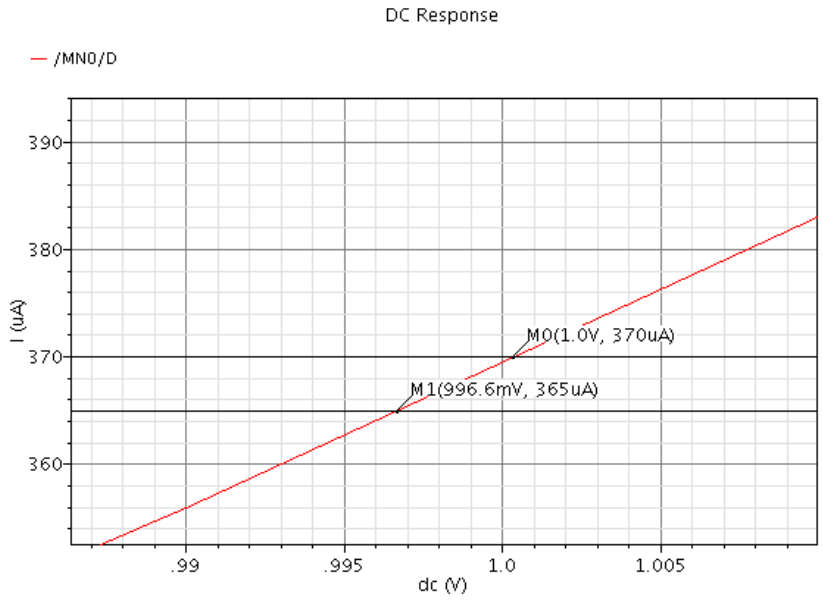

Fig. 4-7. Output current in respect to biasing voltage sweep

By applying the same calculations,

$$I = 370\,\mu A \quad \rightarrow \quad Vbias = 1\,V$$

$$I = 365\,\mu A \rightarrow Vbias = 996\,mV$$

$$(4-13)$$

Which means for each 5 uA current decrease the biasing voltage decreases 4 mV.

$$\Delta I = 5\,\mu A \quad \rightarrow \quad \Delta Vbias = 4\,mV$$

$$(4-14)$$

Finally, the result is that, in order to increase the temperature of one MOSFET, 10°C in the circuit separately, the biasing voltage of that transistor needs to be decreased 4 mV.

As a result of this emulation, the whole sensor circuit was implemented again in the constant temperature of T = 30°C , and Vbias = 1 V, and in order to sweep the temperature of the second sensor (M2) in the circuit between 30 – 100 °C, Vbias of that MOSFET was swept between 1 – 0.972 V.

In order to see the current changes in the circuit made of only two MOSFET sensors, fig 4-1 is brought again in this part. While I_{bias} is constant value of 100uA, I_1 and I_2 are expected to be the same and equal to 50uA in a balancing case. By sweeping the V2 between 1 – 0.972 V, I_1 and I_2 ,were measured separately.

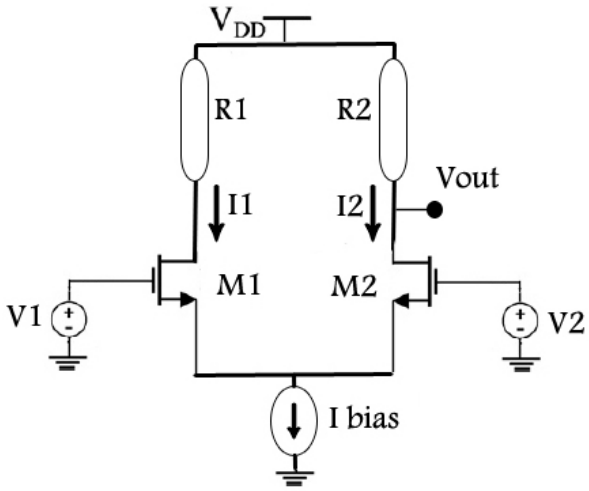

Fig. 4-1

It is obvious that by changing the V2 which is the biasing voltage of M2, we are changing the temperature of this transistor. Hence, output current changes and circuit get unbalanced. different currents for two transistors were measured and shown in fig. 4-9.

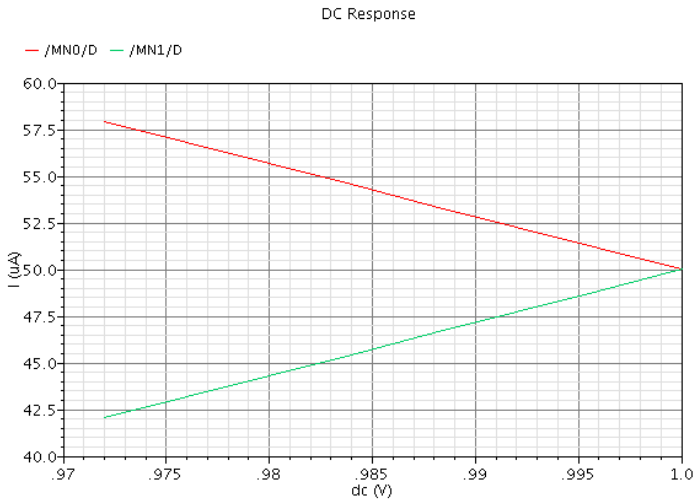

Fig. 4-9, Different Currents in different branches of input differential pair.

Eventually, the ΔI between two transistors as a matter of ΔT between them is shown in nominal values in table 2.

#	V_2	T_2	I_1	I_2	ΔI
1	1 V	30	50 uA	50 uA	0
2	0.996	40	51.14	48.86	2.28
3	0.992	50	52.27	47.73	4.54
4	0.988	60	53.41	46.59	6.82
5	0.984	70	54.52	45.48	9.04
6	0.980	80	55.81	44.19	11.62
7	0.976	90	56.86	43.14	13.72
8	0.972	100	57.93	42.07	15.86

table 2.

As it is presented in table 2 when V2=1 V, which means ambient temperature of M2 is T = 30°C , the two branches of the circuit are balanced so I_{bias} = 100 μA, is divided in to two same amounts of 50 μA into M1 and M2. As a result of this balancing ΔI = 0 μA, which means there is no current mismatching. But as V2 is decreased (In reality temperature of the M2 is increased), the less current goes into M2 branch and so the circuit gets unbalanced which causes mismatching at the output of the circuit. ΔI, could increase up to 15.8 μA, which at the worst case of this experiment ($T1$ = 30°C, $T2$ = 100°C, ΔT = 70°C,).

As a result of the current mismatching in the differential pair, the output DC offset comes up. Depending on the temperature difference between M1 and M2, following table shows the different offset values in output voltage of the circuit.

#	V_2 (V)	T_2 (°C)	ΔI (μA)	$Offset$ (mV)
1	1 V	30	0	0
2	0.996	40	2.28	130
3	0.992	50	4.54	263
4	0.988	60	6.82	395
5	0.984	70	9.04	520
6	0.980	80	11.62	660
7	0.976	90	13.72	745
8	0.972	100	15.86	895

table 4-3. Output DC offset for different temperature variation in M2.

As it is shown in the table 4-3, the output DC offset could be up to 895 mV, in the worst case in this example.

Eventually the graph in fig 4-10, is presented to show the output voltage of the main circuit in respect to variation of the biasing voltage of sensor M2. In ideal case, without having any external power dissipating element and process variation, V2 is the same as V1 which means both of them are in the same temperature. In this case the output voltage is Vdd/2=1.65 V, which is the desired value of the output that was discussed in the previous section. By increasing and decreasing V2 in some mV (ambient temperature changes because of heating source), DC offset appears in Vout. The changes between V2 and V1 can be presented by ΔV, so the same meaning graph is presented in fig 4-11.

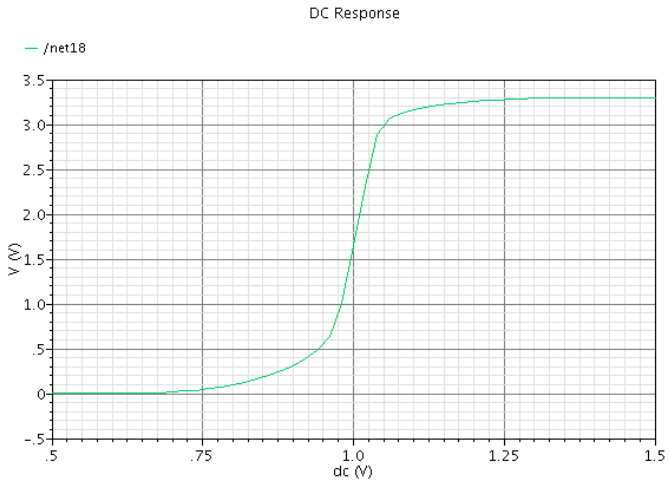

fig 4-10. Output voltage variation in respect to the biasing voltage of M2 variation

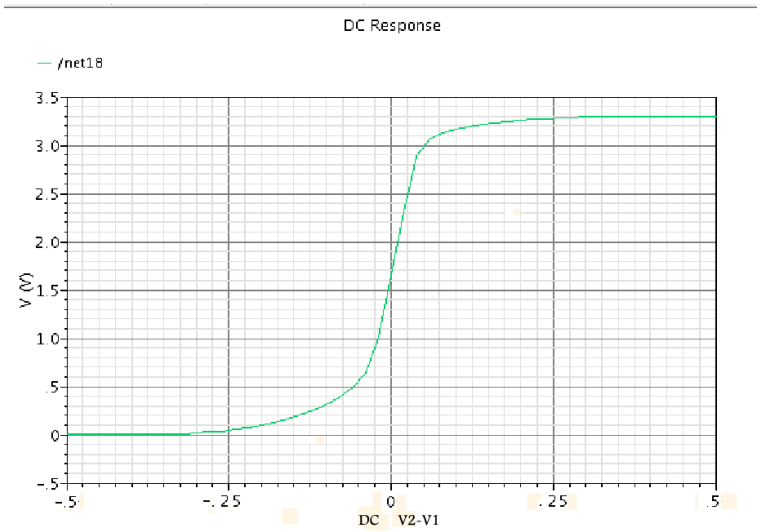

fig 4-11. output voltage variation in respect to the difference between biasing voltages of M1 and M2

When this circuit is implemented in a real situation, for instance in RF receiver, while behaving as a temperature sensor, the measured temperature of two sensors are different so by adding the above-mentioned offset and mismatches to the main operation of the circuit, the fig 4-11 or fig. 4-2 will be shifted to right or left which is the output offset and was shown before.

In the next section, conventional DC offset compensation methods are introduced.

4.4. Conventional offset cancellation method

In this section I am going to introduce two conventional methods of DC offset cancellation in the differential temperature sensors. Firstly, we have the previous mentioned samples of differential sensors which were mentioned in chapter 3, (Fig 3-4).

In these sensors two other transistors of MP1 and MN1 are added to the sensor in order to adjust the output voltage and to compensate for the thermal offset which result from device mismatching. Fig 4-12 shows the sensors after applying the compensation method. The proposed technique was introduced in the work [5].

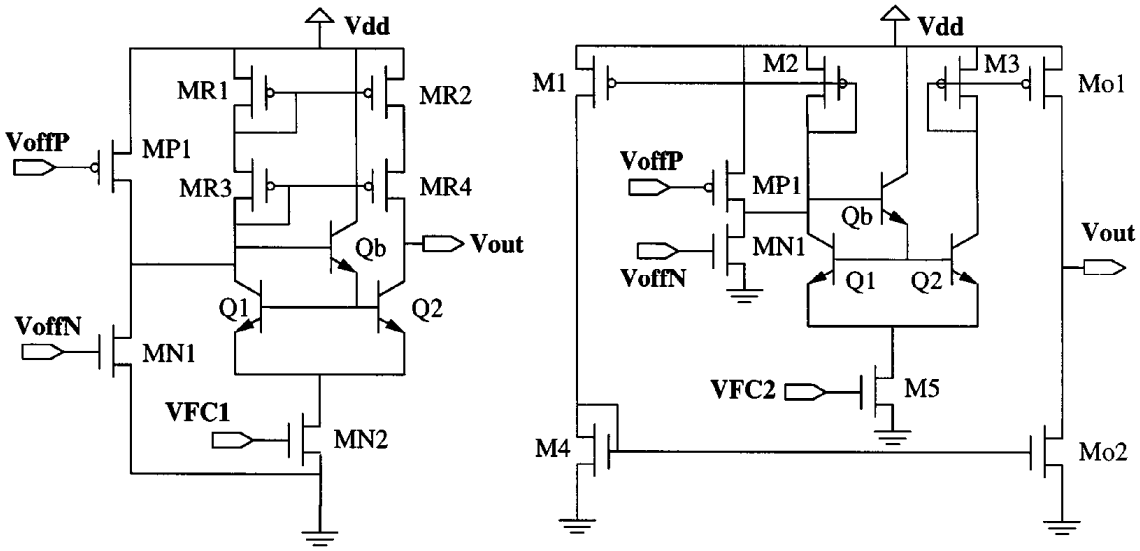

Fig4-12. BiCMOS sensors after applying DC offset cancellation method

Secondly, another conventional Dc offset compensation is brought in the work [6]. In this work, two calibration current sources are added to the sensor circuit in order to inject the current from both side of the circuit in case there is current mismatching in the differential pair. Fig. 4-13 shows the schematic of this method to compensate offsets by I_{cal1} and I_{cal2}.

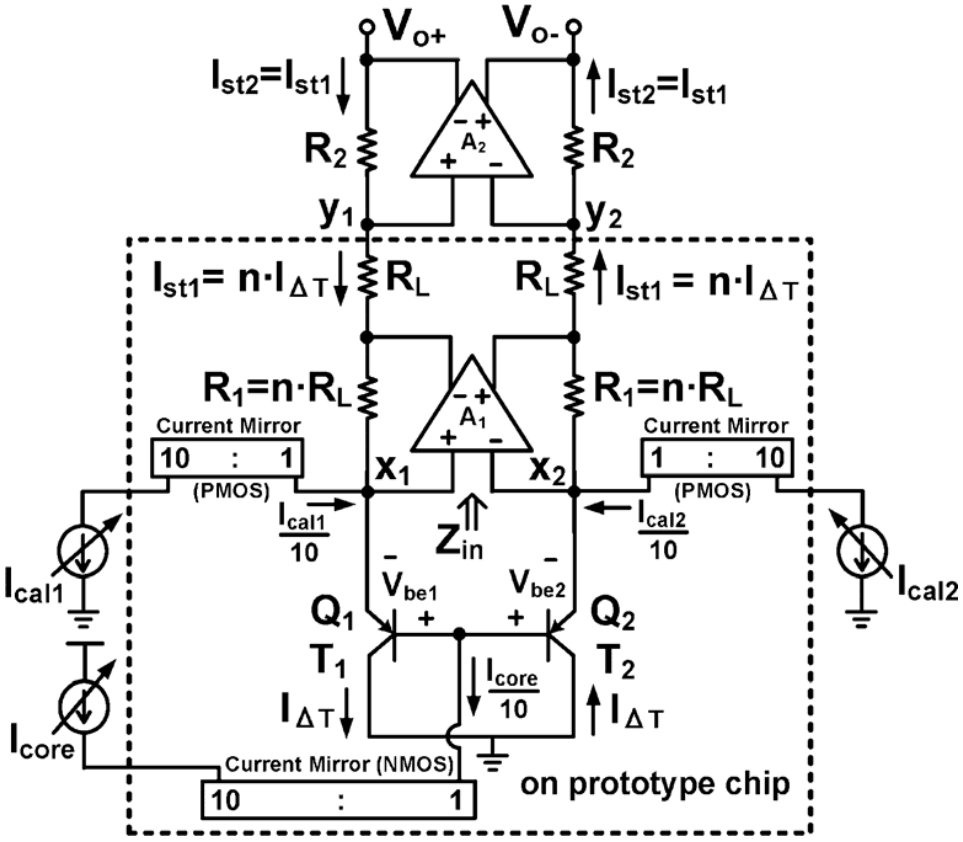

Fig 4-13. conventional offset compensation method brought in work [6]

I_{cal1} and I_{cal2} are the variable current sources which are mirrored by a current mirror of 10 : 1, that causes I_{cal1} and I_{cal2}, to be decreased 10 times. Thus, in practice, $\frac{I_{cal1}}{10}$ or $\frac{I_{cal2}}{10}$, are added to the appropriate branch.

In the both above-mentioned techniques, the compensation is done manually. Depending on the existing DC offset at the output (current mismatching at the input pair), different amounts of current has to be injected manually each time. In the proposed technique shown in this thesis, the automatic DC offset cancellation is presented and explained.

4.5. References

[1] Patrick Drennan, "Understanding MOSFET Mismatch for Analog Design" ***IEEE Journal of Solid-State Circuits, Vol 38, No 3,*** **March 2003 http://www.solidodesign.com/uploads/drennan-mismatch.pdf**

[2] W. Shockley, "Problems related to p-n junctions in silicon." ***Solid-State Electronics, Volume 2,*** **January 1961, pp. 35–67.**

[3] W. Schemmert, G. Zimmer, "Threshold-voltage sensitivity of ion-implanted m.o.s.transistors due to process variations." ***Electronics Letters, Volume 10, Issue 9,*** **May 2, 1974, pp. 151-152**

[4] "Managing Process Variation in Intel's 45nm CMOS Technology." ***Intel Technology Journal, Volume 12, Issue 2*** **June 17, 2008http://www.intel.com/technology/itj/2008/v12i2/3-managing/1-abstract.htm**

[5] J. Altet, A. Rurio, E. Schaub, "Thermal Coupling in Integrated Circuits: Application to Thermal Testing" IEEE Journal of Solid State Circuits, vol.36, no, 1, January 2001

[6] M. Onabajo, J. Altet, E. Aldrete, D. Mateo, J.Silva-martinez, "Electrothermal Design procedure to Observe RF Circuit Power and Linearity Characteristics With a Homodyne Differential Temperature Sensor" IEEE Transaction on circuit and systems, vol. 58, no.3, March 2011

5. Proposed Technique for offset cancellation

5.1. Introduction

As it was described in the previous chapter, one of the offset compensation methods was adding current to one branch of the differential pair in order to balance the current passing through both sensors and compensating the current changes due to some external reasons like process variation or power dissipation of adjacent elements which act as heating sources. Although the mismatching was cancelled in the circuit, all the calibrations were done by an external biasing source manually.

In the proposed technique, an automatic method of offset cancellation is presented which could be as much accurate if it is necessary. Firstly, a very simple and immature schema of this method is shown in Fig. 5-2. We considered the simple differential sensor of fig 5-1 to apply the technique on. The transistor dimensions are given in table 5-1.

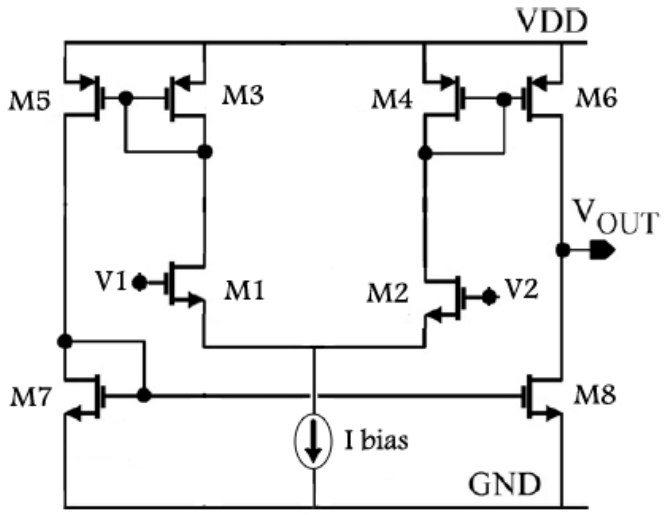

Fig. 5-1 A CMOS differential temperature sensor

This circuit is designed in AMS 0.35 um technology in which M1 and M2 are MOSFET measuring sensors, M3 and M4 are current mirrors and M5 to M8 are output stages to increase the output resistance. V1 and V2 are the biasing sources of the sensors. The circuit is designed in AMS 0.35 um technology with the following sizing. (Vdd = 3.3 V)

MOSFET	W	L
M1	10	0.35
M2	10	0.35
M3	10	0.35
M4	10	0.35
M5	87	0.35
M6	87	0.35
M7	3.8	0.35
M8	3.8	0.35

Table 5-1

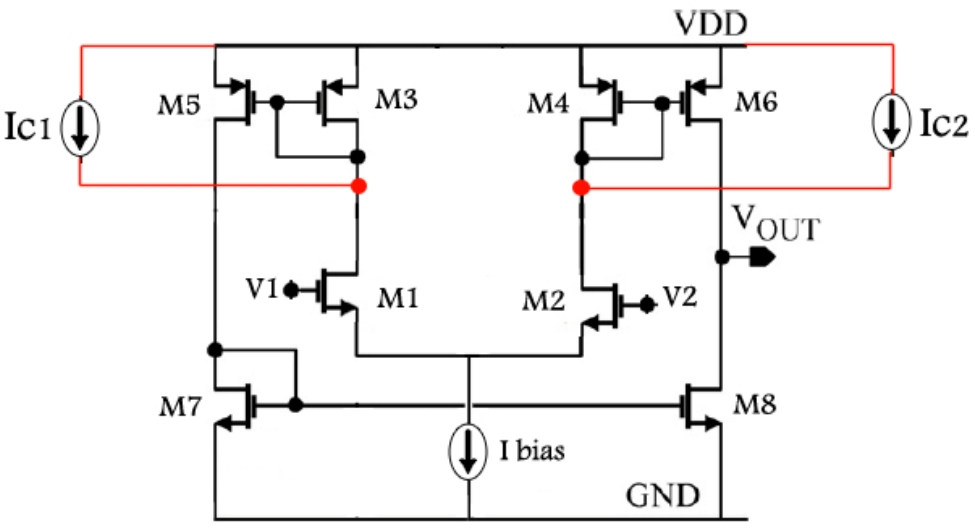

Fig 5-2 Immature schema of the proposed method for DC offset cancellation

In the proposed schematic, M1 and M2 are MOSFET sensors, V1=1 V (constant) and V2 varies between 972 mV and 1 V, in order to emulate the temperature changes of $30 - 100\,°C$, and Ibias = 100 uA (constant), and I_{c1}, I_{c2} are compensating current sources added to each branch of the circuit which needs current to balance the differential pair.

The temperature change of up to 100 °C, is just one consideration that I made to do the calculations and simulate the circuit. This temperature can change below 30°C, or higher than 100 °C, but as a general thought, as this temperature change is as a result of heating source, so it might not get less than 30°C, which is the ambient temperature of the circuit. So it always could be more than the ambient temperature of the sensor.

The idea is to add or subtract current from one branch of the differential pair in order to cancel current difference in the sensors. The value of the current sources I_{c1}, I_{c2} can change in respect to the current needed which varies by temperature variation in each branch. Some measurements have been done which are discussed in details in the next chapter. some of these measurements and experimental result are shown here to make the situation clear.

by changing the temperature from 30 $-$ 100 °C, Vout is changed from 1.65 V to 0.815 V. This is a DC offset of around 835 mV in the worst case (temperature difference of 70°C,). This offset is quite high which may drive the sensor into saturation. The measured current difference between differential pair was 0 uA in the best case (both sensor are in the same temperature of 30°C,) and it was 15.8 uA at the worst case (temperature difference of 70°C,).

Considering the current needed to add to one branch, as it was seen before, its value could change between 0 to 15.8 uA. By calibrating this current source to a value in this range the offset could be reduced dramatically. After applying this technique the output changes between 1.65 V , (the best case for 30°C, in sensor 2) and 1.54 (the worst case for 100°C, in sensor 2). This results shows that after applying this technique, the offset changed from 835 mV to 110 mV in the worst case. It means the offset got 13% of its previous value which is quite acceptable.

5.2. Calibration of injected current

In the previous section a very simple offset compensation method was presented using current sources to add or subtract current two either of the differential pair branches. As we it was seen in the table 4-3, according to the temperature increase in one transistor, there are different current differences between two sensing devices. Thus, a flexible calibration method is required to add or subtract current depending the desired value of current injection. Here I am presenting a way to calibrate these current sources to each necessary value by using current mirrors and switches to change the value of adding or subtracting current to the branches.

In Fig 5-3 the beginning idea of current mirrors are presented to get different currents from a unique current source of I_{ref}. This I_{ref} could be a very small value which can set the accuracy of variation in the current ejected. As it is shown in this figure the injected current to the sensors could vary from 0 uA to $[n.I_{ref} + (n-1)I_{ref} + \ldots + I_{ref}]$.

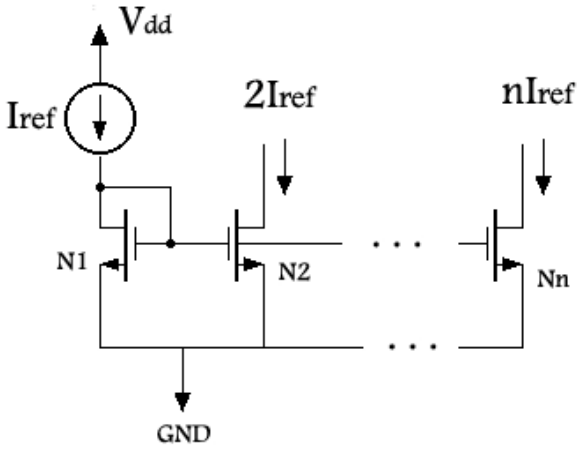

Fig 5-3 Current mirrors method

Thanks to the basic idea of the mirroring current, each branch of the circuit has the current related to the width of its MOS transistor. The current of each transistor is depended on two elements of gate-source voltage and transistor size. Because all the MOS transistors are having the same gate-source voltage, easily by changing the transistors width, we can take the desired value of current. The simplified model of the current in saturation region for MOS transistor is shown in 5-1:

$$I_D = \frac{1}{2}.\mu_n.C_{ox}\left(\frac{W}{L}\right)(V_{gs} - V_{th})^2$$

$$(5-1)$$

where $\mu_n, C_{ox}\ and\ V_{th}$, are mobility of the electrons, gate oxide capacitor and threshold voltage of the transistor respectively, and they don't change in the different circuit structures. So as it was said before, I_D is depended on $\left(\frac{W}{L}\right)$ and V_{gs}. by having the constant V_{gs}, in all the mirror branches and changing the transistor widths, different amounts of currents could be taken from each branch. For instance, in the fig. 5-3, N2 has the width of two times bigger that N1, and N3 two time more than N2, and so on.

$$\left(\frac{W}{L}\right)_1 = \frac{1}{2}.\left(\frac{W}{L}\right)_2 = \frac{1}{4}.\left(\frac{W}{L}\right)_3 = \cdots$$

$$(5-2)$$

The secondary idea of the current injection is to as some switches to each current mirror branch in order to turn it on or off, so that by turning on each current mirror, its value will be added to the whole amount of injected current. The proposed idea is shown in Fig. 5-4

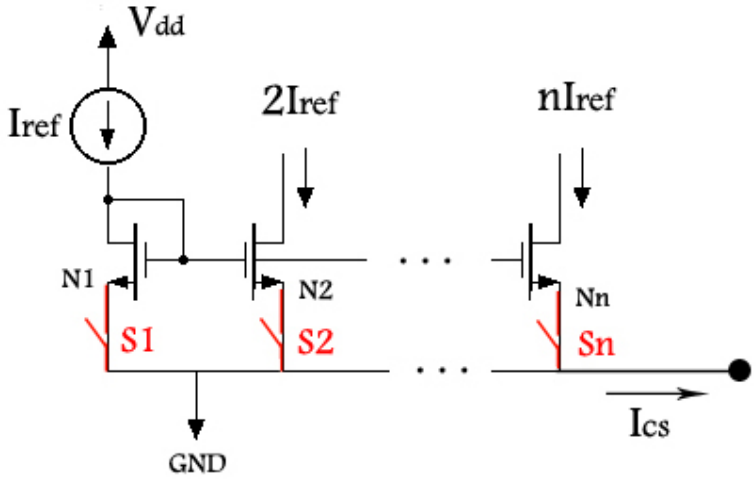

Fig 5-4 Current mirror with controlling switches

where S1, S2, ... and Sn are the switches for I_{ref}, $2I_{ref}$, ... , $(n-1).I_{ref}$ and $n.I_{ref}$ respectively, and I_{cs}, is the injected current to each branch of differential pair in the sensor. All this schematic is going to be replaced by the current source which was shown in the beginning of this chapter in fig 5-2.

According to the this theory, I_{cs} could change with this formula:

$$I_{cs} = I_{ref} . \sum_{i=0}^{n} 2^i . b_i$$

$$(5-3)$$

where I_{cs} is the whole ejected current to one branch of the differential sensor, I_{ref} is the reference current source, b_i is each number branch of the current mirror that can be on ("1") or off ("0"), n is the number of current mirror branches which is optional. So the value for I_{cs} is:

$$I_{cs} = I_{ref}.[b_0 + 2b_1 + 4b_2 + \ldots + 2^n.b_n]$$

$$(5-4)$$

The accuracy of the injected current depends on I_{ref} and the maximum amount of injected current is depended on n. So as I_{ref} is smaller and n is bigger, the highest range of current with smaller steps could be added to the circuit.

Finally a complete circuit with these current mirrors are shown in Fig 5-5

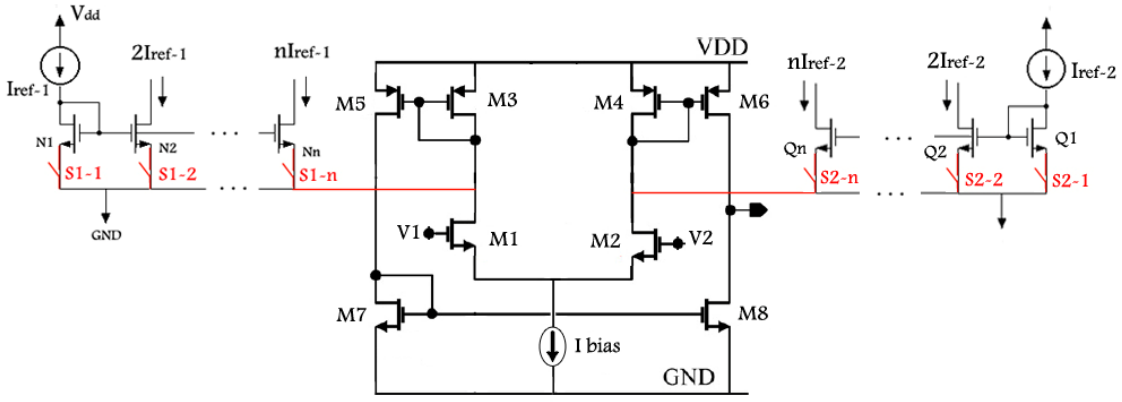

Fig. 5-5 General schematic of the proposed technique for DC offset compensation

where $I_{ref1}\ and\ I_{ref2}$ are the reference current sources for two sensors which are mirrored by different coefficients. Depending on the mismatch on each pair of the input, either S1 or S2 set of switches start working.

To sum up, we have two binary words for controlling the current sources of each branch. According to the necessity of current injection to each branch of the circuit, each of these binary words are activated. each of these binary words says which branches of the current mirrors have to turn off and on, in order to add the desired value of current.

Next section presents an automatic offset cancellation method which provides a close loop operation that is always controlling the output of the temperature sensor and eject the necessary current to each branch.

5.3. Automatic offset cancellation

Up to now, a CMOS differential built-in temperature sensor has been designed and discussed regarding some unexpected limitations which may exist in the simulation and fabrication called process variation, external heat sources and device mismatching. These issues cause the differential pair to be unbalanced and mismatched which finally end up with current mismatching and DC offset in output. In order to solve this problem, two current sources were added to two differential pairs of the circuit in order to add or subtract current to/from each branch. According to the current we need, the current sources are calibrated. Then, by using current mirror theory, some different value of current could be provided to be injected proportionally. In this method a reference current source of I_{ref} is being mirrored by different coefficients and each branch of these mirrors was controlled by a switch in order to turn it on or off. So according to the number of the branches in current mirror and the value of I_{ref} , different ranges of current with different accuracy could be injected to each branch of the circuit.

The limitation with the idea is that this compensation circuit is calibrated once for specific current to be injected and if there is still some offset, the calibration has to be done again manually, that means for each specific application, its unique calibration has to be done manually. In the proposed technique, an automatic compensation method is presented in order to calibrate the circuit and inject the current for any different application and different temperature variation. Furthermore, in one specific application the output voltage is measured concurrently and compared with its desired value. If there is still mismatching that cause offset, the value of the current which is needed will be injected to each branch and then the output will be measured. So a closed loop circuit is designed in order to check the output when the calibration is necessary, and comparing it with the desired value and calibrate the current injection.

The first step is to measure the DC output voltage of the circuit and convert it to a digital value. For this purpose a simple Analog to Digital converter is used. According to the required accuracy for the output this A/D converter may be 16 bits, 32 bits or more. Fig 5-6 shows the A/D and its input and output signals.

Fig 5-6. A/D and input output signals

where Vout is the output voltage of the differential temperature sensor, and V_{AD} is the output digital signal from A/D.

The next step is to compare this digital value with the desired value of the sensor. This comparison is done digitally in this method. Obviously, in order to reach the exact desired value for the output with DC offset of sharp zero, a very accurate current injection is needed and also I_{ref} needs to be very small and too many branches for mirroring current is required. Actually, reaching the zero offset is impossible because there is always some mismatching and some internal errors (width and length changes of the transistor in fabrication, ambient temperature changes of the sensors because of some other elements and etc.) which makes the circuit a little bit unbalanced. So according to the required accuracy and minimum acceptable offset for the application, the circuit is designed.

Generally, in any application, there is an acceptable range of output variation in which the operation of the circuit is concerned as ideal. This output voltage variation could be in some mV or some hundreds of mV due to the importance of required output accuracy. For instance, in this specific presented circuit, the acceptable output variation is concerned between (1.5 V - 1.8 V) because Vdd = 3.3 -----> Vdd/2 = 1.65 .

So two values of V_{refH} and V_{refL} are the maximum and minimum acceptable values of the output that are concerned for the comparator input. So V_{AD} (output of A/D) is always compared with these two values. Fig 5-7 shows the comparator and its input and outputs. According to the output of the sensor, the compensation process could follow one of the following cases.

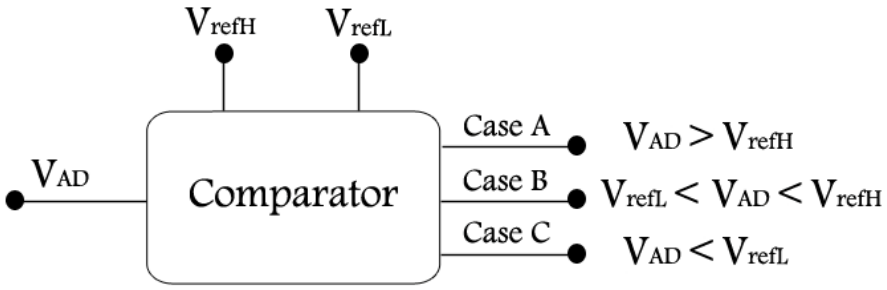

Fig 5-7. Comparator signals

Initially V_D is compared with V_{refH}.

i) Case A: if $V_D > V_{refH}$, it means that the circuit has an offset of more than acceptable value and it has to be compensated.

But if $V_D \leq V_{refH}$, there are two possibilities:

ii) Case B: $V_{refL} \leq V_D \leq V_{refH}$, in this case the output is in the desired range and no compensation is required.

iii) case C : $V_D < V_{refL}$, it means that the circuit has an offset of more than acceptable value and it has to be compensated.

As it was discussed before, in two situations of "case A" and "case C", the compensation is required. Obviously, depending on if case A is happening or case C, current has to be injected to the left or right branch respectively (sensor 1 or sensor 2). But the idea is to add current in very small steps (I_{ref} in each step) and check again if the offset is in the acceptable range or not. If the offset is compensated and the output voltage is now in the desired range (V_{refL} and V_{refH}), compensation is finished, but if output is not in the desired range, another small amount of I_{ref} is added to that branch. Of course each of these steps are happening after some mili seconds of pause, so that the new output is applied to the circuit, and then output is checked, converted to digital value, and compared with V_{refL} and V_{refH}. This process continuous until the desired range of acceptable output is measured.

For adding the current into differential pair branches step by step, two counters are used for each branch. In each step of current injection, the used counter's value increases one step. Number of bits for the counter is totally depended on the maximum probable value of offset and the reference current source as well. These counters are directly controlling the switches designed to turn the current mirror branches on and off. So for instance, if there are four branches of current mirroring, four switches (S_0, S_1, S_2, S_3) are used to turn on/off each branch (to count from I_{ref} to $15I_{ref}$.)

$$I_{cs} = I_{ref} . \sum_{i=0}^{3} 2^i . b_i$$

$$I_{cs} = I_{ref} . [\, b_0 + 2b_1 + 4b_2 + 8. b_3]$$

for instance if the compensation is finished after three times adding I_{ref}, at the end S_0, S_1, are "on" and S_2, S_3 are "off". Hence:

$$I_{cs} = I_{ref} . [\, 1 + 2. (1) + 4. (0) + 8. (0)] \rightarrow I_{cs} = 3I_{ref}$$

Fig 5-8 shows the general schematic of this procedure after getting the digital output from A/D up to getting the counter outputs to control the switches of current mirrors.

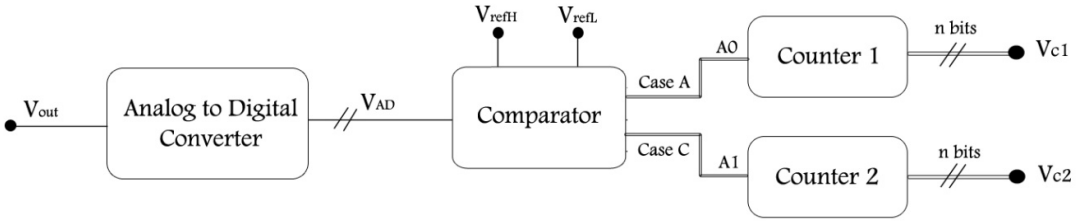

Fig. 5-8, Schematic of selection process to turn the current mirrors controlling switches on/off

where A_0 and A_1 are the controlling switches of the counters. Depending on if case A or C is happening, A_0 or A_1 turns on. Since in case B, no compensation step is required to be done, we don't show that in the output of the comparator. Table 5-2 shows the different values for comparator outputs, A_0 and A_1, which are the controlling signals for counters.

A0	A1	Counter 1	Counter 2	Case
0	**0**	Do nothing	Do nothing	**B**
0	**1**	Enable	Disable	**C**
1	**0**	Disable	Enable	**A**
1	**1**	-	-	**-**

Table 5-2, Different comparator outputs for controlling counters

Tables 5-3 shows the n bits counters outputs values to control the current mirror switches for each branch of the current injection.

S0	...	S(n-1)	Sn
0		**0**	**0**
0		**0**	**1**
0		**1**	**0**
0		**1**	**1**
...		**...**	**...**
1		**0**	**0**
1		**0**	**1**
1		**1**	**0**
1		**1**	**1**

Table 5-3. VC1, Counter 1 output

Depending on the number of current mirrors to select the accuracy and current injection range, *"n"* could change. For the previous example in which we had four current mirror, we have n=3.

In order to make the procedure clear, a Finite State Machine (FSM) of it is drawn in fig 5-9. As it is shown, first there is a waiting state when start switch is "0". By turning start into "1", the comparing process starts. Obviously the comparison operation is always happening in order to compare the output digital value with two reference voltages. Although in case B, when $V_{refL} \leq V_D \leq V_{refH}$, no compensation is required, the comparison happens each 10 seconds, because there is the possibility of temperature increase in either of the sensors as a result of external elements heating. As it was discussed before 2 mS wait in vase A and C is the marginal time dedicated to the output to be updated.

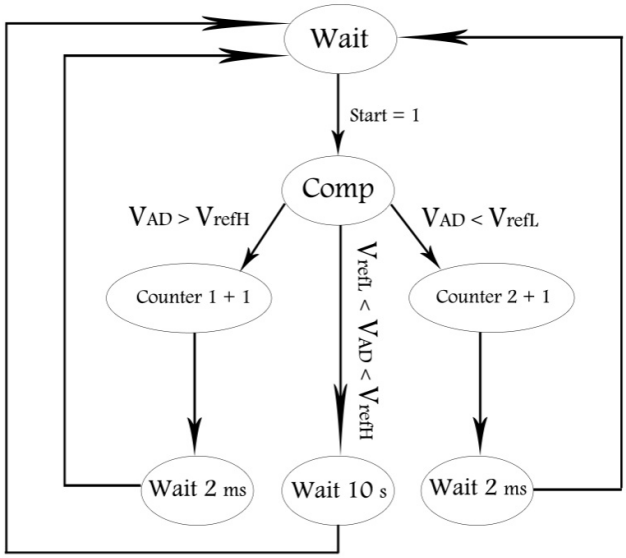

Fig. 5-9, Finite State Machine for the close loop structure

Fig 5-10 presents the whole closed loop schematic of the proposed technique with all the details.

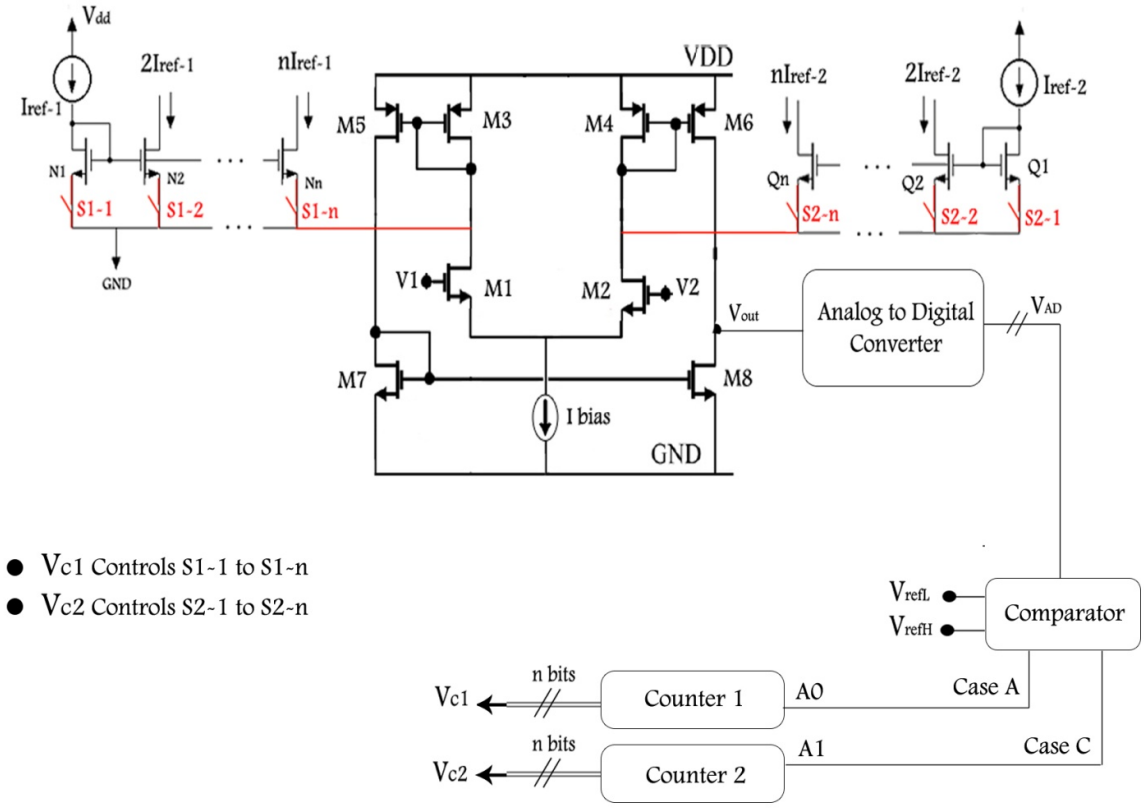

Fig. 5-10, The complete schematic of the proposed automatic DC offset cancellation method

In the next section, some experimental results and measurements are shown for different biasing values and different cases. These results will also be compared with the circuit results without applying the proposed technique.

6. Simulation Results and Discussion

6.1. DC offset measurements without applying the cancellation technique

In this chapter the experimental results are shown in order to see the circuit operation before and after applying proposed technique for offset cancellation. Firstly, a simple circuit of differential temperature sensor is simulated in the 0.35 um technology in Cadence (Fig 6-1). The circuit is designed so that when equal bias voltages of (1 V) is applied to the circuit, the output will be half of the Vdd. The transistor sizes and current bias of the circuit is shown in table 6-1. As we discussed in chapter 4 the temperature changes of one sensor, as a result of power dissipation of adjacent elements which act as a heating source, is emulated by gate voltage changes of that sensor.

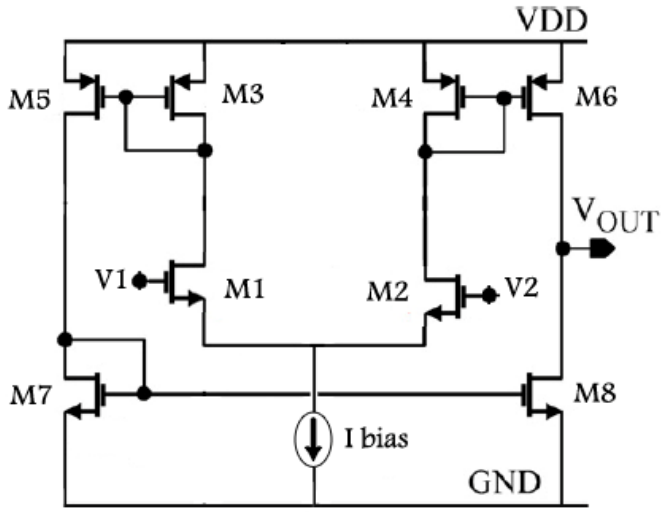

Fig. 6-1, CMOS Differential Temperature sensor schematic without applying proposed technique

MOSFET	W	L
M1	10	0.35
M2	10	0.35
M3	10	0.35
M4	10	0.35
M5	87	0.35
M6	87	0.35
M7	3.8	0.35
M8	3.8	0.35

Table 6-1, Transistor sizes of the mentioned sensor

After sweeping the temperature of M2, emulated by bias voltage sweep, we end up with the following table, which shows the voltage and current offset in the output of the circuit. The current difference between differential pair is the required amount of current which has to be injected to the circuit. Eventually due to this current difference in the differential pair, the DC output voltage varies around the desired value. By increasing the temperature difference of two sensors, the output goes further than desired value and the offset gets higher.

#	V_1 (V)	T_1 (°C)	V_2 (V)	T_2 (°C)	$\Delta I = I_2 - I_1$ (μA)	$Offset$ (mV)
1	1	30	1 V	30	0	0
2	1	30	0.996	40	2.28	130
3	1	30	0.992	50	4.54	263
4	1	30	0.988	60	6.82	395
5	1	30	0.984	70	9.04	520
6	1	30	0.980	80	11.62	660
7	1	30	0.976	90	13.72	745
8	1	30	0.972	100	15.86	895

table 6-2. Output DC offset in voltage and current for temperature variation in M2.

Fig 6-2, is the diagram of the output voltage and differential pair currents as a function of V_2 , after variation of T_2 between 30 to 100 °C.

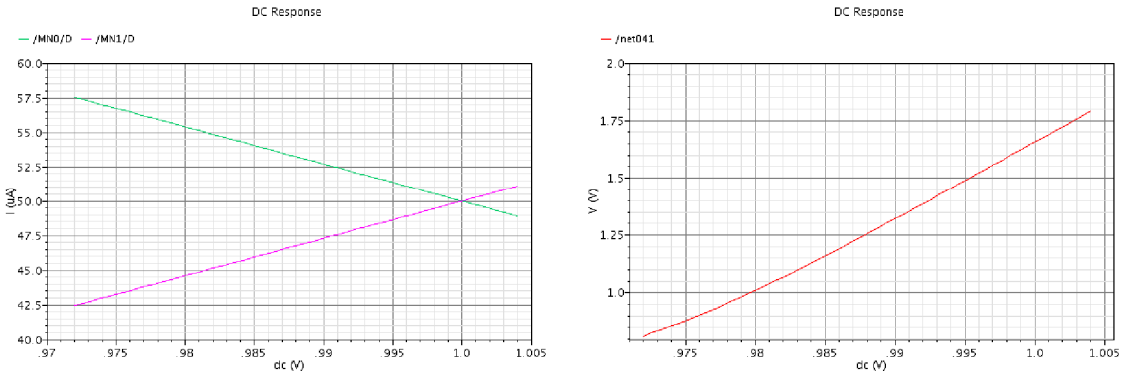

Fig. 6-2, Output voltage and differential pair currents as a function of V2

As we can see in fig. 6-2, the output voltage is at desired value of vdd/2 = 1.65 (V), when the temperature of T_2 = T_1. By increasing the temperature of M2 (decreasing the gate voltage of M2), the output decreases and the output offset increases.

In the next section the above-mentioned parameters are calculated after applying proposed technique.

6.2. DC measurements after applying current injection manually

For compensating this current and voltage firstly the same values as the ΔI was injected manually through the current mirror added in fig 6-3. The results were seen which reduces the output offset dramatically. these experiments are shown in Table 6-3.

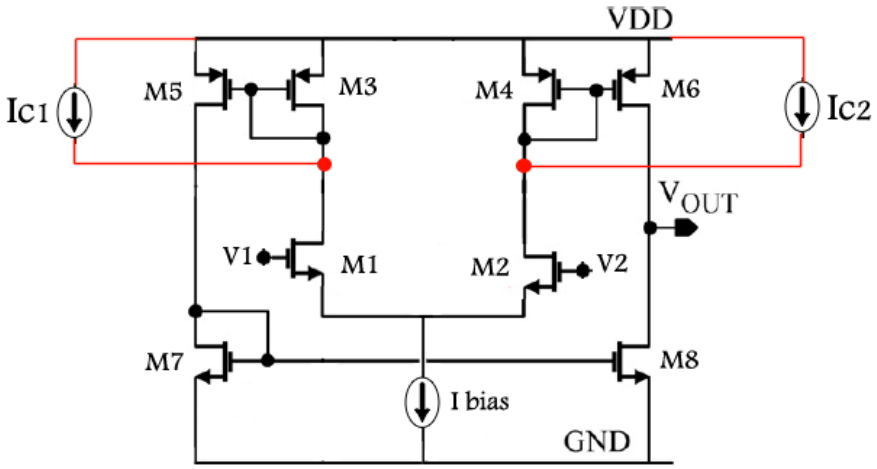

Fig 6-3, Manual Current injection method in temperature sensors

#	V_2 (V)	T_2 (°C)	$I\ injected$	$New\ Offset\ (mV)$
1	1 V	30	0	0
2	0.996	40	2.28	10
3	0.992	50	4.54	30
4	0.988	60	6.82	45
5	0.984	70	9.04	60
6	0.980	80	11.62	70
7	0.976	90	13.72	90
8	0.972	100	15.86	110

Table 6-3, New offset value after injecting current manually.

As it is shown in table 6-3, when the current difference of differential pair increases, the compensation gets less effective which can be interpreted as acting nonlinearity of the circuit operation in very high temperatures.

Table. 6-4, compares the DC offset before and after the manual current injection.

#	V_2 (V)	T_2 (°C)	$Old\ Offset\ (mV)$	$New\ Offset\ (mV)$
1	1 V	30	0	0
2	0.996	40	130	10
3	0.992	50	263	30
4	0.988	60	395	45
5	0.984	70	520	60
6	0.980	80	660	70
7	0.976	90	745	90
8	0.972	100	895	110

Table 6-4, Voltage Offset before and after manual current injection

The red columns in the table 6-4 shows that the offset is reduced down to about 10%. So if we can add this current amounts in a calculated way but not one by one, the offset could be reduced to 10%. In the next section the results of the idea of current mirrors and reference current source are shown. So that, just by setting the I_{ref} value and number of bits to cover all the necessary range of compensation, the compensation can be done.

It has to be emphasized that the injected current can be in both sides of the differential pair, regarding the temperature changes of the sensors. All the results are shown here just in one side of the circuit in order to make them clear and easier but this technique is applicable for both sides.

6.1. DC offset measurements after applying the proposed technique

Now current injection using current mirrors and controlling switches are being applied to the circuit. Primarily, the number of current mirrors has to be discussed in order to adjust the accuracy and the range of the current injection. As it was presented before, the minimum current difference for 10 degrees of temperature changes, was 2.2 uA. Of course by changing the temperature smaller (5 degrees or 2 degrees) this current difference could be less. However, for this special experiment we have this amount of ΔI as minimum, so I_{ref} = 2.2 μA. On the other side, the maximum required current in this case is about 15.2 uA, so by applying formula 5-3 and 5-4 the value of (n) can be 2, in order to have three current mirrors and three switches.

$$I_{cs} = I_{ref} . \sum_{i=0}^{n} 2^i . b_i$$

where n=2 and $I_{ref} = 2.2\ \mu A$

$$I_{cs} = 2.2\ \mu A . \sum_{i=0}^{2} 2^i . b_i$$

$$I_{cs} = I_{ref} . [b_0 + 2b_1 + 4b_2] = 2.2\ \mu A . [b_0 + 2b_1 + 4b_2]$$

when all switches are off $(b_0 + 2b_1 + 4b_2) = 0$, it means no compensation is needed (Case B)

Table 6-5 shows the different current injection values for different switches conditions.

#	V_2 (V)	T_2 (°C)	$b_2b_1b_0$	I_{cs} (μA)
1	1 V	30	0 0 0	0
2	0.996	40	0 0 1	2.2
3	0.992	50	0 1 0	4.4
4	0.988	60	0 1 1	6.6
5	0.984	70	1 0 0	8.8
6	0.980	80	1 0 1	11
7	0.976	90	1 1 0	13.2
8	0.972	100	1 1 1	15.4

Table 6-5. Different current injected values in respect to the control word.

Thus by applying the control word for controlling the switches of current mirrors, after simulating the circuit with this compensation method, the results of new output value and new offset were seen in table 6-6.

#	V_2 (V)	T_2 (°C)	$b_2b_1b_0$	I_{cs} (μA)	New Vout (V)	New Offset (mV)
1	1 V	30	0 0 0	0	1.65	0
2	0.996	40	0 0 1	2.2	1.644	6
3	0.992	50	0 1 0	4.4	1.632	18
4	0.988	60	0 1 1	6.6	1.62	30
5	0.984	70	1 0 0	8.8	1.606	44
6	0.980	80	1 0 1	11	1.59	60
7	0.976	90	1 1 0	13.2	1.58	70
8	0.972	100	1 1 1	15.4	1.57	80

Table 6-6, Vout and new offset values after applying the proposed current sources technique.

where the maximum offset has reduced to 80 mV which is quite acceptable. Fig 6-4 is the diagram of the desired output voltage, real output voltage before compensation and the

new output voltage after proposed technique in offset compensation, as a function of $T_2 - T_1$.

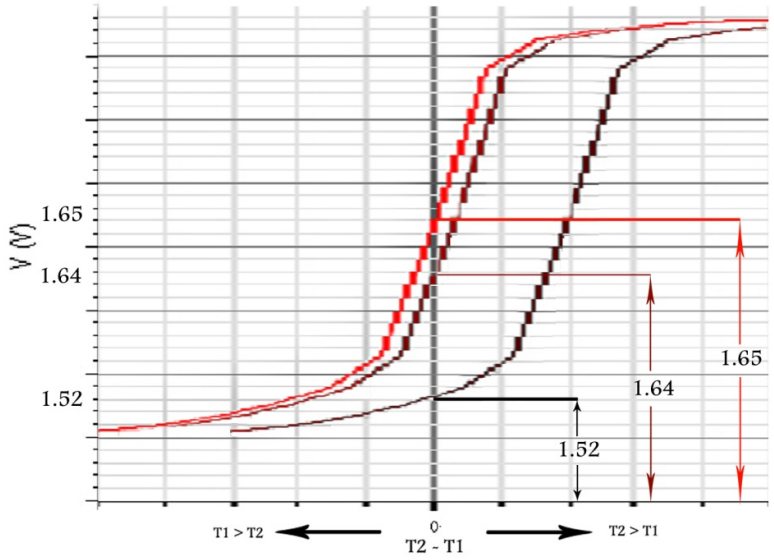

Fig. 6-4, i)Light Red Diagram: Desired output function, ii)Dark Red Diagram: New output after applying proposed technique. iii) Black Diagram: Real output before applying the technique.

As we can see from fig. 6-4, the real diagram before applying the compensation technique has the value of 1.52 (V), when T1=T2, which presents the 130 (mV) offset, and after compensation, this value reduced to 10 (mV).

6.4. New analysis with different Biasing current.

In the previous experiment I_{bias} = 100 μA and I_{ref} = 2.2 μA, it shows that :

$$I_{ref} = 2.2\ \%\ of\ I_{bias}$$

Now, new experiments are done by changing I_{bias} to 50 uA.

For having this amount of I_{bias} we need to change the transistor sizes in order to reach balance the circuit and have Vdd/2 in the output. The new transistor design of the circuit if shown in table 6-7.

MOSFET	W	L
M1	10	0.35
M2	10	0.35
M3	10	0.35
M4	10	0.35
M5	124.6	0.35
M6	124.6	0.35
M7	3	0.35
M8	3	0.35

Table 6-7, New transistor sizes for new amount of biasing current

In this case, by sweeping the temperature of M2 (gate voltage of M2), the differential current mismatch is different from the previous case. Thus, the necessary injected current to each branch is different, and eventually the reference current source needs to be changes. All the mentioned changes are shown in the table 6-8. We skip repeating the basic ideas and applied technique, because all the basic ideas and techniques are the same as before but just the values change.

#	V_2 (V)	T_2 (℃)	$Vout$ (V)	ΔI (μA)	$Offset$ (mV)
1	1 V	30	1.65	0	0
2	0.996	40	1.5	1.4	145
3	0.992	50	1.36	2.8	290
4	0.988	60	1.22	4.3	430
5	0.984	70	1.08	5.74	563
6	0.980	80	0.963	7.16	687
7	0.976	90	0.854	8.6	796
8	0.972	100	0.765	10	885

Table 6-8, Current mismatch and DC offset for I_{bias} = 50 μA

By recalling the switching current mirrors idea, and considering 3 bits for control word, and the minimum necessary injected current (I_{ref} = 1.5 μA), the new version of table 6-6 for I_{bias} = 50 μA will be shown in table 6-9.

#	V_2 (V)	T_2 (℃)	$b_2b_1b_0$	I_{cs} (μA)	$New\ Vout$ (V)	$New\ Offset$ (mV)
1	1 V	30	0 0 0	0	1.65	0
2	0.996	40	0 0 1	1.5	1.638	12
3	0.992	50	0 1 0	3	1.625	25
4	0.988	60	0 1 1	4.5	1.614	36
5	0.984	70	1 0 0	6	1.603	47
6	0.980	80	1 0 1	7.5	1.592	58
7	0.976	90	1 1 0	9	1.582	62
8	0.972	100	1 1 1	10.5	1.573	77

Table 6-9, Vout, offset values after applying the current sources technique for I_{bias} = 50 μA

In this case, the by having I_{ref} = 1.5 μA and I_{bias} = 50 μA,

$$\frac{I_{ref}}{I_{bias}} = 3\%$$

which is approximately the same percentage of the previous case.

As we can see, this proposed technique is applicable for different cases with different biasing values. Moreover, this changes is also applicable in bias voltage of the transistors as well.

6.5. Conclusion

On the basis of the literature review on measuring temperature in Integrated Circuits, it has been found that there are three main temperature measurements methods in ICs, namely: Optical, Mechanical and Electrical (Built-in temperature sensors) methods. Optical and mechanical methods require direct visual access to the silicon die or a specially prepared laboratory to perform the measurements. On the other hand, in built-in temperature sensors, neither direct visual access to the silicon die nor a laboratory environment are required.

According to if the output signal of the sensor is proportional to absolute temperature or the difference in temperature at two point of the silicon surface, temperature sensors were categorized into Absolute and Differential temperature sensors respectively.

Specifically in the thesis, we considered differential temperature sensors to explain and research the issues effecting their operation. Although the desired output voltage of differential sensors are shown as,

$$Signal_{\ out} = S_D . (T_2 - T_1) + V_{Desired}$$

we found that there are some global and local issues which cause the output signal change and have s DC offset. The resources of these issues could be either of i)process variation, ii) device mismatching, as a result of activation of the device or circuit, that is on the same silicon die and dissipate power that provokes a temperature difference between two sensing devices. iii)Bias voltage variation. As a result of the above-mentioned resources of DC offset, the undesired output signal appears as:

$$V_{\ out} = S_D . (T_2 - T_1) + V_{offset}$$

The amount of the V_{offset} is calculated using the emulation of temperature changes of one sensing device by gate voltage of it. Thus, by simulating the simple structure of differential sensor, the amount of offset in different cases is quantified. By controlling

the DC offset in differential temperature sensors, the dynamic range of the sensor can be adjusted.

In addition, some conventional offset compensation methods were introduced but they were all manual compensation methods.

The thesis proposed the new automatic technique for compensating the DC offset using a closed loop structure which checks the output of the sensor whenever it is necessary to see if the output is in the appropriate range or not. If not, the compensation loop starts working in order to control the current sources that are adding current to each branch of input differential pair in order to balance the differential pair and finally minimize the DC offset.

Experimental results show that the output DC offset was reduced into about 10% of the real one before compensation process. Some different analysis, such as changing the biasing current were also done in order to observe the applicability of the proposed technique in different cases.