Design and assemble of a DC/AC prototype power converter and a general-purpose interface board dedicated to control and/or monitoring functions.

REPORT

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# Table of contents

List of figures.............................................................................................................................................. 4
List of tables .................................................................................................................................................. 6
Abstract.......................................................................................................................................................... 7
Abbreviations ................................................................................................................................................ 8

1- Introduction ............................................................................................................................................... 9

2- Objectives ................................................................................................................................................. 11

3- Power converter: Design of an integrated 12-phase inverter ................................................................. 12

3.1- Design restrictions .................................................................................................................................. 12

3.2- Block diagram....................................................................................................................................... 12

3.2- Components selection ............................................................................................................................ 13

3.2.1- MOSFET: IRF7769L2TR1PbF ........................................................................................................... 13

3.2.2- Diode .................................................................................................................................................. 13

3.2.3- Driver: ISL2110 .................................................................................................................................. 14

3.2.4- Linear regulator: L7805ABD2T-TR .................................................................................................... 15

3.2.5- Digital temperature sensor: TMP100 ............................................................................................... 15

3.2.6- Connectors ....................................................................................................................................... 16

3.3- Simulations with LTSpice ..................................................................................................................... 17

3.4- Electrical scheme .................................................................................................................................. 20

3.5- List of selected components .................................................................................................................. 21

3.6- Thermal performance ............................................................................................................................ 21

3.7- Electrical characteristics ....................................................................................................................... 23

3.8- Layout .................................................................................................................................................... 24

3.8.1- PCB characteristics ........................................................................................................................... 24

3.8.2- Design rules ...................................................................................................................................... 24

3.8.3- Views ................................................................................................................................................. 24

3.9- Future actions ....................................................................................................................................... 25

4- ADC board: Design of a modular interface board dedicated to monitoring and control functions of the integrated 12-phase voltage source inverter (VSI) ......................................................... 26

4.1- Design restrictions .................................................................................................................................. 26

4.2- Block diagram....................................................................................................................................... 27

4.3- Analog components selection ............................................................................................................... 27

4.3.1- Voltage follower ................................................................................................................................ 27

4.3.2- Anti aliasing filter LTC1563 ............................................................................................................. 28
4.3.3-Level shifter: Voltage follower + adder .........................................................28
4.4- Analog part simulation with LTSpice ...............................................................30
4.5- Electrical scheme .............................................................................................31
4.6- List of selected components ............................................................................31
  4.6.1- Analog components .....................................................................................32
  4.6.2- Digital components .....................................................................................35
  4.6.3- Capacitors ....................................................................................................35
4.7-Thermal characteristics ......................................................................................36
4.8- Electrical characteristics ..................................................................................36
4.9- Layout ................................................................................................................36
  4.9.1- PCB characteristics ....................................................................................36
  4.9.2- Design rules .................................................................................................36
  4.9.3- Views ............................................................................................................37
4.10- Experimental results ......................................................................................38
5- Conclusions ..........................................................................................................40
6- Acknowledgments .................................................................................................41
7- Bibliography .........................................................................................................42
8- Appendices ............................................................................................................43
List of figures

Figure 1: Test bench architecture ........................................................................................................... 9
Figure 2: Box’s input channels .................................................................................................................. 10
Figure 3: Half bridge configuration ......................................................................................................... 12
Figure 4: Driver’s application .................................................................................................................. 14
Figure 5: Gate to Source Voltage versus Total Gate Source ................................................................. 14
Figure 6: Connector’s distribution and its name ..................................................................................... 17
Figure 7: Half bridge diagram. U3&U4 are the MOSFETs and U1&U2 are the diodes ...................... 18
Figure 8: \( V_G \) step response .................................................................................................................. 18
Figure 9: \( V_G \) simulation result with \( R_G = 1 \, \Omega \) ........................................................................... 19
Figure 10: \( V_G \) simulation result without \( R_G \) external resistance ...................................................... 19
Figure 11: \( I_G \) simulation result with \( R_G = 1 \, \Omega \) ......................................................................... 20
Figure 12: \( I_G \) simulation result without external gate resistance ...................................................... 20
Figure 13: \( R_{thPCBa} \) equivalent .............................................................................................................. 22
Figure 14: MOSFET power losses and thermal resistances ................................................................. 22
Figure 15: Heat sink example. ................................................................................................................. 23
Figure 16: Manufactured power converter top layer view without components. ......................... 24
Figure 17: Manufactured power converter top layer view ................................................................. 25
Figure 18: Principal diagram of the circuit. Parts 1, 2 and 3 correspond to the analog part, and 4 and 5 to the digital part .................................................................................................................. 27
Figure 19: Electric scheme of the analog part ......................................................................................... 27
Figure 20: Voltage follower .................................................................................................................... 27
Figure 21: Filter application .................................................................................................................... 28
Figure 22: Voltage follower in the level shifter .................................................................................... 27
Figure 23: Level’s shifter adder .............................................................................................................. 29
Figure 24: Offset voltage from the ADC ................................................................................................. 30
Figure 25: Analog part diagram ............................................................................................................ 30
Figure 26: Analog part simulation results ............................................................................................. 31
Figure 27: 2.5V power supply schematic ............................................................................................... 33
Figure 28: -5V/5V power supply schematic ......................................................................................... 33
Figure 29: Manufactured ADC board top layer view ........................................................................... 37
Figure 30: Manufactured ADC board bottom layer view .................................................. 37
Figure 31: Mother board top layer view ........................................................................ 38
Figure 32: ADC board on the mother board.................................................................. 38
Figure 33: Connectors location. All dimensions are in millimetres................................. 39
Figure a.1: Power converter top layer view ...................................................................... 47
Figure a.2: Power converter top silk view ....................................................................... 47
Figure a.3: Mother board top view .................................................................................. 49
Figure a.4: Mother board bottom view ........................................................................... 49
Figure a.5: ADC board top layer view ............................................................................. 53
Figure a.6: ADC board top layer silk view ...................................................................... 53
Figure a.7: ADC board bottom layer view ...................................................................... 53
Figure a.8: ADC board bottom layer silk view ................................................................. 54
Figure a.9: ADC board ground layer view ...................................................................... 54
Figure a.10: ADC board power layer view ..................................................................... 54
List of tables

Table 1: Address pins and slave addresses for the temperature sensor ..................... 16
Table 2: Thickness and thermal conductivity layers ............................................. 23
Table 3: Power converter board’s electrical characteristics ..................................... 23
Table 4: Design rules according to the manufacturer .............................................. 24
Table 5: List of the digital and analog components ............................................... 32
Table 6: Signals of the analog part connector (TFM) .............................................. 34
Table 7: Signals of the digital part connector (TFM2) .......................................... 34
Table 8: ADC board’s electrical characteristics .................................................... 36
Table 9: Layer’s names and its characteristics ....................................................... 36
Table 10: Design rules according to the manufacturer ........................................... 37
Abstract

The aim of this project is to develop the hardware for a flexible platform for testing control strategies for voltage source inverters. Using a modular approach, two boards will be designed, an inverter and a signal acquisition board. The power converter will be manufactured using IMS technology. Electrical and thermal verification of the design will be performed by simulations. Exhaustive details on the implementation will be given in this document. Experimental results will be presented.
Abbreviations

AC = Alternating Current
ADC = Analog-to-Digital Converter
CAD = Computer-Aided Design
CNV = Convert Input
DC = Direct Current
$f_c$ = Cut-off frequency
FPGA = Field Programmable Gate Array
GND = Ground
HI = High-side Input
I = Input
$^2$C = Inter-Integrated Circuit
IMS = Insulated Metal Substrate
LI = Low-side Input
MOSFET = Metal Oxide Semiconductor Field Effect Transistor
O = Output
Op-Amp = Operational Amplifier
PCB = Printed Circuit Board
PWM = Pulse-Width Modulation
PWR = Power
$R_G$ = Gate Resistance
$R_{thJC}$ = Thermal Resistance Junction-Case
$R_{thJA}$ = Thermal Resistance Junction-Ambient
SCL = Serial Clock
SCK = Clock
SDA = Serial Data Line
SDI = Serial Data Input
SDO = Serial Data Output
SMB = Server Message Block
SMD = Surface Mount Device
SPI = Serial Peripheral Interface
TTL = Transistor-Transistor Logic
VSI = Voltage Source Inverter
1- Introduction

The mechatronics department of the UTC (Université de Technologie de Compiègne) involves research and teaching activities that merge mechanical skills (vibrations and acoustic noise analyses in electric machines), power electronics (specially power electronics converters dedicated to powertrain control in electric or hybrid vehicles) and analog/digital signal processing dedicated to real-time control and monitoring (vector control applied to AC machines-induction and synchronous drivers).

The analysis of the acoustic noise and electromagnetic compatibility must be based on a realistic model of the actual converters integrated in the targeted applications in order to establish scientific results as relevant as possible to the industrial reality. At the same time, these studies might require to develop complex schemes allowing us to evaluate possible interactions between several converter/machine sets.

A general purpose power electronics platform is interesting in such a context. The project is based on the architecture presented in figure 1.

![Figure 1: Test bench architecture](image)

This platform will be based on a modular design, involving a motherboard and several standarized daughter boards. All these boards will be fitted in a customized box, excepting the power converter (12-phase VSI).

The figure 2 shows the input’s box:
This box have 6 inputs because there are 6 analog input channels. It is also possible to switch off channels independently.

Box external dimensions are:
- Width: 165 mm.
- Length: 220 mm.
- Height: 51.5 mm.

But the internal, and the usable dimensions are:
- Width: 140 mm.
- Length: 210 mm.
- Height: 50 mm.
2-Objectives

The project is focused in two objectives:

Topic 1: **Power converter**. Design of a half bridge inverter, to form an integrated 12-phase voltage source inverter (VSI). The 12-phase inverter uses a IMS board technology that dissipates a lot of thermal power.

Topic 2: **Analog to digital converter (ADC) board**. Design of an interface board dedicated to monitoring functions of the integrated 12-phase voltage source inverter (VSI).

In the corresponding section, their characteristics will be explained.

Each topic covers the full design process, from electric circuit proposal to final experimental verification of the assembled boards.
3- Power converter: Design of an integrated 12-phase inverter

3.1-Design restrictions

This design is based on a first prototype based in a half-bridge which includes:

- Two low voltage/high current power MOSFET (100V/124A): IRF7769L2TR.
- A high speed driver: Intersil ISL211x.
- Connectors used for input and output signal are SMB coaxial terminals bringing a high level of signal integrity within a small footprint.
- Temperature sensor: TMP100.
- The power converter has 2 input channels accepting PWM signals up to 50 kHz.
- Power side voltage is fixed at12V
- Maximum output intensity is fixed at 50A.
- IMS technology board.

3.2-Block diagram

The design is based in a half-bridge configuration. In figure 3 it can be seen a half-bridge:

![Half bridge configuration](image)

*Figure 3: Half bridge configuration*

There are two different parts: the logic and the power part, so there are two different supplies.
3.2-Components selection

3.2.1-MOSFET: IRF7769L2TR1PbF

MOSFET’s characteristics:
It is a DirectFET Power MOSFET with low conduction losses and L8 outline.
\( V_{DS} = 100\text{V} \)
\( I_{S} = 124\text{A} \)

MOSFET’s Gate Resistance (\( R_{G} \)):
There is a additional external Gate resistance in order to limit the driver’s output current.
In the simulation section, the MOSFET’s behaviour will be simulated in order to find this value.

3.2.2- Diode \(^1\)

It is necessary a freewheeling protection diode for the MOSFET, so it is chosen the 120LQ100, a Schottky diode with SMD package. This diode has a fast recovery time and high peak current.

The current rating for the diode must be the same rating of the MOSFET. It has the following characteristics:
\( V_{RMM} = 100\text{V} \) (Maximum Peak Repetitive Reverse Voltage)
\( I_{F} = 120\text{A} \) (Maximum Average Forward Current)
\( I_{FSM} = 1000\text{A} \) (Maximum Peak One Cycle Non-Repetitive Surge Current)

\(^1\) Currently 120LQ100 is out of stock, so it is impossible to have the component now.

We found diodes with the same ratings and SMD package but they were too large for our board.
For this reason, a temporary solution (in order to test the circuit) is to use the APT100S20B diode, which is no SMD, but has the required ratings.

There is also another solution: the 12CWQ06FNPbF diode with SMD package. This one has the following characteristics:
\( V_{RMM} = 60\text{V} \), \( I_{F} = 12\text{A} \), \( I_{FSM} = 320\text{A} \). \( I_{FSM} \) is bigger than the maximum current in the circuit. In the next section (Simulations with LTSpice) it will be checked if the diode works.

In conclusion, the board will be tested with the APT100S20B diode and then with the 12CWQ06FNPbF diode in order to check what is the best solution.
3.2.3- Driver: ISL2110

The driver is a 100V, high frequency, half bridge N-Channel power MOSFET driver. Peak output pull-up/pull-down current is 3A/4A, which allows very high switching frequency of the power MOSFETs.

The following figure illustrates the application block diagram:

![Application Block Diagram](image)

*Figure 4: Driver's application*

For the HB pin (High-side bootstrap supply), a external bootstrap capacitor is required. For the supply pin (Vdd) it is also required a decoupling capacitor.

**Bootstrap capacitor (Cbootstrap)**

Bootstrapping refers to a self-sustaining process. So, bootstrapping in electronics, is a form of positive feedback in an analog circuit design.

Figure 5 shows the MOSFET's Gate to Source Voltage (Vgs) versus the Total Gate Charge (Qg):

![Graph](image)

*Figure 5: Gate to Source Voltage versus Total Gate Source*

The aim of this graphic is to calculate the stockage energy of the MOSFET.
Stockage energy:

\[ E_{stock} = \frac{1}{2} C V_{gs}^2 = \frac{1}{2} \frac{Q_{final}}{12} 12^2 = 6 \cdot Q_{final} \]

From MOSFET’s datasheet: \( Q_{final} = 200nC = 2 \cdot 10^{-7}C \)

\[ E_{stock} = 6 \cdot 2 \cdot 10^{-7} = 1.2 \mu J \] for MOSFET’s.

With the stockage energy it is possible to find the value of the bootstrap capacitor for the driver.

The acceptable range of values of bootstrap energy is from 500 to 1000 times the stockage energy:

\[ E_{bootstrap} = 1000 \cdot E_{stock} = 1200 \mu J \]

and:

\[ E_{bootstrap} = \frac{1}{2} C_{bootstrap} V_{gs}^2 = 72 \cdot C_{bootstrap} = 1200 \mu J \Rightarrow C_{bootstrap} = 16.6 \mu F \]

Finally it is chosen: \( C_{bootstrap} = 10 \mu F \) with a \( V \geq 25V \) because it is an standard value.

That corresponds to \( E_{bootstrap} = 600 \cdot E_{stock} \). It is acceptable because it is in the chosen range of values.

Decoupling capacitors

To decrease the resistive effect of the 100\( \mu \)F polarized decoupling capacitor, it has been added two smaller capacitors in parallel of 10\( \mu \)F and 100nF (no polarized).

3.2.4- Linear regulator: L7805ABD2T-TR

It is required a linear regulator with \( V_i=12V \) and \( V_0=5V \).

The L7805ABD2T-TR is a positive and linear voltage regulator with a D2PAK package. The DC input voltage in the application is 12V, and the maximum input voltage is 35V, so this component is acceptable.

3.2.5- Digital temperature sensor: TMP100

The digital temperature sensor has a digital output with \( I^2C \) interface (2 Wire), a resolution from 9 to 12 bits, and a wide supply range from 2,7V to 5,5V.

The TMP100 require no external components for operation except for pull-up resitors on SCL and SDA bus lines.
I²C interface:

PC uses two bidirectional open-drain lines, Serial Data Line (SDA) and Serial Clock (SCL).

Because of the fact that I²C protocol uses open drain outputs, a external pull-up resistor is required for the SDA and SCL bus. The correct pull-up resistance for the I²C bus depends on the total capacitance of the bus and the frequency you want to operate the bus at. The sensor will work in a frequency lower than 100KHz, so, a typical and acceptable pull-up resistance value is:

\[ R_{\text{pull-up}} = 1.8\, \text{k}\Omega. \]

The address pins values for the configuration of the slave addresses for the TMP100 are shown in the table 1:

<table>
<thead>
<tr>
<th>ADD1</th>
<th>ADD0</th>
<th>SLAVE ADDRESS</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1001000</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1001010</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1001110</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1001111</td>
</tr>
<tr>
<td>Float</td>
<td>0</td>
<td>1001011</td>
</tr>
<tr>
<td>Float</td>
<td>1</td>
<td>1001111</td>
</tr>
</tbody>
</table>

Table 1: Address pins and slave addresses for the temperature sensor

ADD1 and ADD0 pins are hardware selectable and their values can be: 0, 1 or float. Float indicates the pin is left unconnected.

To do the 1 logic it is required a pull-up resistor to Vcc (typically 10 kΩ). To do a 0 logic, it is required to connect the pin to ground.

3.2.6- Connectors

There are three round connectors on the board. In the figure 6 it can be seen its location.
There are also six more connection pads in the PCB. A signal wire will be soldered at each pad. Every pad has its name printed on the board. Their names are: SCL, SDA, 12V, GND, HI, LI.

HI and LI are PWM input control signals from the PWM controller.

The connection pad named 12V corresponds to V+ signal in the circuit, and the connector named co1 corresponds to Vcc signal.

### 3.3-Simulations with LTSpice

The half bridge will be simulated in order to verify its behaviour.

For the simulation is necessary to calculate the half bridge load (R and L):

The desired values for intensity and output voltage are the following:

- Intensity=I=50A
- Input voltage=V_{in}=12V so, for a PWM signal of the 50%, the output voltage of the half bridge is: \( V_{RMS_{out}}=6V \)

-Resistance value:

\[ V=RI \Rightarrow 6=R\times50A \Rightarrow R=0,12\Omega \]

-Impedance value:

\[ \tau=L/R=2.10^{-3}=L/0,12 \Rightarrow L=2,4\times10^{-4}F \]

R and L are placed in series.
In the figure 7 it can be seen the half bridge diagram. The driver is substituted by two complementary PWM signals with dead-time (V1 and V2). Maximum MOSFET’s $V_{GS} = \pm 20V$, so driver output can never exceed this value.

PWM frequency=50KHz

PWM duty cycle used for the simulation= 50%

![Figure 7: Half bridge diagram. U3&U4 are the MOSFETs and U1&U2 are the diodes](image)

There is a $R_G$ (Gate Resistance), named R1 and R2 in the diagram. The MOSFET+$R_G$ behaviour is like a RC circuit, because the MOSFET gate has a capacitive behaviour.

The step response of a RC circuit is illustrated in figure 8:

![Figure 8: $V_G$ step response](image)

It is desired $V_G$ (Gate’s voltage) as squared as possible, so the time constant ($\tau$) is as small as possible.

The total gate resistance is the addition of the internal and the external gate resistance. The external resistance can be decreased, so that the maximum peak of $I_G$ is lower than
3A (maximum output current of the driver). Eventually external $R_G$ might be not necessary. So, with a external gate resistance value of $1\Omega$, the circuit will be simulated in order to verify $V_G$ and $I_G$.

$V_G$ simulation result is shown in figure 9:

\[ \text{Figure 9: } V_G \text{ simulation result with } R_G = 1 \ \Omega \]

Then, the circuit will be simulate without the external resistance:

\[ \text{Figure 10: } V_G \text{ simulation result without } R_G \text{ external resistance} \]

Without resistance the behaviour is ideal, but the value used is $1\Omega$ because this external resistance prevents undesirable high driver output currents.

Figure 11 shows $I_G$ simulation results for $1\Omega$ value of $R_G$. 
The maximum $I_G$ value is 1.82A.

Without external resistance, $I_G$ is shown in figure 12.

The maximum $I_G$ value is 2.02A.

Always $I_G$ is in the correct range ($I_G < 3A$).

In conclusion, the used value is $R_G = 1 \Omega$.

**3.4- Electrical scheme**

In the appendix A.1 there is the electrical scheme.
3.5- List of selected components

In the appendix A.2 there is a table that illustrates all the used components, with all their specifications: Name, value, characteristics, manufacturer’s name, identification manufacturer code, component unit price and total price.

3.6- Thermal performance

It is interesting to analyse the board thermal performance since it uses IMS technology. IMS corresponds to a copper circuity bonded onto an electrically insulated dielectric layer, that is bonded to a metallic substrate. This technology advantages are the lower operating temperature, improve product thermal and mechanical properties/performance, increase the power density and enable better use of surface mount technology.

The heat produced by the MOSFET power losses cause an increment of the component’s temperature. So, in this section will be sized a heat sink for the MOSFET, because it is the component with the higher power losses. The heat sink will be put in the PCB bottom to take advantage of the IMS board technology. It helps to dissipate the heat by transferring it to the surrounding air.

-MOSFET’s characteristics:

- Max. thermal resistance junction-to-ambient: $R_{\text{JA}}=45^\circ \text{C/W}$ (Surface mounted on 1 in square Cu board, steady state).
- Max. thermal resistance Junction-to PCB mounted: $R_{\text{J-PCB}}=0.5^\circ \text{C/W}$
- Max. thermal resistance Junction-to can: $R_{\text{J-Can}}=1.2^\circ \text{C/W}$
- Storage Temperature Rang from -55 to 175 ºC.

It is considered an ambient temperature ($T_A$) of 25ºC, and a MOSFET’s working temperature ($T_J$) of 100ºC.

The MOSFET’s total thermal resistance is calculated with the following expression:

$$P = \frac{\Delta T}{R_T} = \frac{T_J - T_A}{R_T} = \frac{100-25}{R_T} \ [\text{W}] \ \Rightarrow \ R_T = \frac{100-25}{P} \ [^\circ \text{C/W}]$$

In order to find the total thermal resistance, previously it has to be calculated the MOSFET’s power (P). Power losses will be deduced with the following expression using the model introduced in the section 3.3:

$$P_{\text{avg}} = \text{average}((V_D - V_S) \cdot I_D) = 7,368 \ \text{W}$$

The maximum power dissipation corresponds to a PWM’s duty cycle of 50%, because there are two MOSFETS, and one is the complementary of the other.
The heat sink will be sized for one MOSFET and the board will have a heat sink for every MOSFET.

So, the total thermal resistance is: \[ R_T = \frac{100-25}{p} = 10,179 \, ^\circ\text{C}/\text{W} \]

Figure 13 shows \( R_{th\text{PCB}_a} \). It is the equivalent thermal resistance across the IMS board to air, using a heat sink attached to the metal layer of the board:

\[ \text{Figure 13: } R_{th\text{PCB}_a} \text{ equivalent} \]

So, the equivalent thermal resistance can be split in the following terms:

\[ R_{th\text{PCB}_a} = R_{th\text{copper-dielectric}} + R_{th\text{dielectric-aluminium}} + R_{th\text{aluminium-heat sink}} + R_{th\text{ heat sink-air}} \quad (1) \]

The following diagram illustrates the total thermal resistance’s layout:

\[ \text{Figure 14: MOSFET power losses and thermal resistances} \]

\[ R_T = \frac{R_{th\text{ja}} (R_{th\text{PCB}_a} + R_{th\text{PCB}_a})}{R_{th\text{ja}} + R_{th\text{PCB}_a} + R_{th\text{PCB}_a}} = \frac{45 (0.5 + R_{th\text{PCB}_a})}{45 + 0.5 + R_{th\text{PCB}_a}} = 10,179 \, ^\circ\text{C}/\text{W} \]

So, \( R_{th\text{PCB}_a} \) value is:

\[ R_{th\text{PCB}_a} = 12,678 \, ^\circ\text{C}/\text{W} \]

The thermal resistances associated to the IMS board are calculated with the following expression:

\[ R = \frac{d}{A \cdot \lambda} \quad (2) \]
d=thickness layer
A=contact area
λ= thermal conductivity

Contact area is 1.2 times the MOSFET’s area, so:
MOSFET area= 63.472 mm² and A=1.2*MOSFET area= 76.17mm²

The other parameters are shown in table 2:

<table>
<thead>
<tr>
<th>Layer</th>
<th>Thickness (d)</th>
<th>Thermal conductivity(λ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Copper</td>
<td>35 µm</td>
<td>390 W/m*K</td>
</tr>
<tr>
<td>Dielectric FR4</td>
<td>75 µm</td>
<td>0.25 W/m*K</td>
</tr>
<tr>
<td>Aluminium</td>
<td>1.5 mm</td>
<td>237 W/m*K</td>
</tr>
</tbody>
</table>

Table 2: Thickness and thermal conductivity layers.

Resistances calculated with expression (2) are the following:

\[R_{\text{thcopper-dielectric}} = 0.001^\circ\text{C/W}\]
\[R_{\text{thdielectric-aluminium}} = 3.938^\circ\text{C/W}\]
\[R_{\text{thaluminium-heat sink}} = 0.083^\circ\text{C/W}\]

In order to size a heat sink it is necessary the thermal resistance value from heat sink to air (R_{th heat sink-air}). So, according to equation (1) the value is:

\[R_{\text{th heat sink-air}} = 8.655^\circ\text{C/W}\]

According to this thermal resistance value it will be selected a proper heat sink.

Figure 15 shows a heat sink example.

3.7- Electrical characteristics

The electrical characteristics of the power converter are in table 3:

<table>
<thead>
<tr>
<th>Input’s characteristics</th>
<th>Output’s characteristics</th>
</tr>
</thead>
<tbody>
<tr>
<td>PWM signal</td>
<td>Maximum delivered power: 600W</td>
</tr>
<tr>
<td>Maximum frequency: 50KHz</td>
<td>Maximum power side voltage: 12V</td>
</tr>
<tr>
<td>Maximum logic side supply: 12V</td>
<td></td>
</tr>
</tbody>
</table>

Table 3: Power converter board’s electrical characteristics
3.8- Layout

3.8.1- PCB characteristics

PCB size: **43.03 x 73.83mm**

Number of layers: 1 (top)

There is a ground plane on the top layer that improves the noise immunity of the board. There are routing constraints in this board because only a single layer is available due to IMS (Insulated Metal Substrate) board technology. The layer is attached to a metallic cooling surface, thus all components must have SMD packaging and be placed on top layer.

3.8.2- Design rules

According to the design rules of the manufacturer (Eurocircuits), the following design parameters have been chosen:

<table>
<thead>
<tr>
<th>Top layer</th>
<th>Trace width</th>
<th>0.7 mm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Trace clearance</td>
<td>0.7 mm</td>
<td></td>
</tr>
<tr>
<td>Copper to board outline</td>
<td>1 mm</td>
<td></td>
</tr>
</tbody>
</table>

Table 4: Design rules according to the manufacturer

For the rated current of the board, the power trace's widths are wider (1mm wide) than the signal traces to prevent overtemperature.

The designed PCB has the following service: I (IMS pool).

3.8.3- Views

In appendix A.3 there are the layout views.

The top view of the manufactured PCB without the components is shown in figure 16:

*Figure 16: Manufactured power converter top layer view without components.*
The top view of the manufactured PCB with all components is shown in figure 17:

![Manufactured power converter top layer view](image)

**Figure 17: Manufactured power converter top layer view**

### 3.9- Future actions

This board will be checked. So obtain this it will be supplied with 12V. Two complementary PWM signals of 50 kHz will be applied and a external variable load will be connected. The output voltage will be observed.
4- ADC board: Design of a modular interface board dedicated to monitoring and control functions of the integrated 12-phase voltage source inverter (VSI).

4.1- Design restrictions

Since sampling frequency requirements are not the same for each kind of measurement, a generic solution should be investigated (including a parameterized anti-aliasing filter) with a unified SPI or I2C digital bus.

In order to adapt this board to as many applications as possible, it should be as small as possible and include only one analog channel. Among all the required features, the main ones are (for one daughter board):

- One analog channel.
- Adaptability to +/-10V voltage range using jumpers.
- Anti-aliasing filter based on active circuits (integrated circuit such as Linear Technology LTC1563) usable over a wide frequency range (from 10Hz to 500 kHz).
- Resolution: 14 bits.
- Maximum sampling frequency: 2MS/s (Analog Devices AD7944).
- Full stand-alone operation capabilities.

High-speed logic insulators are also required for a safe control of power converters. Key features of such insulators are (for one daughter board):

- Time delays lower than 20ns.
- Insulation equal to (or higher than) 1kV.
- Insulation circuits, embedded DC/DC converters and PCB tracks clearance should guarantee insulation.
- At least 16 I/O terminals are required.
- Data direction should be configurable by jumpers if possible.
- Logic voltages should be programmable by jumpers (at least TTL 5V, 3.3V are required).
4.2- Block diagram

![Block diagram](image)

*Figure 18: Principal diagram of the circuit. Parts 1, 2 and 3 correspond to the analog part, and 4 and 5 to the digital part.*

4.3- Analog components selection

Figure 19 shows the electric scheme of the analog part:

![Electric scheme](image)

*Figure 19: Electric scheme of the analog part*

4.3.1- Voltage follower

![Voltage follower](image)

*Figure 20: Voltage follower*

-10V < \(V_i\) < 10V
-5V < \(V_o\) < 5V

\[
V_o = \frac{R_2}{R_1 + R_2} \cdot V_i
\]

If \(R_1 = R_2:\)
\[ V_o = \frac{R_2}{R_1 + R_2} \cdot V_i = 0,5 \cdot V_i \ \Rightarrow \ A = \frac{V_o}{V_i} = 0,5 \]

A= gain

\[ R_1=R_2=100K\Omega \]

**4.3.2-Antialiasing filter LTC1563** (analog low-pass filter)

- \(-5V < V_i < 5V\)
- \(-5V < V_o < 5V\)

From filter datasheet:

\[ f_c = 256KHz \cdot \left( \frac{10K\Omega}{R_3} \right) \]

\( f_c \) = cutting frequency

Maximum \( f_c \) that the filter works is 256KHz. \( \Rightarrow f_c = 256KHz \)

\[ f_c = 256KHz \cdot \left( \frac{10K\Omega}{R_3} \right) = 256KHz \ \Rightarrow \ R = 10K\Omega \]

**4.3.3-Level shifter: Voltage follower + adder**

**4.3.3.1-Voltage follower**

\[ f_c = 256KHz \cdot \left( \frac{10K\Omega}{R_3} \right) = 256KHz \ \Rightarrow \ R = 10K\Omega \]
\[-5V < V_i < 5V\]
\[-V_{ref}/2 < V_o < V_{ref}/2, \quad V_{ref}= 4.096\text{V}\]

\[
\frac{V_o}{V_i} = \frac{2.048}{5} = \frac{R_2}{R_1+R_2}
\]

If \(R_1=100\text{K}\Omega \Rightarrow R_2=69.37\text{K}\Omega \)

\(R_1=100\text{K}\Omega \)

\(R_2=69.37\text{K}\Omega \)

For \(R_2\): They have to be 2 resistances in series because it does not exist a resistance of 69.37KΩ.

\(R_2=R+R'\)

With a 0.1% tolerance and 0805 SMD package:

\(R=68.1\text{K}\Omega\)

\(R'=1.27\text{K}\Omega\)

\(R_2=R+R'=68.1\text{K}\Omega+1.27\text{K}\Omega\)

4.3.3.2-Adder

\[\text{Figure 23: Level’s shifter adder}\]

\[
V_{\text{offset follower}}=V_{\text{adder}} \Rightarrow V_o=V_i'
\]

\[-V_{\text{ref}}/2 < V_i' < V_{\text{ref}}/2, \quad V_{\text{ref}}= 4.096\text{V}\]

\[0 < V_o' < V_{\text{ref}} \quad , \quad V_o'=V_{\text{ADC}}\]

\[
V^+ = \frac{V_i'+V_{\text{off}}}{R_1+R_2} = \frac{R_2(V_i'+R_1-V_{\text{off}})}{R_1+R_2}
\]

\[
V^- = \frac{V_o'}{R_1+R_2} = \frac{V_o'R_1}{R_1+R_2}
\]

\[
V^+ = V^- \Rightarrow \frac{R_2(V_i'+R_1-V_{\text{off}})}{R_1+R_2} = \frac{V_o'R_1}{R_1+R_2} \Rightarrow V_o' = \frac{R_2(V_i'+R_1-V_{\text{off}})}{R_1} = \frac{R_2}{R_1} \cdot V_i' + V_{\text{off}}
\]

If \(R_1=R_2\) \Rightarrow \(V_o'=V_i'+V_{\text{off}}\)

\(R_1=R_2=100\text{K}\Omega\)
In figure 24 it will be shown how to create $V_{\text{offset}}$ from $V_{\text{ref}}$.

![Figure 24: Offset voltage from the ADC](image)

$V_{\text{ref}}$ comes from ADC pin 1 (REF1).

$V_{\text{ref}} = 4.096V$

$V_{\text{offset}} = \frac{V_{\text{ref}} \cdot R_2}{R_1 + R_2}$

If $R_1 = R_2 = 100K\Omega$

$V_{\text{offset}} = 0.5 \cdot V_{\text{ref}} = 0.5 \cdot 4.096 = 2.048V$

$C = 100nF$

### 4.4- Analog part simulation with LTSpice

An analog part simulation has been done observing the inputs and outputs of the different subcircuits.

In the figure 25 it can be seen the analog part diagram.

![Figure 25: Analog part diagram](image)

The inputs and the outputs voltages of each subcircuit shown in figure 25 are shown in figure 26.
Figure 26: Analog part simulation results

$V_1$, the red curve named $V(n015)$, in figure 26, is the input signal of the board. (-10V < $V_1$ < 10V).

The output ($V_2$) (the blue curve) is reduced by half by the voltage divider. (-5V < $V_2$ < 5V).

Since the frequency of the input signal is 1kHz, the low pass filter is only used as an antialiasing filter with a cut-off frequency of 256 kHz. In $V_3$ (the light green curve overlapping $V_2$) it is checked that the output voltage is still reduced at the half. (-5V < $V_3$ < 5V).

Next is the voltage follower. With the voltage divisor it is obtained an output voltage named $V_3^*$ (the green curve): $-V_{ref}/2 < V_3^* < V_{ref}/2$ (-2,048V < $V_3^*$ < 2,048V). Then it is passed through the voltage adder to shift the output voltage: $0V < V_4 < 4.096V$

$V_4$ (the pink curve) is the output voltage and also the ADC’s input voltage.

4.5- Electrical scheme

In the appendix B.1 there is the electrical scheme.

There is the analog and digital part, and the power supply.

4.6- List of selected components

In the appendix B.2 there is a table that illustrates all the used components, with all their specifications: Name, value, characteristics, manufacturer’s name, identification manufacturer code, component unit price and total price.
This section explains the main characteristics of the components and also why they have been chosen.

Before that, table 5 lists the analog part and the digital part components:

<table>
<thead>
<tr>
<th>Top layer (digital)</th>
<th>Description</th>
<th>Bottom layer (analog)</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>AD7944</td>
<td>Analog to digital converter</td>
<td>LMV721</td>
<td>Operational amplifier</td>
</tr>
<tr>
<td>SN74LVC8T245DGVR</td>
<td>Voltage converter buffer</td>
<td>LTC1563</td>
<td>Filter</td>
</tr>
<tr>
<td>ISO7241ADW</td>
<td>Isolated buffer</td>
<td>LT1118CST-2.5</td>
<td>Voltage regulator</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DCR010505U</td>
<td>Isolated DC/DC converter</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Connectors</td>
<td></td>
</tr>
</tbody>
</table>

### 4.6.1- Analog components

- **Filter: LTC1563-2**
  
  Active RC, 4th order low pass filter family with rail-to-rail inputs and outputs and low DC offset suitable for systems with a resolution of up to 16 bits. It has a single resistor value that gives a unity-gain Butterworth response.
  
  - Cut-off frequency (fc): 256Hz < fc < 256KHz
  - Power dissipation= 500 mW

- **Op-Amp: LMV721**
  
  It is a 10MHz low-noise low-voltage and low-power operational amplifier.
  
  - Rail-to-rail output swing.
  - Power supply voltage: 2.2V to 5.5V.
  - High unity-Gain Bandwidth: 10 MHz.

- **Power supply**
  
  It is required to have a supply of: 2.5V, 5V, -5V and 3.3V.
  
  3.3V comes from FPGA.
  
  The others come from LT1118CST-2.5 and DCR010505U components.
**LT1118CST-2.5**

It is a low dropout regulator that regulates the output voltage. It regulates while sourcing or sinking current.

- \( V_{\text{in}} = 5V \)
- \( V_{\text{out}} = 2.5V \)

Figure 27 shows the power supply schematic.

![2.5V power supply schematic](image)

*Figure 27: 2.5V power supply schematic*

**DCR010505U**

DC/DC regulated and isolated converted to supply the buffers.

- 1W
- Regulated
- Isolated
- Input voltage = 5V
- Output voltage = 5V

In the figure 28 it can be seen the power supply schematic.

![+/-5V power supply schematic](image)

*Figure 28: ±5V/5V power supply schematic*
Connectors

**Analog port connection**

The analog port connection is a 10 pins 2x5 dual row.

Next table shows the signals of the analog part connector named TFM.

<table>
<thead>
<tr>
<th>Signal</th>
<th>Description</th>
<th>I/O</th>
<th>Pin</th>
</tr>
</thead>
<tbody>
<tr>
<td>+5V</td>
<td>Power supply</td>
<td>PWR</td>
<td>1</td>
</tr>
<tr>
<td>-5V</td>
<td>Power supply</td>
<td>PWR</td>
<td>2</td>
</tr>
<tr>
<td>GND</td>
<td>Ground</td>
<td>PWR</td>
<td>3</td>
</tr>
<tr>
<td>IN</td>
<td>Input voltage of the circuit</td>
<td>I</td>
<td>4</td>
</tr>
<tr>
<td>GND</td>
<td>Ground</td>
<td>PWR</td>
<td>5</td>
</tr>
<tr>
<td></td>
<td>No signal</td>
<td></td>
<td>6</td>
</tr>
<tr>
<td></td>
<td>Connected to pin 7</td>
<td></td>
<td></td>
</tr>
<tr>
<td>GND</td>
<td>Ground</td>
<td>PWR</td>
<td>8</td>
</tr>
<tr>
<td>GND</td>
<td>Ground</td>
<td>PWR</td>
<td>9</td>
</tr>
<tr>
<td>GND</td>
<td>Ground</td>
<td>PWR</td>
<td>10</td>
</tr>
</tbody>
</table>

Table 6: Signals of the analog part connector (TFM)

**Digital port connection**

The digital port connection is a 10 pins 2x5 dual row.

Table 7 shows the signals of the digital part connector (TMF2 connector):

<table>
<thead>
<tr>
<th>Signal</th>
<th>Description</th>
<th>I/O</th>
<th>Pin</th>
</tr>
</thead>
<tbody>
<tr>
<td>ISO_5V</td>
<td>Isolated power supply</td>
<td>PWR</td>
<td>1</td>
</tr>
<tr>
<td>3.3V</td>
<td>Power supply from FPGA</td>
<td>PWR</td>
<td>2</td>
</tr>
<tr>
<td>GNDearth</td>
<td>Isolated ground</td>
<td>PWR</td>
<td>3</td>
</tr>
<tr>
<td>OUT_D</td>
<td>ADC data bit (SDO)</td>
<td>O</td>
<td>4</td>
</tr>
<tr>
<td>GNDearth</td>
<td>Isolated ground</td>
<td>PWR</td>
<td>5</td>
</tr>
<tr>
<td>IN_C</td>
<td>ADC data bit (CNV)</td>
<td>I</td>
<td>6</td>
</tr>
<tr>
<td>GNDearth</td>
<td>Isolated ground</td>
<td>PWR</td>
<td>7</td>
</tr>
<tr>
<td>IN_B</td>
<td>ADC data bit (SDI)</td>
<td>I</td>
<td>8</td>
</tr>
<tr>
<td>GNDearth</td>
<td>Isolated ground</td>
<td>PWR</td>
<td>9</td>
</tr>
<tr>
<td>IN_A</td>
<td>ADC data bit (SCK)</td>
<td>I</td>
<td>10</td>
</tr>
</tbody>
</table>

Table 7: Signals of the digital part connector (TFM2)
4.6.2- Digital components

-ADC: AD7944
  - 14 bit resolution
  - 2.0 MSPs (normal mode)
  - Low power dissipation
  - $0V < V_{in} < V_{ref}$

ADC only works in internal reference mode. Internal reference: $V_{ref} = 4'096V$

Resolution: $\Delta V_{dc} = \frac{4.096V}{2^{14}} = \frac{1mV}{4} = 0.25mV$

Power supplies: 
- $AVDD= 2'5V$
- $DVDD= 2'5V$
- $BVDD= 5V$
- $VIO= 2'5V$

-SN74LVC8T245DGVR

Voltage converter buffer. 8 bit dual-supply bus transceiver with configurable voltage translation and 3 state outputs. Only it is used 4 bits (4 inputs and 4 outputs).
  - $V_{in}= 2.5V$
  - $V_{out}= 5V$

-Isolated buffer: ISO7241ADW

It is necessary to isolate de output of the ADC of the rest of the circuit. ISO7241 it is a high speed digital isolator.
  - 1 input
  - 3 outputs
  - Input voltage= 3.3V
  - Output voltage= 5V

4.6.3- Capacitors

Each integrated chip has its own decoupling capacitor at the feeding terminals.

The 5V and -5V supplies have a decoupling capacitor of 100nF.

The 2.5V and the 3.3V supplies have two decoupling capacitors in parallel of decreasing value. We do this because the smaller the value, the lesser the resistive behavior.

The first one is non polarized, a ceramic capacitor. Its value is 10nF.
The second one is polarized, a tantalum capacitor. Its value is \(100\text{nF}\).

4.7- Thermal characteristics

It is not necessary to analyse the ADC board’s thermal characteristics, because any of the integrated chips have important power losses.

The ADC is the component with more losses, but it never will work at the maximum frequency allowed.

4.8- Electrical characteristics

The electrical characteristics of the ADC are summarized in the following table:

<table>
<thead>
<tr>
<th>Input characteristics</th>
<th>Value</th>
<th>Output characteristics</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum frequency</td>
<td>256KHz</td>
<td>Resolution</td>
<td>14 bits</td>
</tr>
<tr>
<td>Input voltage</td>
<td>+10V/-10V</td>
<td>4 wire, SPI protocol</td>
<td></td>
</tr>
<tr>
<td>Voltage supply</td>
<td>5V</td>
<td>Clock frequency</td>
<td>50MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Output voltage</td>
<td>5V</td>
</tr>
</tbody>
</table>

Table 8: ADC board’s electrical characteristics

4.9- Layout

The objective is to make the interface board as small as possible, for this reason all the components are SMD (Surface Mount Device).

4.9.1- PCB characteristics

PCB size: \(26.03 \times 85.09\ \text{mm}\)

Number of layers: 4

<table>
<thead>
<tr>
<th>Layer’s name</th>
<th>Characteristics</th>
</tr>
</thead>
<tbody>
<tr>
<td>Top</td>
<td>Digital part of the circuit</td>
</tr>
<tr>
<td>Bottom</td>
<td>Analog part of the circuit, isolated 0V voltage layer</td>
</tr>
<tr>
<td>GND</td>
<td>0V voltage layer</td>
</tr>
<tr>
<td>PWR</td>
<td>3 power voltages: 5V, -5V and 3.3V</td>
</tr>
</tbody>
</table>

Table 9: Layer’s names and its characteristics

4.9.2- Design rules

According to the design rules of the manufacturer (Eurocircuits), the following design parameters have been chosen:
In order to find via’s diameter:

The designed PCB has the following services: P (PCB proto), T (TECH pool) and S (STANDARD pool), that is class A, B or C for the drill class and class 3, 4, 5 or 6 for the pattern class.

For the drill class it is chosen the C class → minimum NPTH=0,30 and minimum PHD=0,35 = via hole diameter.

For the pattern class it is chosen class 6 → OAR = 0,125 (ring)

So: 0,125*2+0,35=0,25+0,35=0,6 = via outer diameter.

4.9.3- Views

In appendix B.3 there are the layout views.

The manufactured PCB is the following:

- Top view:

![Figure 29: Manufactured ADC board top layer view](image)

- Bottom view:

![Figure 30: Manufactured ADC board bottom layer view](image)
4.10- Experimental results

In order to check the board, a mother board will be used. The mother board function is to supply the ADC board with the correct voltage levels (+5V (isolated) and 3.3V). The following ADC signals are also available for external treatment: CNV, SDI, SCK, SDO, +5V, -5V and the input signal of the board.

Figure 31 shows this mother board:

![Figure 31: Mother board top layer view](image)

Connectors

In appendix A.4 there is the mother board electrical scheme and all layout views. ADC board will be connected on the two black connectors. Figure 32 shows the result:

![Figure 32: ADC board on the mother board.](image)

In the figure 33 it can be seen the location between the two black connectors and the boards:
- In order to check the ADC board, firstly the mother board is supplied with 12V (red connector in figure 32), and the board converts it to 5V and 3.3V with the correspondent voltage regulator in order to feed the ADC board. The mother board red LED is light up when ADC board is supplied with the 5V and 3.3V.

- Next, with a tester it is checked the output voltage of the three regulators of the board. All is correct.

- Then the analog part will be checked. In order to do this, figure 26 voltages will be checked with an oscilloscope.

- In order to check the digital part, the communication signals from the ADC board (CNV, SDI, SCK, SDO) will be connected to the computer. A Bus Pirate\(^2\) will be used to verify the ADC chip. Bus Pirate is a universal bus interface that talks to most chips from a PC serial terminal, eliminating a ton of early prototyping effort when working with new or unknown chips. Using a Bus Pirate, developers can use a serial terminal to interface with devices over a variety of hardware protocols, such as SPI and I\(^2\)C.

---

\(^2\) Bus Pirate web site: http://dangerousprototypes.com/bus-pirate-manual/
5-Conclusions

In this project it has been designed and built two electronic boards. First, a power converter has been done and secondly, a data acquisition board. The same steps have been followed to develop the two boards. Now, they will be explained:

First, the block’s diagram has been designed according to the given design restrictions. Then the blocks have been implemented with the actual electric circuit. The following task was to select all components, and then the correct electrical performances of the components have been verified with simulations.

Next, the board’s thermal characteristics have been checked. With the simulations, the maximum power dissipation of the critical components has been calculated in order to decide if a heat sink must be added.

Later, with CAD software, the board’s layout has been done. Once the board has been built by the manufacturer, all components were soldered. To finish, it is verified that the performance of the boards is the expected from the simulations. For the ADC board this has been possible with the mother board, because its function is to supply it.

The power converter has an inverter topology. The end user might use it as an inverter or like a DC/DC converter, depending on the supply connections. The principal characteristic of the designs is that all boards are very small, essential condition to fit them in the box.

In the future, 12 identical converter boards will be built in order to have the 12-phase inverter, and 6 identical data acquisition boards will be built in order to have the 6 input channels of the box.
6-Acknowledgments

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I would also like to thanks Jordi for his help and patience with me.
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  - DigiKey: www.digikey.com
  - Farnell: http://fr.farnell.com/
  - Mouser: www.mouser.com
  - RS (RadioSpare): http://radiospares-fr.rs-online.com/web/
-Manufacturer’s web sites:
  - Analog Devices: www.analog.com
  - International Rectifier: http://www.irf.com/
  - Linear Technology : www.linear.com
  - National Instruments: www.ni.com
  - Samtec : www.samtec.com
  - Texas Instruments: www.ti.com
8-Appendices

Appendix A: Power converter.
  Appendix A.1 Power converter’s electrical scheme.
  Appendix A.2 Power converter’s table with all used components and all their specifications.
  Appendix A.3 Power converter’s layout views.
  Appendix A.4 Mother board electrical scheme and layout views.

Appendix B: ADC board.
  Appendix B.1 ADC board’s electrical scheme.
  Appendix B.2 ADC board’s table with all used components and all their specifications.
  Appendix B.3 ADC board’s layout views.

Appendix C: Component’s datasheets.

  Power converter
  1-MOSFET IRF7769L2TR1PbF
  2-Diode 120LQ100
  3- Diode APT100S20B
  4-Diode 12CWQ06FNPbF
  5-Driver ISL2110
  6-Linear regulator: L1805ABD2T-TR
  7-Digital temperature sensor TMP100

  ADC board
  8-Analog to digital converter AD7944
  9-Voltage converter buffer SN74LVC8T245DGVR
  10- Isolated buffer ISO7241
  11-Operational amplifier LMV721
  12-Filter LTC1563
  13-Voltage regulator LT1118CST-2.5
  14- Isolated DC/DC converter DCR010505U
  15-Header connector TFM-105-02-S-D-WT
  16-Socket connector SFM-105-02-S-D
Appendix A

Power converter.

*Appendix A.1*

Power converter’s electrical scheme.

*Appendix A.2*

Power converter’s table with all used components and all their specifications.

*Appendix A.3*

Power converter’s layout views.

*Appendix A.4*

Mother board electrical scheme and layout views.
### Appendix A.2

<table>
<thead>
<tr>
<th>Name</th>
<th>Quantity</th>
<th>Value</th>
<th>Identification name</th>
<th>Manufacturer</th>
<th>Code</th>
<th>Unit price (€)</th>
<th>Total price (€)</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mosfet</td>
<td>10</td>
<td>100V/124A</td>
<td>IRF7769L2TR1PBF</td>
<td>FARNELL</td>
<td>1791558</td>
<td>6.24</td>
<td>62.4</td>
<td>Direct Fet</td>
</tr>
<tr>
<td>R</td>
<td>10</td>
<td>1Ω</td>
<td>LR1206-1R0FI</td>
<td>FARNELL</td>
<td>1100340</td>
<td>0.61</td>
<td>6.1</td>
<td>1206</td>
</tr>
<tr>
<td>Driver</td>
<td>5</td>
<td>-</td>
<td>ISL2110</td>
<td>Avnet</td>
<td>ISL2110ABZ-T</td>
<td>2.165</td>
<td>10.825</td>
<td>8 SOIC</td>
</tr>
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<td>C</td>
<td>10</td>
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<td>12103C106K4Z2A</td>
<td>FARNELL</td>
<td>1833857RL</td>
<td>1.8</td>
<td>18</td>
<td>1210</td>
</tr>
<tr>
<td>C</td>
<td>5</td>
<td>47µF</td>
<td>T491D476K025AT</td>
<td>FARNELL</td>
<td>1457517</td>
<td>1.37</td>
<td>6.85</td>
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**TOTAL:** 153.87€
Appendix A.3

Power converter’s layout views.

-Top view:

Figure a.1 shows the top layer routing.

![Figure a.1: Power converter top layer view](image)

The following figure illustrates the top layer silk view in order to watch all components and their distribution.

![Figure a.2: Power converter top silk view](image)
Appendix A.4

Mother board electrical scheme and layout views.
-Top view:
Figure a.3 shows the top layer routing.

-Bottom view:
Figure a.4 shows the bottom layer routing.
Appendix B

ADC board.

Appendix B.1
ADC board’s electrical scheme.

Appendix B.2
ADC board’s table with all used components and all their specifications.

Appendix B.3
ADC board’s layout views.
## Appendix B.2

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**TOTAL:** 358.95€
Appendix B.3

ADC board’s layout views.

-Top view:

![ADC board top layer view](image)

*Figure a.5: ADC board top layer view*

Figure a.6 shows the top layer silk view in order to watch the components and their distribution:

![ADC board top layer silk view](image)

*Figure a.6: ADC board top layer silk view*

-Bottom view:

![ADC board bottom layer view](image)

*Figure a.7: ADC board bottom layer view*
Figure a.8: ADC board bottom layer silk view

-Ground view:

Figure a.9: ADC board ground layer view

-Power view:

Figure a.10: ADC board power layer view
Appendix C

Component’s datasheets.

Power converter
1-MOSFET IRF7769L2TR1PbF
2-Diode 120LQ100
3-Diode APT100S20B
4-Diode 12CWQ06FNPbF
5-Driver ISL2110
6-Linear regulator: L1805ABD2T-TR
7-Digital temperature sensor TMP100

ADC board
8-Analog to digital converter AD7944
9-Voltage converter buffer SN74LVC8T245DGVR
10-Isolated buffer ISO7241
11-Operational amplifier LMV721
12-Filter LTC1563
13-Voltage regulator LT1118CST-2.5
14-Isolated DC/DC converter DCR010505U
15-Header connector TFM-105-02-S-D-WT
16-Socket connector SFM-105-02-S-D