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Systematic and random variability analysis of two different 6T-SRAM layout topologies

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ABSTRACT

This paper studies the device variability influence on 6T-SRAM cells in a function of the regularity level of their layout. Systematic and random variations have been analyzed when these memory circuits are implemented on a 45 nm technology node. The NBTI aging relevance on these cells has been also studied for two layout topologies and SNM has been seen as the parameter that suffers the highest impact with respect to cell aging and variability.

1. Introduction

The device performance of consumption circuits is improved by shrinking their dimensions and by obtaining faster, smaller and lower power circuits. However, as a side effect of this scaling down, small differences in devices and imperfections, due to the manufacturing process, become increasingly important. In this sense, variability has been stated as a hot topic for electronics reliability researchers [1], such as when the technology node is reduced. Variability sources are usually classified in two groups, systematic and random [2]. The first group cause deterministic shifts in device parameters, related to different manufacturing process conditions or critical process limitations [3]. For instance, one type of systematic variation is related to the difficulty of printing lines narrower than the wavelength of the light that it is used to print them [4]. The second group, random variation, relates to atomistic effects which become relevant due to the aggressive geometrical scaling down of devices. Both effects may affect a design at any time in an unpredictable manner. Random Dopant Fluctuation (RDF) is usually assumed to be the main variability source [1,3,5]. Although systematic variations can be mitigated through the employment of process control or special design techniques, i.e. layout regularity and lithography improvements [4,6], random variations cannot be minimized due to their nature, and thus have to be tolerated and expected.

In this context, process variations are of particular concern in memories, since these are typically designed using minimum feature sizes for density reasons. In this work, the six transistor SRAM (6T-SRAM) cell is used as reference. The cell robustness is usually determined by the Static Noise Margin (SNM), which is the minimum DC noise voltage necessary to flip the state of the SRAM cells [4,5,7]. We have assumed SNM as a reference parameter throughout the study, although other usual cell metrics are the Read Noise Margin (RNM), access times (write and read) and power consumption of the static cell [8]. Note that device variations have a large impact on 6T-SRAM cell performance, since this requires high stability [5]. In this sense, the process variations are usually related to a threshold voltage (V_T) shift, whose standard deviation is a function of the device area [9]. Additionally, the device degradation is another relevant factor to consider in a reliability analysis of a SRAM cell [10]. The aging consequence is commonly reflected in a SNM reduction and, as a consequence, worse cell behavior stability is observed, i.e. larger timing delay and higher power consumption [11]. Bias Temperature Instability (BTI) is usually considered to be the main cause of aging in a 6T cell [7,9,10] and its main impact is a V_T-shift of cell devices. In these contexts, the Negative BTI (NBTI) damage which only affects the pMOSFETs has always been stated as one of the major reliability issues to be considered [8,11] when analyzing the behavior of a 6T-SRAM cell.

This paper analyses the influence of systematic and random variability, on two different layout topologies, by studying the relevance of a more regular pattern on 6T-SRAM cell performance. Few studies have compared both kinds of variability, and even fewer have developed their own cell layouts focusing on these variable conditions. As such, the paper is organized as follows; Section II shows how the layouts have been designed and the

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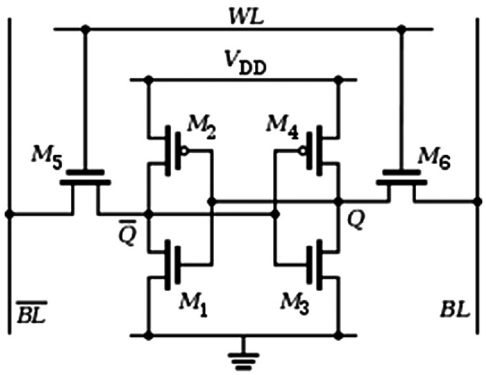

Fig. 1. 6T-SRAM cell design.

influence of systematic variability is analyzed. In Section III the importance of random process fluctuation on both layouts is illustrated. Section IV depicts the influence of aging in SRAM cells, and our conclusions are outlined in Section V.

2. Study of systematic variations

2.1. A. Design of the implemented layouts

Fig. 1 depicts the traditional schematic layout of a 6T-SRAM cell. Two topologies with different degrees of layout regularity have been implemented, seeking to analyze the influence of both kinds of variability (systematic and random). A regular layout is defined as when only straight rectangle shapes are contemplated, with all the shapes in a given layer running in one direction (i.e. 1-D or gridded design) and with all layers equally spaced [6]. Therefore, Ishida's topology (type 4) [12] has been considered, since it is today's industry standard SRAM bit-cell layout. This has been compared with a Mann 6T cell (type 5) [13] proposal, which is a new layout configuration presented as a competitive alternative topology, able to be scaled to 22 nm and beyond, with a relevant complexity reduction and a more regular style.

In order to implement this we have used an open-source 45 nm technology Process Design Kit (PDK) provided by North Carolina State University (NCSU), FreePDK45 1.4 [14]. Both layouts have been proposed in compliance with the Design Rules provided by FreePDK45. It is worth pointing out that our topologies have not implemented local interconnect [15] as this kit does not provide it and which would help to achieve a smaller cell area. We measured both layouts using the smallest dimensions for this technology. Thus our device sizes have been drawn with $W=90$ nm and $L=50$ nm assigned to both pull-up (pMOS) and access transistors (nMOS), and $W=140$ nm and $L=50$ nm for the pull-down (nMOS). We have stated the same ratio between pull-down and pull-up transistors used in [13], which provides the highest memory cell performance [8]. Fig. 2 illustrates the two reference layouts topologies designed from Ishida (a) and Mann (b). The latter one (Fig. 2b) shows a more regular design, which reduces the lithographic difficulty, although a larger cell area is obtained ($0.81\ \mu m^2$ in front of $0.65\ \mu m^2$). Note that type 5 area could be minimized using local interconnections.

With continued CMOS scaling, the lithography effects on yield have become a growing concern due to the difficulty of printing lines much narrower than the current light wavelength, 193 nm. As a consequence a decrease in design dependability has been observed. We have identified and fixed the problematic pattern in order to meet acceptable yields [6]. Lithography simulation tools have been developed to predict the sensitivity of designs to process variations which allows them to be tweaked at the design

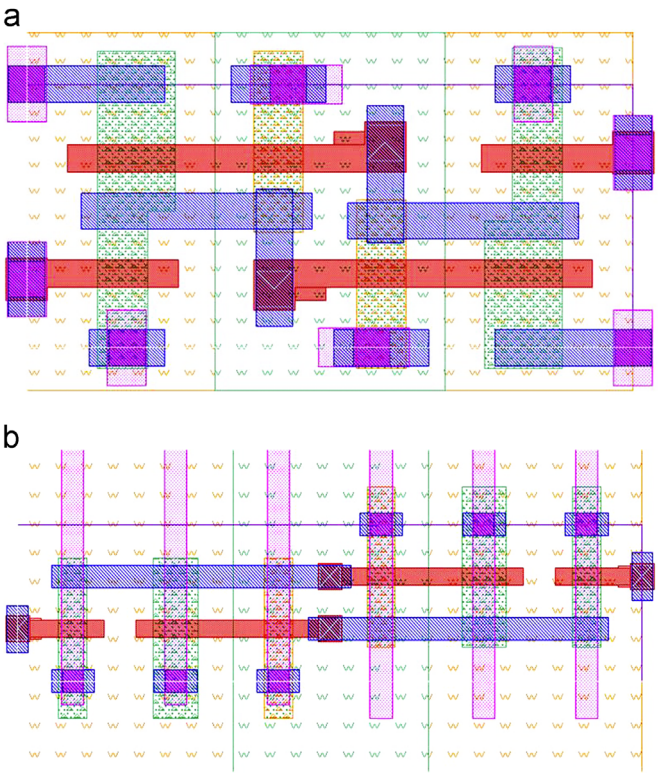

Fig. 2. SRAM bit-cell layouts implemented in this work. (a) Ishida's and (b) Mann's topology. Larger regularity and lower complexity is observed in the second one. red: poly, blue: metal 1, pink: metal 2, cross: contact, orange: nMOS and green: pMOS. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

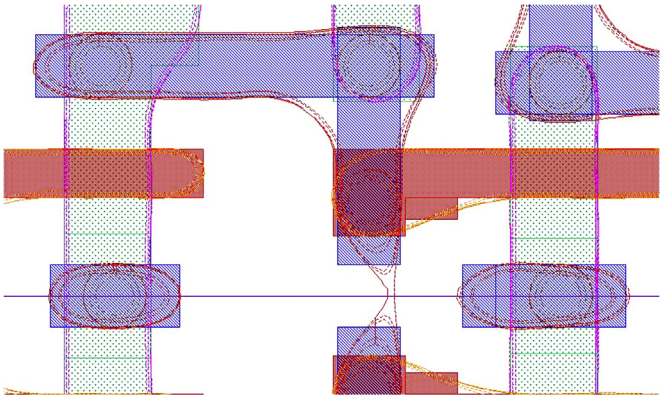

Fig. 3. Example of type 4 M1 lithography errors solved in this work, using lithographic tools.

phase. In this sense, several verifications with the Caliber Litho Friendly Design (LFD) [16] were necessary to guarantee error free lithography results, such as proximity effects which appeared between metal 1 (M1) features of adjacent cells. For instance, Fig. 3 shows the effect of the small distance between M1 features which caused them to be printed together forming undesired shortenings. These issues reveal how important lithography simulations are, and it shows that Design Rule Check (DRC) clean layouts are currently not enough to ensure a valid printable design.

With this in mind we have also used NCSU's LithoSim Kit 1.2 [17] along with Caliber LFD to model lithographic effects and produce litho process variation bands. These Process Variation bands (PV-bands) depict the area in which a given feature will

print as the process conditions vary. As they are context sensitive, the PV-band for a given feature is different from the PV-band for the same aspect in a different location with other neighboring features. Moreover, the across-field (position in reticle) variations are related to photolithographic process parameters and etching sources, i.e. dose and focus. Dose shift is due to a variation in light intensity across the wafer during the manufacturing process, whereas focus changes are caused by a variation in the alignment of the wafer on the *Z*-axis, as well as different film stack thickness variations. The effects of across-field variations could contribute to nominal width (W) and length (L) fluctuation. Hence, to analyze the systematic variability, lithographic system variations have been modeled with the worst case combinations of dose ($\pm 5\%$) and focus variations (± 75 nm), provided by the lithograph [17]. Table 1 states the six experimental conditions simulated throughout this paper.

2.2. B. Impact of systematic variability

Six lithographic scenarios have been implemented. The influence of the systematic variability on device dimensions of both 6T cells are depicted in Table 2. Different effective transistor widths (W) and lengths (L) are obtained for each 6T cell device at every lithographic scenario as well as for both layout topologies. The difference is related to the lithographic distortions. These transistor dimensions will be used for all the studies performed throughout this paper to determine the cell behavior. Additionally, the cell ratio obtained from the relation between the driver transistors and access transistors of the 6T cells, which monitor cell stability [5], is also represented. In this context, the difference between the analyzed scenarios indicates that both A6 configurations would provide the worst cell results.

Table 1
Lithographic scenarios assumed in this work to analyze the systematic variability.

Scenarios	Focus	Dose
A1	Std.	Std.
A2	Std.	1%
A3	+75 nm	−5%
A4	+75 nm	+5%
A5	−75 nm	−5%
A6	−75 nm	+5%

Table 2
Lithographic variability impact on 6T-SRAM cell device dimensions (W and L) obtained for both layout topologies: (a) Type 4 and (b) type 5. Cell ratios are also shown giving an idea of the cell stability.

(a) Type 4

Scenario	Pull-down		Pull-up		Cellratio
	W	*L*	*W*	*L*	
Ref.	140	50	90	50	1.55
A1	139.25	50.2	89	50	1.55
A2	138.5	49.75	88.75	49.58	1.54
A3	140	51.4	90.75	51.56	1.55
A4	133.4	45.3	85.25	45.3	1.48
A5	137.25	47.4	88.75	48	1.52
A6	130	40.4	83	41.1	1.44

(b) Type 5

Scenario	Pull-down		Pull-up		Cellratio
	W	*L*	*W*	*L*	
Ref.	140	50	90	50	1.55
A1	140	50	90	50.1	1.55
A2	139	49.3	90.75	49.6	1.54
A3	140.5	50.5	85.25	51.1	1.56
A4	134	44.5	88.75	45.1	1.48
A5	138	45.7	83	47	1.53
A6	130.7	38.8	82	40.2	1.45

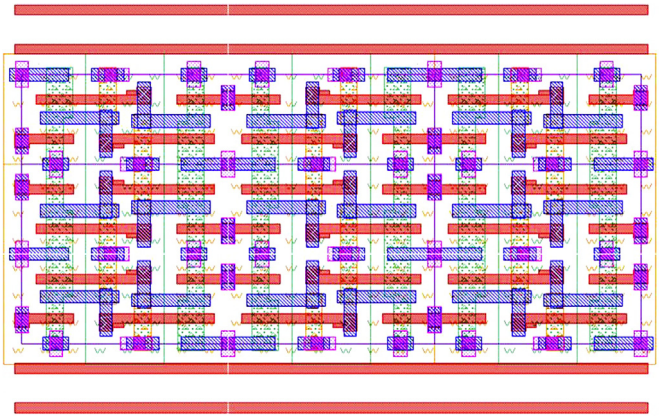

Fig. 4. Type 4 3×3 bitcells layout used to obtain both noise margin values (SNM and RNM). The rectangular zone depicts the analyzed 6T-SRAM cell. red: poly, blue: metal 1, pink: metal 2, cross: contact, orange: nMOS and green: pMOS.

Table 3
Difference between the resulting SNM and RNM values after the performance of the six different topologies.

Scenario	SNM variation		RNM variation	
	Type 4	**Type 5**	**Type 4**	**Type 5**
Ref.	0.3426 V		0.1922	
A1	0.3%	0.0%	0.1%	0.0%
A2	−0.5%	−1.3%	−0.3%	−1.1%
A3	2.2%	0.9%	2.3%	0.9%
A4	−11.7%	−14.3%	−10.1%	−12.8%
A5	−5.3%	−9.8%	−5.5%	−10.1%
A6	−37.8%	−51.3%	−32.1%	−45.1%

Hereafter, with the obtained 6T-SRAM cell device dimensions, we have simulated the memory cell performance to get the SNM and RNM values for each topology at each lithographic scenario. For more realistic values, our cell topology has been inserted in a 3×3 bit-cell array for each layout type. For instance, Fig. 4 shows our type 4 bit-cell in the center with a surrounding topology that approaches the cells performance in a denser environment. Moreover, two additional lines of dummy poly features are added to the 3×3 array layout, parallel to existing functional poly features and using the same spacing as within the bit-cell. This ensures consistent neighboring features for the edge cells at the poly layer.

Table 3 illustrates the nominal SNM and RNM values obtained for a memory cell implemented with the reference dimensions (Ref). We have related this to a scenario without any kind of process fluctuation, and it is compared to the other topologies, expressing the difference as a percentage. A1 scenarios depict that even with no focus or dose deviations the calculated SNM and RNM factor differs slightly from the reference (ideal sizing), since this deviation is due to the sub-wavelength lithography distortion. The other simulations introduce across-field variations, whose effect on the SNM is much greater. Type 5 cell presents slightly lower SNM values (worse performance) than type 4. This is probably related to the smaller device dimensions obtained for type 5 topology (Table 2). A similar tendency is obtained for RNM values. Moreover, both layout topologies follow the same overall trend, responding particularly badly to the A6 scenario, in accordance to the worst cell ratio presented in Table 2.

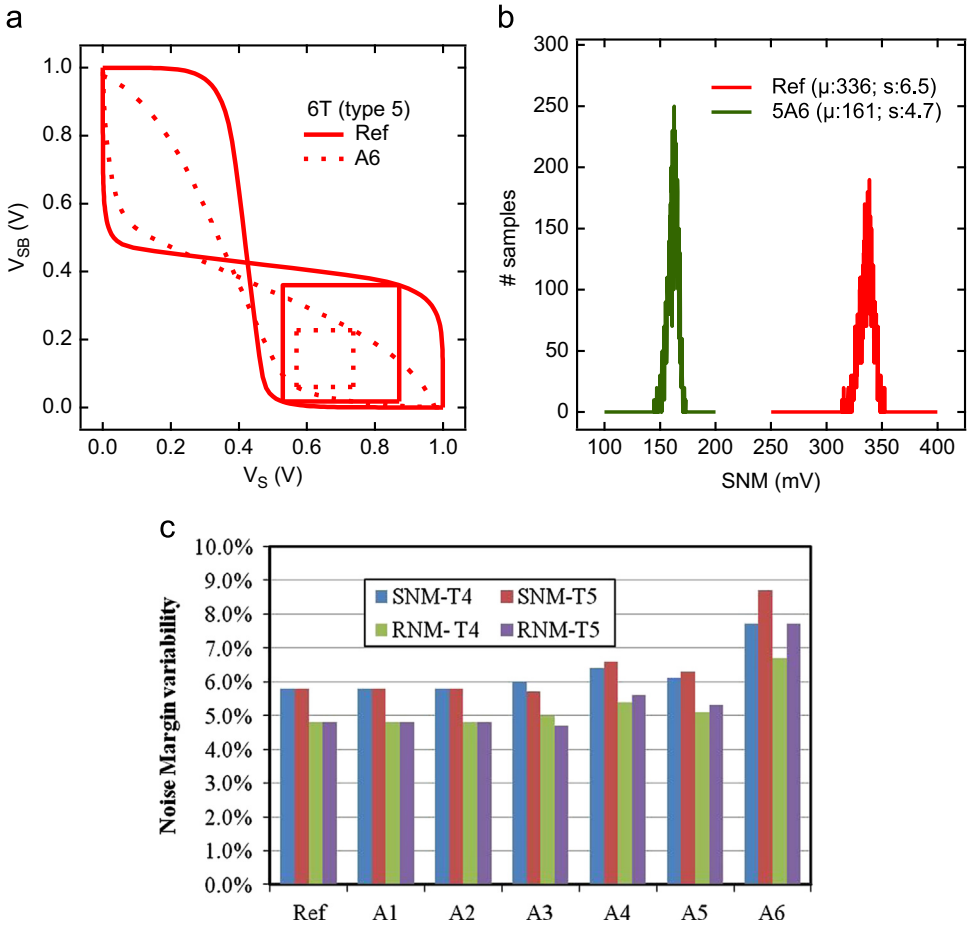

Fig. 5. (a)VTC example, where SNM are extracted from, obtained for type 5 topology in front of Ref and A6 scenarios. (b) Histogram of the SNM values for Ref and 5A6 cells. (c) Variability influence in SNM and RNM parameters for every layout topology and lithographic scenario.

3. Study of random variations

In this section we analyze the impact of random variability in all 6T-SRAM cells, with the device dimensions previously reported for every lithographical scenario. In order to simulate the random variations we have assumed the RDF as the main process variation source, with a V_T-shift of each cell device being the main consequence. We have taken into account that the variability amount depends on the device dimensions [9]. Therefore, we have assumed a 4% V_T fluctuation [18] for the minimum dimensions. In order to study the impact of the V_T variation, 10,000 Monte Carlo simulations have been performed. For all the tables the fluctuation will be analyzed with the $3\sigma/\mu$ ratio, expressed as a percentage. To monitor the variability influence on 6T-SRAM cells, several parameters have been analyzed: SNM, RNM, access times, write and read (WAT and RAT, respectively) and dynamic Power consumption (PW).

Fig. 5a shows the SNM performance depicted in the Voltage Transfer Curve (VTC) obtained from our 6T-SRAM cell, where type 5 topology is under Ref and A6 lithography scenarios. Significant SNM difference is observed between both cell scenarios and which entails the worst cell performance in the 5A6 case. Moreover, Fig. 5b illustrates the histogram of both SNM distributions when the variability impact is considered. Larger variability impact is observed for a 5A6 scenario. Afterwards, Fig. 5c depicts the process fluctuation impact on SNM and RNM (as a percentage) for both layouts at each studied case. We observe an insignificant difference between both layout topologies for most of the studies. However, A6 scenarios show a relevant variability increase in comparison with Ref. samples, which could be related to the cell ratio of each configuration. Moreover, similar performance is observed between SNM and RNM.

Table 4
Variability impact for WAT, RAT and PW. Similar performance is observed for both layout topologies. Only PW at A6 scenarior shows a significant difference.

Scenario	WAT		RAT		PW	
	Type 4	Type 5	Type 4	Type 5	Type 4	Type 5
Ref.	8.5		12.6		2.6	
A1	8.5	8.5	12.6	12.6	2.6	2.6
A2	8.4	8.4	12.6	12.6	2.6	2.6
A3	8.6	8.6	12.6	12.6	2.6	2.6
A4	8.1	8.1	12.9	12.9	2.7	2.7
A5	8.1	8.1	12.9	12.9	2.6	2.6
A6	9.9	10.6	13	12.8	19.2	27.7

Table 4 presents the variability influence focused on cell parameters (WAT, RAT and PW). A slight increment of the variability relevance on the 6T-SRAM cell performance has been obtained, whereas similar tendency has been depicted between both topologies. An insignificant difference has been observed between all the analyzed scenarios in front of the reference values. In fact, we notice a larger increase in power consumption for the A6 scenario, whatever topology has been analyzed. This could be related to the smaller device dimensions obtained for this lithographic scenario (Table 2), since less device channel length entails an exponential power consumption increase.

4. Aging influence

To complete the reliability analysis of the different 6T-SRAM cells scenarios, the introduction of device degradation is required to study the memory cell performance. In this context note that we have implemented our cell designs using FreePDK45 libraries, whose transistor model is based on SiO_2 material as a gate dielectric. This means that NBTI, which is only produced in the pMOS, is the main degradation mechanism to be examined [11]. Therefore, we assume that only one of the two pMOS pull-up devices would be affected by the degradation. Subsequently we have also considered the usual static behavior of the cell that means that only one the two pMOS will be damaged. To simulate the aging of the device, we have ranged a V_T increase from 10 to 200 mV. Moreover, throughout this section, we have only analyzed the aging influence on the extreme lithographic cases, the reference (Ref.) one and A6 lithographic scenario for both topologies, type 4 and 5 (4A6 and 5A6).

4.1. A. Aging influence on SNM values

Fig. 6 illustrates the impact of V_T-shift on the SNM evolution. Note that the cell variability is also taken into account. In this sense, Fig. 6a shows the impact of the aging introduction on SNM values. We observe that for a V_T-shift lower than 50 mV a small variation is obtained, while for larger values a significant increase is shown. Meanwhile, when we analyze the SNM variability, we can distinguish two regions. Below 100 mV V_T-shift a steep slope is observed, while for higher V_T variations a flatter one is obtained. All the analyzed scenarios (Refs. 4A6 and 5A6) present the same tendency, showing a consistent performance. To explain this behavior, Fig. 6b points out the influence of NBTI degradation on the behavior of mean (μ) and standard deviation (σ) related to the SNM values. The former presents a continuous reduction for all the cases as the threshold voltage shift increases, which explains the greater SNM aging. On the other hand, σ-SNM shows a relevant initial increase till 100 mV, then, for larger values σ becomes constant or even a slight reduction is observed. This could explain the lower slope of the SNM variability at V_T-shift greater than 100 mV, since at this range σ remains constant but μ still reduces, what involves lower SNM variation. A similar performance is obtained when the RNM parameter is considered (not shown).

4.2. B. Degradation influence on cell timing

In this section, the influence of cell degradation on access times and power consumption are analyzed. In these terms, Fig. 7 shows the impact of V_T shift in relation to cell variability. In fact, Fig. 7a presents a similar performance for all the analyzed scenarios, and only WAT presents a noticeable reduction for the three cases. Meanwhile, Fig. 7b shows a linear increase of WAT for every cell configuration, when we focus on cell parameter degradation. This is related to the higher sensitivity of the write access time in front of the NBTI stress [8]. The steepest slopes are obtained for A6 configurations. Otherwise, RAT depicts a negligible influence of

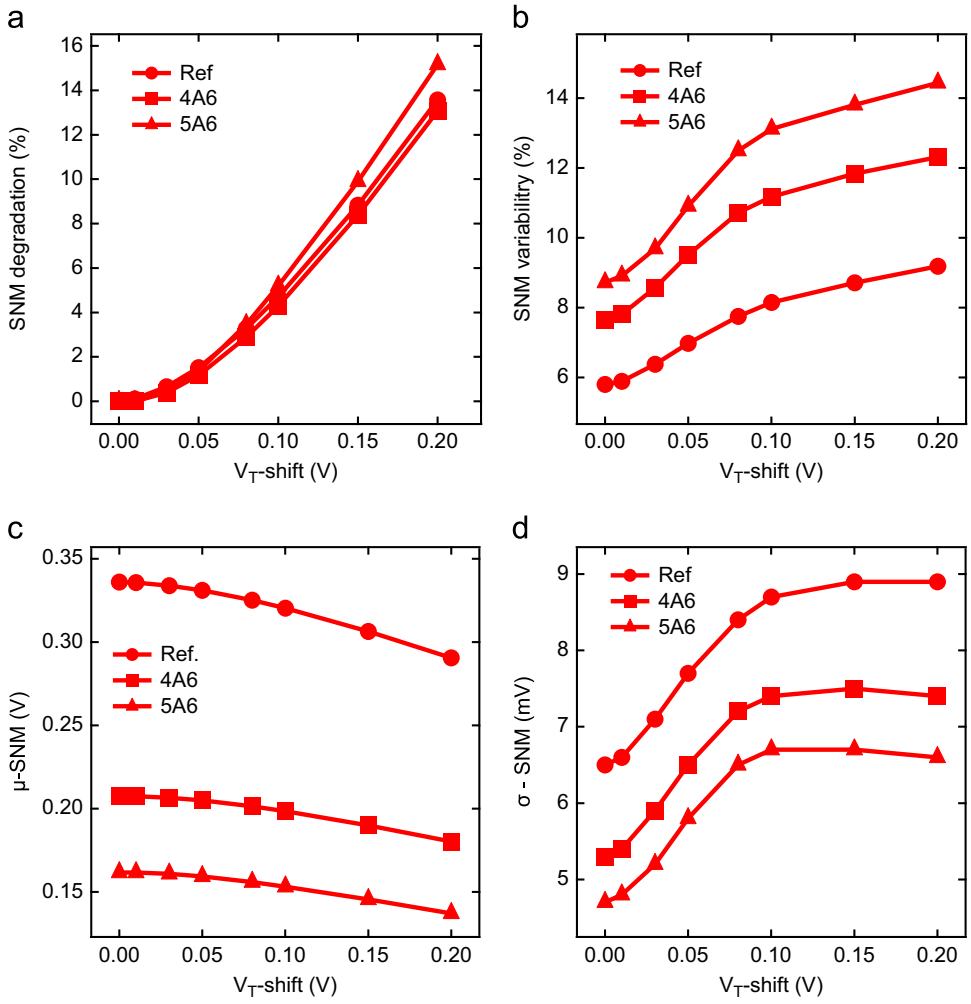

Fig. 6. Study of the aging influence on SNM performance. i.e. percentage of degradation (a), variability (b), variation of μ-SNM (c) and σ-SNM (d) in front of the V_T-shift.

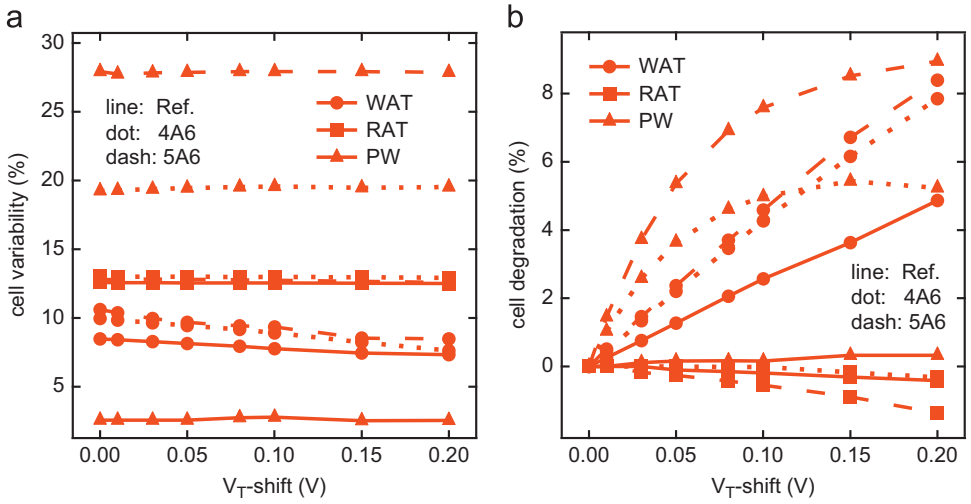

Fig. 7. Influence of the cell aging on the different cell configurations and cell parameters: WAT (circles), RAT (squares) and PW (triangles), when cell variability is analyzed (a) and for the parameters aging (b).

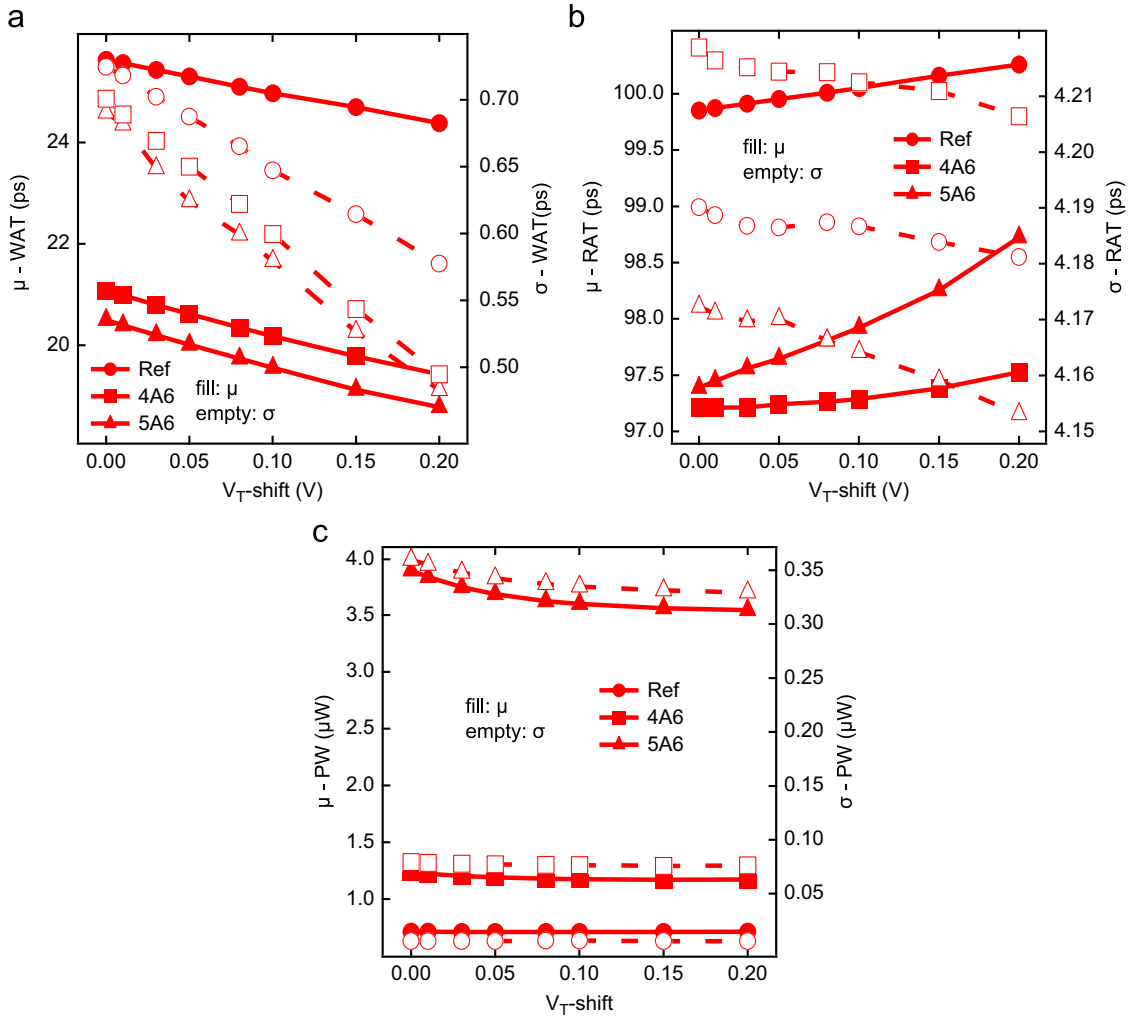

Fig. 8. Study of the behavior of WAT (a), RAT (b) and PW (c) when the 6T-SRAM cell is affected by degradation for all the analyzed layout scenarios (Refs. 4A6 and 5A6). Mean (μ, fill) and standard deviation (σ, empty) values are represented and the aging influence on the V_T-shift is observed.

cell aging in accordance to its small influence of NBTI aging [8]. In particular, PW presents a significant increase for both A6 scenarios, while the reference sample shows negligible damage. In this context, if we compare SNM and WAT-RAT-PW results (Figs. 6a and 7b, respectively), we could observe a larger impact for SNM (~15% in front of ~8%) subjected to device aging. This could

determine a larger relevance of the SNM shift, due to its more detrimental behavior on cell aging.

To understand this performance, Fig. 8 depicts the mean and standard deviation tendency for the three cell scenarios as V_T-shift increases. Fig. 8a illustrates the V_T-shift impact on WAT, and we observed that both μ and σ reduce, but with different slopes (higher for σ than for μ). This explains the smaller variability reduction observed in Fig. 7a as the cell aging increases. Meanwhile, Fig. 8b represents RAT behavior, and a similar tendency is observed for all cells. Only 5A6 mean shows a slightly bigger slope which explains the small influence of the cell damage observed in Fig. 7a. Fig. 8c points out the relevance of V_T-variation on PW trend. Parallel shapes are obtained for all the cases (μ and σ). This clarifies the non-influence of the damage observed on cell variability (Fig. 7a), while a noticeable influence of V_T aging that explains the large degradation obtained in Fig. 7b.

5. Conclusions

In this work, two 6T-SRAM layout topologies have been designed following different regular layout styles to analyze their influence on the final cell behavior. Higher regular patterns have involved lower complexities, i.e. fewer process difficulties in terms of fewer design rules to be contemplated. So, a regular cell could be a promising option to facilitate circuit design and reduce layout problems.

The performance of both different layout topologies has been analyzed, when they are subjected to different variability types, i.e. systematic and random. Systematic variations (at lithographic level) show a dependence on dose and focus variations, and as a consequence significant differences between the W and values are depicted, due to the lithographic process variations. In order to analyze the random variability, several cell parameters (SNM, RNM, access times and power consumption) have been taken into account. Insignificant differences between both layout topologies have been noticed. We have observed that the SNM parameter is the most important cell parameter at the reliability level.

Meanwhile, the analysis of cell behavior in front of NBTI aging has shown a more relevant behavioral variation between both extreme scenarios. While cell timing and power consumption have a low influence on cell aging, SNM has depicted the most detrimental impact on cell performance. In this regard, an insignificant difference has been observed between both layout topologies analyzed when studies of variability and aging are performed.

Acknowledgments

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