A comparative study of terminal and conventional sliding mode start-up peak current controls for a synchronous buck converter

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Abstract—An alternative to the linear control techniques, which are based on small signal averaged models, is the sliding mode control. That method uses instantaneous models of the switched power converter to design robust controllers. The large signal modelling allows not only to control the system behaviour around the steady-state, but also the start-up transient. This paper presents the design of two sliding mode controllers that regulate the output voltage of a synchronous buck converter and limit the start-up peak current. A terminal sliding mode control is designed and compared with a first order sliding mode control, which is called here as a conventional sliding mode control. The study shows that the terminal sliding mode control presents lower transient time to reach the final value as compared to the conventional one because of its finite time convergence property. It also achieves better performance in terms of line and load regulation. A power converter prototype of 150 W / 100 kHz is assembled and both sliding mode controllers are digitalized and implemented in a microcontroller. Numerical simulations and experimental results validate the proposal.

Index Terms—Sliding mode control, terminal dynamics, synchronous buck converter.

I. INTRODUCTION

Switching power converters are present in almost all industrial and household equipments. They can be found in smartphones, household appliances, elevators, electric vehicles, photovoltaic systems [1]–[4], etc. The most important feature of these systems is their high efficiency, normally above 90 %. This property comes directly from their working principle: high switching frequency operation of electrical circuits based on semiconductors, acting as switches, and reactive elements. Therefore, the control inputs are discontinuous and the dynamic characterization of the power system is bilinear. In order to design a controller using well-known linear techniques, normally an averaging procedure is applied and the discontinuous control is replaced by a continuous one, the so-called duty cycle [5], [6]. The averaged models are often linearized by using a small signal method around the nominal working point. As a result, the design achieves the required regulation in steady-state but the robustness of the system parameters is compromised. Furthermore, the system start-up usually needs to be controlled with soft-start algorithms [7], or by adding specific circuitry [8], [9] or by changing the power stage [10].

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Sliding mode control (SMC) fits perfectly with the power converter's discontinuous control. SMC operates over the control action by sign functions, switching at high frequency between two discrete states. In the power converters, these discrete values correspond to the ON and OFF state of the switches. Furthermore, the chattering characteristic of the sliding mode, which for some systems is an important drawback, is inherent to the power converters operation. Theoretically, the conventional sliding mode control (CSMC) is based on enforcing the system trajectories to evolve onto a desired manifold, where the system slides asymptotically to the desired steady-state, providing a very good robustness and a fast transient response. The application of CSMS to power converters has been proposed in the literature [11], [12]. Recently, CSMC has also been successfully implemented by several authors [13]–[20], where its main implementation problem, namely variable switching frequency, has been largely amended.

An improvement of the CSMC was proposed in [21], where the sliding parameters are on-line adjusted for minimizing the convergence time to the origin. Alternatively, terminal sliding mode control (TSMC) slightly modifies the structure of the CSMC to achieve finite time convergence to the steady-state. The difference resides in the manifold where the system trajectories slide, by changing the linear hyperplanes of the CSMC to nonlinear switching surfaces in TSMC. With this modification, TSMC preserves all the benefits of the CSMC but achieves finite time convergence to the origin. In [22], an initial formulation was proposed for the application of TSMC to power converters. Following that idea several works have been developed to apply TSMC to a wind energy conversion system [23], to step-up converters [24] or to design a TSMC observer for a *Buck* converter [25]. One of the main issues to be overcome when implementing TSMC is related to the nonlinearity of the switching function. This problem has been studied from a theoretical point of view in [26], where some aspects about TSMC discretization are discussed, or in [27], where the TSMC dynamic behaviour is analysed. As it has been noted already, a lot of works exist on the study of the TSMC but it is very hard to find practical approaches for power converters. One of those works is of Yazici and Yaylaci [24], in which a TSMC is implemented for a boost converter showing good results.

Both CSMC and TSMC are designed by using large signal model. This means that the behaviour of the system is globally controlled, unlike a linear controller that is designed based on small-signal models. Therefore, different issues related to

the converter operation can be controlled simultaneously, such as robustness, steady-state performance or start-up transient. An interesting point to be studied is how CSMC and TSMC behave during transients; at the start-up or load changings. Studies can be found in the literature following this idea, e.g.; the work of Martínez-Salamero et al. [10], where two switching surfaces are combined to get start-up control and voltage regulation in the steady-state, and the work of Xiu et al. [28], where a study of the reaching law in sliding mode is presented.

In this paper, a CSMC and a TSMC are designed to control the start-up peak current of a synchronous buck converter. A comparative study of the behaviour of both CSMC and TSMC is provided. The desired goal is to obtain a fast convergence to the steady-state (in the case of the CSMC to a region close to the steady-state) without exceeding the maximum current and, hence, avoiding components saturation and/or converter malfunctioning. Thanks to the finite-time convergence property, the TSMC shows perfect line regulation in practice. The exponential term required in the TSMC have been calculated through a direct look-up table (LUT) providing an accurate result with a low execution time by the μC . The LUT has been programmed in order to keep a good emulation of the exponential function in face of input voltage, desired output voltage and power levels variations.

For the experimental evaluation, an implementation method that preserves the continuous time TSMC and CSMC dynamics in a digital implementation is applied [29]. That technique implements a digital emulation of a continuous time hysteresis comparator, where a pulse width modulator is used as a set-reset flip flop. The proposed controllers are implemented in a well-known digital control board (μC F28377) and experimental results in a 150 W power stage with a switching frequency of 100 kHz are obtained.

This paper is structured as follows. The synchronous buck converter dynamical model is presented in Section II. The design of the CSMC and the TSMC for the start-up peak current control is derived in Section III, followed by a set of simulation results comparing both techniques in Section IV. The implementation details are in Section V. Experimental results of both approaches are shown in Section VI. Finally, conclusions are drawn in Section VII.

II. SYNCHRONOUS BUCK CONVERTER MODEL

Equations (1) and (2) describe the dynamics of the inductor current and the output voltage of the synchronous Buck converter depicted in Fig. 1:

$$\frac{di_L}{dt} = \frac{1}{L}(uE - v_c), \quad (1)$$

$$\frac{dv_c}{dt} = \frac{1}{C}(i_L - \frac{v_c}{R}). \quad (2)$$

The control signal, $u \in \{0,1\}$, takes the value $u = 1$ when $M1$ is turned on and $M2$ is open and $u = 0$ otherwise.

Defining the state variables:

$$x_1 = v_c - v_c^*, \quad (3)$$

$$x_2 = \dot{x}_1 = \dot{v}_c, \quad (4)$$

Figure 1. Synchronous Buck converter.

where v_c^* is the reference output voltage, (1) and (2) are rewritten as:

$$\dot{x}_1 = x_2, \quad (5)$$

$$\dot{x}_2 = -\frac{x_2}{RC} + \frac{1}{LC}(uE - v_c^* - x_1). \quad (6)$$

Assuming that the control signal is constant, $u = u^*$ the equilibrium point of the system given by (5) and (6) is ($x_1^* = u^*E - v_c^*$, $x_2^* = 0$). Therefore, stabilizing the system to the origin will entail the desired regulation target, $v_c = v_c^*$.

III. DESIGN OF SLIDING MODE CONTROLLERS IN A SYNCHRONOUS BUCK CONVERTER

This section is devoted to the design of the sliding mode controllers, namely: the CSMC (subsection III-A) and the TSMC (subsection III-B).

A. Conventional Sliding Mode Control (CSMC)

The switching function of the CSMC uses a linear combination of the state variables:

$$s = \lambda x_1 + x_2, \quad (7)$$

where $\lambda > 0$ is the sliding parameter. Therefore, the sliding straight line $s = 0$ crosses the origin of the phase plane and has a slope given by $(-\lambda)$, as it is depicted in Figure 2. Furthermore, the sliding dynamics is obtained by imposing $s = 0$ in (7) and replacing in (5):

$$x_1(t) = x_1(t_0)e^{-\lambda(t-t_0)}, \quad (8)$$

which shows that $x_1(t)$ converges exponentially to the equilibrium. The required time, t_f^{CSM} , to get a value close to the origin, $x_1(t_f)$, starting from an initial value $x_1(t_0)$ is given by:

$$t_f^{CSM} = -\frac{1}{\lambda} \int_{x_1(t_0)}^{x_1(t_f)} \frac{dx_1}{x_1} = \frac{1}{\lambda} (\ln |x_1(t_0)| - \ln |x_1(t_f)|). \quad (9)$$

The control law needed to produce sliding mode on $s = 0$, is derived by requiring $s\dot{s} < 0$. From this last expression, it is straightforward to show that such control signal is:

$$u = \frac{1}{2}(1 - \text{sign}(s)). \quad (10)$$

The practical control uses a hysteresis comparator to set the steady-state switching frequency. Hence, the control signal is redefined as:

$$u = \begin{cases} 1 & \text{if } s < -h \\ 0 & \text{if } s > h \end{cases}, \quad (11)$$

where $h > 0$ is the hysteresis bandwidth.

The equivalent control [30] is the ideal value that the control signal should take when the system slides. Hence, the equivalent control for the CSMC is obtained by imposing $s = \dot{s} = 0$, and it is given by:

$$u_{eq}^{CSM} = \frac{LC}{E} \left(\frac{x_2}{RC} + \frac{1}{LC} (x_1 + v_c^*) - \lambda x_2 \right), \quad (12)$$

which depends on the state and the control parameters. Sliding motion is enforced when u_{eq} takes values between the minimum and the maximum value of the control signal, u . Therefore, for the synchronous Buck converter the inequality $0 < u_{eq} < 1$ has to be fulfilled.

In this work, the sliding parameter, λ , is designed to limit the start-up peak current. Hence, assuming that the power converter starts up with no reactive power, that is $i_L = 0$ and $v_c = 0$, the initial condition in the new variables framework is $x_1(0) = -v_c^*$ and $x_2(0) = 0$. Therefore, in order to set the maximum value of the current, i_{Lmax} , λ is designed in such a way that the start-up free system trajectory for $u = 1$ (reaching mode) crosses the switching surface $s = 0$ for the state $(\tilde{x}_1, \tilde{x}_2)$, where $\tilde{x}_2 = \frac{1}{RC} (Ri_{Lmax} - (\tilde{x}_1 + v_c^*))$. The start-up system trajectory can be seen in Figure 2. In this case, the system reaches the sliding line (purple color for the CSM) after a free dynamics transient, known as reaching mode, from the initial condition $x_1(0) = -v_c^*$ and $x_2(0) = 0$. It should be remarked that $\tilde{x}_1$ is determined by calculating the solution of the system defined by (5) and (6). Finally, considering that in the crossing point $\lambda\tilde{x}_1 + \tilde{x}_2 = 0$, λ is obtained as:

$$\lambda = -\frac{\tilde{x}_2}{\tilde{x}_1}. \quad (13)$$

Once the switching surface is reached, the system trajectory slides (sliding mode) towards the equilibrium with the dynamics given by (5) and (8), as long as the system is within the sliding domain defined by $0 < u_{eq}^{CSM} < 1$.

B. Terminal Sliding Mode Control (TSMC)

The terminal sliding mode control is characterized by its nonlinear switching function, which answers to:

$$s_t = \lambda x_1^\gamma + x_2, \quad \lambda > 0, \quad 0 < \left(\gamma = \frac{n}{d} \right) < 1, \quad (14)$$

where the parameters n and d are odd positive integers. The ideal sliding motion is obtained by imposing $s_t = 0$ in (14). Doing so and replacing in (5), the ideal sliding dynamics of x_1 is given by the following nonlinear differential equation:

$$\dot{x}_1 = -\lambda x_1^\gamma, \quad (15)$$

with solution:

$$|x_1(t)|^{1-\gamma} - |x_1(t_0)|^{1-\gamma} = -\lambda(1-\gamma)(t-t_0). \quad (16)$$

From (16), the required time to reach a value close to the equilibrium, $x_1(t_f)$, from an initial condition, $x_1(t_0)$, is found as:

$$t_f^{TSM} = -\frac{1}{\lambda} \int_{x_1(t_0)}^{x_1(t_f)} \frac{dx_1}{x_1^\gamma} = \frac{|x_1(t_0)|^{1-\gamma} - |x_1(t_f)|^{1-\gamma}}{\lambda(1-\gamma)}. \quad (17)$$

In particular, assuming $t_0 = 0$, the system achieves the value $x_1 = 0$ at the time instant:

$$t_s^{TSM} = \frac{|x_1(0)|^{1-\gamma}}{\lambda(1-\gamma)}, \quad (18)$$

which means that the steady-state is reached in finite time.

The terminal switching function depends on two parameters, λ and γ , therefore there are different combinations of the parameters leading to functions that cross the same reaching point in the phase plane, $(\tilde{x}_1, \tilde{x}_2)$, and also contain the equilibrium. Figure 2 illustrates this idea. Notice that by direct comparison of (7) and (14) it concludes that TSMC would become the CSMC for $\gamma = 1$.

Figure 2. Switching functions in the phase plane (x_1, x_2) with the same reaching point ($i_{Lmax} = 12A$).

The design of the sliding parameters is carried out in order to meet three different goals, namely: First- to ensure the desired start-up peak current, Second- to optimize the settling time to reach the equilibrium and Third- to guarantee sliding regime on the switching surface. The following items detail the proposed design method:

- Regarding the first goal, the sliding parameters have to verify the equation:

$$\lambda = -\frac{\tilde{x}_2}{\tilde{x}_1^\gamma}, \quad (19)$$

where the reaching point $(\tilde{x}_1, \tilde{x}_2)$, see Fig. 2, is calculated numerically following the above exposed procedure exposed in Subsection III-A. Thus, considering the converter parameters shown in Table I, and taking $i_{Lmax} = 12A$, the reaching point becomes $(-23.603, 11.96 \cdot 10^4)$ and $\lambda = \frac{11.96 \cdot 10^4}{23.603^\gamma}$. Figure 3 depicts the pairs of (γ, λ) that accomplish this last equation. Notice that there is a certain number of combinations of pairs (γ, λ) fulfilling (19) since, from (14), γ is a quotient of odd positive integers. Moreover, for $\gamma = 1$ the switching function given by (14) becomes linear, thus corresponding to the CSMC design, and the value of $\lambda = 5.067 \cdot 10^3$ can be calculated from (19).

Figure 3. Pairs (γ, λ) providing the same start-up peak current ($i_{L_{max}} = 12$ A) with a terminal switching function.

- Concerning the second item, the required time to get the origin once the system reaches the switching surface can be determined by replacing (19) in (18) and noticing that $x_1(0) = \tilde{x}_1$, this yielding to:

$$t_s^{TSM}(\gamma) = \frac{|\tilde{x}_1|}{|\tilde{x}_2|(1-\gamma)}. \quad (20)$$

Since $t_s^{TSM}(\gamma)$ is monotonically increasing with γ , the design should consider the lowest possible value of that parameter. Notice also that t_s^{TSM} tends to infinite when γ is approaching one, thus fitting the exponential convergence property of the CSMC behaviour. Furthermore, the start-up TSMC dynamics of the converter output voltage is faster than the CSMC one. This statement can be easily proved by linearizing the sliding surfaces around the point $(\tilde{x}_1, \tilde{x}_2)$, thus yielding: $x_2 - \tilde{x}_2 = \frac{\tilde{x}_2}{\tilde{x}_1}(x_1 - \tilde{x}_1)$ for the CSMC and $x_2 - \tilde{x}_2 = \gamma \frac{\tilde{x}_2}{\tilde{x}_1}(x_1 - \tilde{x}_1)$ for the TMSC. Since $\gamma < 1$, the slope of the TMSC linearized sliding surface is higher than the CSMC one at the reaching point and the value of x_2 for the TMSC sliding surface is always higher than the CSMC one for the same x_1 , see figure 2. Therefore, the TMSC $x_1(t)$ behaves faster than the CSMC one.

- The last condition is the most restrictive one. Following the previously detailed analysis, it is easy to show that the control law

$$u = \begin{cases} 1 & \text{if } s_t < -h \\ 0 & \text{if } s_t > h, \end{cases} \quad (21)$$

enforces sliding motion in s_t when the inequality $0 < u_{eq}^{TSM} < 1$ is fulfilled. The equivalent control for the TSM is found as:

$$u_{eq}^{TSM} = \frac{LC}{E} \left(\frac{x_2}{RC} + \frac{1}{LC} (x_1 + v_c^*) - \lambda \gamma x_1^{\gamma-1} x_2 \right). \quad (22)$$

The equivalent control depends on the sliding parameters, λ and γ , which can take different values according to (19). As a consequence the sliding domain is also influenced by the chosen pair (γ, λ) . Figures 4, 5 and 6 show the terminal switching surfaces and the locus of

the phase plane points that verify $u_{eq} = 0$ (blue colour) and $u_{eq} = 1$ (red colour) for $\gamma = 0.20$, $\gamma = 0.44$ and $\gamma = 0.68$. Notice that the sliding motion is lost around the origin in the cases $\gamma = 0.20$ and $\gamma = 0.44$, whereas it is ensured for $\gamma = 0.68$. The case $\gamma = 0.44$ is interesting since the crossing point between the terminal switching surface and $u_{eq} = 1$ occurs very close to the origin and, taking into account the hysteresis bandwidth, the loss of sliding mode can be neglected in practice.

Figure 4. Terminal switching surface and locus for $u_{eq} = 0$ (blue) and $u_{eq} = 1$ (red) for $\gamma = 0.20$.

Figure 5. Terminal switching surface and locus for $u_{eq} = 0$ (blue) and $u_{eq} = 1$ (red) for $\gamma = 0.44$.

Table I
BUCK CONVERTER PARAMETERS

Parameter	Symbol	Value
Input voltage	E	40 V
Reference voltage	v_c^*	24 V
Inductor	L	22 μ H
Capacitor	C	100 μ F
Nominal load	R	10 Ω

C. Sliding mode controllers design procedure

Considering the previous study, the control parameters design guidelines can be summarized in the following steps:

Figure 6. Terminal switching surface and locus for $u_{eq} = 0$ (blue) and $u_{eq} = 1$ (red) for $\gamma = 0.68$.

- 1) Set the values of i_{Lmax} and v_c^* .
- 2) Determine the state $(\tilde{x}_1, \tilde{x}_2 = \frac{1}{RC}(Ri_{Lmax} - (\tilde{x}_1 + v_c^*)))$ from the solution of (5) and (6), assuming that the initial condition is $x_1(0) = -v_c^*$ and $x_2(0) = 0$.
- 3) Calculate $\lambda = -\frac{\tilde{x}_2}{\tilde{x}_1}$ for the CSMC.
- 4) Select the lower value of γ that fulfils the inequality $0 < u_{eq}^{TSM} < 1$, where u_{eq}^{TSM} is given by (22), and calculate $\lambda = -\frac{\tilde{x}_2}{\tilde{x}_1}$ for the TSMC

Finally, applying the detailed procedure, the designed values of the sliding parameters are: $\gamma = 0.44$ and $\lambda = 2.97 \cdot 10^4$ for the TSMC, and $\lambda = 5.067 \cdot 10^3$ for the CSMC.

IV. SIMULATION RESULTS

The simulation results obtained with both designs, TSMC and CSMC, are presented in this section. The converter parameters are given in Table I and the controllers' coefficients are the ones designed in the previous section. The simulation pattern is: First- the start-up is performed with a reference output voltage of $v_c^* = 24$ V and a load of 10Ω , Second- at $t = 5$ ms the reference voltage is changed to 12 V, Third- at $t = 8$ ms the reference voltage is taken back to the previous value, Fourth- at $t = 10$ ms the load is changed from 10Ω to 30Ω and, finally, Fifth- the load is switched to 5Ω at $t = 12.5$ ms. In the graphs the TSMC waveforms are plotted in red colour and the CSMC ones are depicted in blue colour.

Figure 7 shows the simulation results of the output voltage, v_c , and the inductor current, i_L , achieved according to the described pattern. Zoomed views are included in the graphs to highlight the differences between the behaviours obtained with the TSMC and the CSMC during the transients. For instance, in the zoomed view of the inductor current, at the start-up, it allows us to easily compare the finite time behaviour of the TSMC with the asymptotic transient of the CSMC. Additionally, it is also confirmed with the output voltage behaviour, which converges to the final value in finite time of $340 \mu s$ in the TSMC. For the CSMC the settling time (considering a 5 % of tolerance around the steady-state value) is of $780 \mu s$. Notice how the dynamics of TSMC in the transients is always faster than the CSMC one.

On the other hand, the start-up peak current is the same for both controllers. The maximum value of the current is of 14 A instead of the theoretical value of 12 A. This difference is due to the hysteresis bandwidth, $h = 2 \cdot 10^4$, calculated to get the desired steady-state switching frequency of 100 kHz. The phase plane shown in Fig. 8, which corresponds to the start-up transient, verifies this idea. In ideal sliding mode, the system trajectory would reach the sliding surface exactly at $(\tilde{x}_1, \tilde{x}_2)$ and would switch at infinite frequency to keep the system in sliding motion. In real sliding mode, the hysteresis produces finite switching frequency, but the system trajectory chatters around the sliding surface, producing currents within 14 A and 10 A, approximately. This effect could be easily included in the design procedure just replacing $(\tilde{x}_2$ by $\tilde{x}_2 - h)$ in equations (13) and (19).

Concerning the reference voltage and load transients, it should be pointed out that the output voltage always recovers the desired value, which means that both controllers present a perfect regulation, and the TSMC shows a faster finite time behaviour whereas the CSMC presents the characteristic first order transient.

V. IMPLEMENTATION DETAILS

A power converter prototype was assembled with the following components: the MOSFET PSMN013100 acting as power switches, $M1$ and $M2$; $2 \times 33 \mu F + 5 \times 10 \mu F$ electrolytic capacitors placed in parallel implementing the output capacitance, C ; the inductance, L , was made with a PQ32/20 ferrite core wound with 12 turns with a saturation current above 20 A. The MOSFET driver LM5106 from Texas instruments has been used. Figure 9 shows a picture of the assembled converter.

The implementation block diagram is shown in Figure 10. The sensing stage includes a voltage divider to measure the output voltage and a transformer to measure the current through the output capacitor, i_c , which is proportional to $\dot{v}_c$. An acquisition board adapts these signals to be acquired by the ADC of the μC . The controllers have been digitally implemented using the board Launchxl-F28377s, based on the F28377s μC . This device incorporates two processing units, the main CPU and the CLA, capable of executing code in parallel. Some implementation issues deserve special attention with regard to the μC : the controllers discretization and the exponential term calculation.

A. Controllers discretization

The sliding mode controllers are digitally implemented according to the technique proposed in [29]. The idea is to use a PWM module as a Set-Reset Flip-Flop, controlling the time instant at which the control signal commutates. In order to keep the switching function within the hysteresis bands, the sampling of the control ($T_s = 1 \mu s$) must be higher than the desired switching period ($10 \mu s$). Moreover, due to the delay produced by the computing time (700 ns), a simple switching function prediction algorithm was proposed, achieving a continuous time hysteresis comparator emulation (see [29] for details). A simulation of the technique is shown in

Figure 7. Simulation results for both the TSMC (red) and the CSMC (blue).

Figure 8. Start-up phase plane of the TSMC (red) and the CSMC (blue).

Figure 10. Implementation block diagram. The CPU is just used for plotting signals through DAC for visualization purpose.

Figure 9. Picture of power and control stages.

Figure 11. Sampled simulation for the CSMC with fixed hysteresis and the designed sliding parameter. Plots of the switching function, the hysteresis bands, C_A , C_B , the PWM counter and the control signal, u .

Figure 11. The top plot shows the sampled switching function, s_k , its predicted behaviour in a two samples horizon, $\hat{s}_{k+2}$, and the hysteresis value, h . In the mid plot, the PWM counter, PWM_c , and the PWM registers, C_A and C_B , are depicted. The PWM triggers the ADC acquisition at 1 MHz. When the ADC ends the conversion, the control sequence starts. Once

the computation of ((7) or (14)) is made, the prediction is obtained as (23) states.

$$\hat{s}_{k+2} = 3s_k - 2s_{k-1} \quad (23)$$

Subsequently, the control determines the PWM registers (C_A , C_B), which produces the desired behaviour of u , depending

on the cases:

$$\text{if } \hat{s}_{k+2} > h \rightarrow C_A = \frac{N(h - \hat{s}_{k+1})}{\hat{s}_{k+2} - s_{k+1}}, C_B = N + 1, \hat{u}_k = 1, \quad (24)$$

$$\text{if } -\hat{s}_{k+2} > h \rightarrow C_A = N + 1, C_B = \frac{N(h - \hat{s}_{k+1})}{\hat{s}_{k+2} - s_{k+1}}, \hat{u}_k = 0, \quad (25)$$

$$\text{else } \rightarrow C_A = (N + 1)(1 - \hat{u}_k), C_B = (N + 1)\hat{u}_k, \hat{u}_k = u_{k-1}. \quad (26)$$

where N is PWM_c counts and the signal $\hat{u}$ is an auxiliary control action defining the registers within the hysteresis band. Notice that $N + 1$ is only used to avoid a specific event as, for example, the activation of the reset when the signal has to remain at 1.

B. Exponential term

In general, the exponential operation is not an instruction included in the μC used for power converters control. Moreover, it is not easy to perform it analogously, since it requires complex circuitry. In this work, it was implemented with a lookup table, thus providing a fast execution time. An off-line generated table with the values of x_1^γ was stored in the μC memory. The measurement range of the ADC and the lookup table size have been designed for a specific ranges of input voltage, output voltage and load level. The resolution was of 17 mV, this being the maximum achievable, since the dimension of the lookup table (4095) matches the ADC ones.

VI. EXPERIMENTAL RESULTS

In the following subsections, different experiments tests are carried out to validate the controller design.

A. Line regulation and load regulation.

Table II presents the measured values of the output voltage when the converter operates with different loads for the designed TSMC and CSMC. As it can be seen in the table, the CSMC shows a very good load regulation of 0.2 %, which is even improved by the TSMC, thus achieving a perfect load regulation. Line regulation has been also tested for both controllers. The input voltage has been increased from 36 V to 48 V in steps of one volt. Figure 12 shows the measured values of the line regulation for the TSMC (left plot) and the CSMC (right plot). Both sets of measured indexes validate the good performance of the designed controllers, the one for the TSMC (with a maximum of line regulation of 0.29 %) being better than that of the CSMC (with a maximum of 0.46 %).

Table II
LOAD REGULATION

Load	TSMC Output voltage ¹	CSMC Output voltage ¹
No load	24 V	24.05 V
$R = 22\Omega$ (1.09 A)	24 V	24 V
$R = 10\Omega$ (2.4 A)	24 V	24 V
$R = 4.1\Omega$ (5.85 A)	24 V	23.95 V

¹ FLUKE 179 True RMS multimeter

B. Start-up.

Figure 13 shows the system start-up when the converter is loaded with 10 Ω for both the TSMC (on the left plot) and the CSMC (on the right plot). The plots present the behaviour of the output voltage, the capacitor current (with a scale factor of 70 mV/A), the switching function and the control signal. Notice that the maximum current in the start-up is around of 14 A, while the output voltage is properly regulated to the desired voltage (24 V). The measured settling time (finite convergence time) of the TSMC is 320 μs , as expected, much better than the 750 μs (considering a small error of 5 % around the steady-state value) measured in the CSMC test. Notice that there is a slight difference between the experimental maximum current and the theoretical one due to the hysteresis bandwidth of the comparator. This deviation can be amended in the design procedure. On the other hand, the right bottom plot of both oscilloscope captures confirms that a steady-state switching frequency of 100 kHz is achieved for both controllers. For comparison purposes the phase-plane oscilloscope capture is shown in Figure 14. Notice the different behaviour of the converter state variables in sliding (quasi-sliding) motion and how the experimental result fits with the simulation depicted in the Fig. 8.

C. Transient response for a load change.

Figure 15 shows the responses of the output voltage, the output current, the capacitor current (with a scale factor of 70 mV/A) and the switching function when the load suddenly changes from no load to 4.1 Ω (5.85 A at the output). The TSMC behaviour is presented on the left plot and the CSMC is shown on the right plot. In both cases, the desired output voltage (24 V) is recovered after a smooth transient response. Notice in the oscilloscope captures, how the TSMC reaches again the steady-state values in only 3 switching periods whereas the first order sliding motion of the CSMC can be observed in the output voltage transient.

VII. CONCLUSIONS

A comparative study of a CSMC and a TSMC is presented in this paper. The sliding mode controllers have been designed to regulate the output voltage and limit the start-up peak current in a synchronous buck converter. The analysis concludes that the TSMC shows faster transient response than the CSMC, because of its inherit finite time convergence property, and better line and load regulation indexes. Both controllers have been discretized and implemented in a microprocessor, and the experimental results obtained with a 150 W / 100 kHz power converter have confirmed the theoretical predictions. The study of an on-line adaptation of the TSMC parameters to control the convergence rate constitutes a further research subject of this work.

ACKNOWLEDGEMENTS

This work was partially supported by the Government of Spain through the *Agencia Estatal de Investigación* Project DPI2017-85404-P and by the *Generalitat de Catalunya* through the Project 2017 SGR 872. Authors would also like to thank the reviewers for their valuable suggestions.

Figure 12. Line regulation of the TSMC (left) and the CSMC (right).

Figure 13. Start-up of the TSMC (left) and the CSMC (right). v_c : green; i_c : blue; s_t or s : magenta; u : yellow.

Figure 14. Start-up phase plane of both the TSMC and the CSMC.

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Figure 15. Load change from no load to 4.1Ω for the TSMC (left) and the CSMC (right). v_c : green; i_c : blue; s_t or s : magenta; i_o : yellow.

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