FOCSI: A New Layout Regularity Metric

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Abstract

Digital CMOS Integrated Circuits (ICs) suffer from serious layout features printability issues associated to the lithography manufacturing process. Regular layout designs are emerging as alternative solutions to reduce these ICs systematic subwavelength lithography failures. However, there is no metric to evaluate and compare the layout regularity of those regular designs. In this paper we propose a new layout regularity metric called Fixed Origin Corner Square Inspection (FOCSI). FOCSI allows the comparison and quantification of designs in terms of regularity and for any given degree of granularity. When FOCSI is oriented to the evaluation of regularity while applying Lithography Enhancement Techniques, it comprehends layout layers measurements considering the optical interaction length and combines them to obtain the complete layout regularity measure. Examples are provided for 32-bit adders in the 90 nm technology node for the Standard Cell approach and for Via-Configurable Transistor Array regular designs. We show how layouts can be sorted accurately even if their degree of regularity is similar.

Keywords: Design For Manufacturability, Regular Designs, Deep Sub-Micron, CMOS, Digital ICs, Lithography Enhancement Techniques

1 Introduction

Yield loss in Integrated Circuits (ICs) can be decomposed into three factors: random, parametric and systematic yield loss [1]. Random yield loss is caused by defect-density related problems. Parametric yield loss occurs because the manufactured chip does not meet a design parameter, like frequency or power dissipation. Finally systematic yield loss, which is becoming the dominant yield loss factor [2], is related to subwavelength lithography failures. In this paper we focus on this last yield loss contributor from the point of view of layout design.

As we enter the Deep Sub-Micron era, optical lithography ICs manufacturing process needs new solutions to manufacture products at low cost [3, 4]. 193 nm Argon Fluoride light sources are still used for the technology nodes of 65 nm, 45 nm and probably 32 nm resulting in geometrical layout variability that leads to variations on the electrical characteristics of the devices and interconnections in ICs [5, 6]. Lithography enhancement techniques like Subresolution Assist Features (SRAF) or Optical Proximity Correction (OPC) improve layout patterns fidelity at the Rayleigh's optical resolution limit. Alternating Phase Shift Mask (AltPSM) and Off-Axis Illumination (OAI) can help go beyond this resolution limit. However, these techniques are computationally expensive and time consuming for huge ICs with arbitrary layout patterns [7, 8].

This issue is addressed by means of new Design For Manufacturability (DFM) techniques. In particular, regular layout designs with a reduced amount of layout patterns and with predictable layout neighborhood show to be highly beneficial. Regularity-based techniques like Via-Programmable Gate Arrays (VPGAs), Field-Programmable Gate Arrays (FPGAs), Structured ASICs (SAs) and Via-Configurable Transistor Array (VCTA) are emerging as a possible solution for manufacturers [9–15]. There is a trade-off that must be studied between area, delay, energy consumption and the regularity imposed. Usually regular techniques

offer worse area, delay and energy consumption than the Standard Cell approach but, according to the degree of regularity, they reduce cost and time associated to lithography enhancement techniques and therefore systematic yield loss. Area is measured directly from the layout design, and delay and energy consumption can be predicted by simulation. However, there is not a clear method to measure layout regularity.

From the layout designers point of view, the measure of the layout regularity of their designs can be a useful information to adjust and optimize in a comprehensive way the degree of layout regularity while considering the energy, delay and area trade-offs. This way designers can also compare a pair of layouts in terms of regularity. To the best of our knowledge, the only method that has already been used for this purpose is a visual comparison of a two-dimensional Fourier transform, which performs a spatial frequency analysis of the layout in order to find out the degree of layout patterns repetition [16]. However, it can lead to ambiguous comparisons if it is based only on the visual inspection of the resulting Fourier graph.

In this paper we propose a new layout regularity metric called FOCSI that associates a number to the layout instead of an entire function. FOCSI quantifies regularity allowing an accurate, deterministic and unambiguous comparison of layout designs. FOCSI is a parameterizable metric whose parameters are set depending on the specific application of regularity to be measured. There are multiple applications of FOCSI. As FOCSI evaluates layout regularity it can be used to predict systematic yield loss, that is reduced by a higher amount of regularity. FOCSI can also be used to estimate the time required to correct lithography issues by the means of lithography enhancement techniques that benefits from a reduced number of different areas to correct. Designers can also be interested on using FOCSI to evaluate the layout regularity impact on the initial yield and on the yield ramp over time of a particular fabric in a given technology node.

The structure of the paper is as follows. In section II we state the problem aborded, we provide a definition of regularity and we propose and formulate FOCSI layout regularity metric from the single layout layer to the complete layout. In section III we present the particular case study of FOCSI oriented to evaluate the benefits of layout regularity while applying lithography enhancement techniques and we briefly describe VCTA and Standard Cell layouts that we use for our regularity measurements. Finally, in section IV conclusions and future work are provided.

2 FOCSI Layout Regularity Metric

2.1 Problem Statement

As stated before, there is the need to develop a layout regularity metric that allows DFM ICs designers to compare in a deterministic and unambiguous manner any pair of layouts in terms of regularity. A metric is by definition a system of related measures that facilitates the quantification of some particular characteristic. In our case the characteristic to quantify is the amount of layout regularity. The metric function has to give to a layout a value indicating how much regular it is. Then, for any two layouts, it can determine which of them has higher regularity.

In [16] a two-dimensional Fourier transform has been used to compare the degree of regularity of a polysilicon layer of an SRAM array, logic implemented using standard cells and logic implemented using a regular fabric. Since a regular layout utilizing a small number of layout patterns is expected to have a finite number of frequency components the comparison is based on the number of frequency components obtained by the Fourier transform. By graphical inspection it can be seen that the SRAM and regular fabric layouts are more regular than the standard cells. However, the graphical inspection of the Fourier graphs does not give enough information to find out which of the two regular layouts is more regular than the other because the two frequency responses are similar.

The two-dimensional Fourier transform does not quantify regularity. It is a graphical representation giving an intuitive and qualitative measure of regularity. It can be used to compare regular versus non-regular layouts but it is difficult to use it to compare similar layouts in terms of regularity like for instance two layouts developed with DFM regular design techniques. That is why we propose FOCSI: a new layout regularity metric that allows a deterministic and unambiguous regularity comparison for any pair of layout designs. We show in next sections that our metric can determine which of the layouts under study is more regular even if they have similar degrees of regularity.

2.2 Layout Regularity Definition

We define layout regularity as the property of a layout to be generated by a reduced number of layout areas of a given shape and size (e.g., squares of 160 nm x 160 nm). Therefore, the lower is the number of different layout areas that can be found in a layout the higher the regularity is. The maximum regularity will be achieved when a single layout area can be used to

generate the whole layout by repeating itself along all the layout. On the other hand, the minimum regularity will occur when all areas in the layout are unique, and therefore, there is no repetition at all.

Regularity can be studied at different granularities depending on the size considered for layout areas inspected. On one hand, the smallest layout area that can be considered is defined by the manufacturing grid (5 nm for the 90 nm technology used in this work) so that the layout area considered will be a square with this manufacturing grid as both dimensions. Possible layout areas are in this case binary. We can only find in the layout two different areas: one containing the material of the layer inspected and the other containing nothing. Therefore all layouts inspected will have the same regularity and that is why we are not interested in using this extreme. On the other hand, the highest layout area that can be considered is the complete layout area. Again, all layouts will present the same regularity being generated by a single layout area. Thus, regularity must be evaluated using layout areas between these two extremes. In particular we propose the use of square areas and the size of these square areas will depend on the application of the regularity evaluation.

2.3 Metrics Studied Before FOCSI

In order to explore the layout to find out the number of square area generators, our first approach was to divide the complete layout in squares multiple of the manufacturing grid (e.g., square size of 32 x 5 nm = 160 nm) and then to compare one to each other noting the number of different ones. However this option was inadequate because even if the layout was composed by only one layout pattern, low repetition and a high number of generators were observed, and thus very low regularity. Figure 1 shows how regularity is not captured by using this method because all the area squares are different while the visual inspection of the layout shows an important degree of regularity.

The first modification to capture the amount of regularity was to allow two squares to be noted as the same generator even if they have a given fraction of the area different, being such fraction a threshold to be chosen (e.g., 5%). This way squares like the first and the third one of the upper row in Figure 1 were considered equal. However this threshold also led to mistakes. Since irregular layouts sometimes have a low number of polygons in some layout layers, depending on the threshold considered, some really different square areas were considered equal and thus the resulting regularity was higher than expected. The real problem was to find the way to align the square areas and the material polygons in the layout.

2.4 FOCSI Proposal

The Fixed Origin Corner Square Inspection (FOCSI) proposal arises from the previous observations. FOCSI first explores the layout in order to detect all upper left shape corners and then considers these corners as the origins of the square areas to be compared. In that way FOCSI ensures that regularity is captured because squares are aligned to layout patterns. Figure 2 depicts how FOCSI works for the same example shown before. In this case, types 1 and 2 of squares layout areas can be detected. Note that in this figure different square sizes are also illustrated with red and blue squares. Once the corners are fixed, various sizings can be applied to squares in order to evaluate different granularities of regularity. For small sizings it can happen that all layout shapes are not fully inspected, however, by upsizing the square dimensions we ensure that the whole layout is considered. In fact FOCSI is shape oriented as it inspects at least one layout area for each of the shapes present in the layout.

Regarding the implementation of our FOCSI proposal, to be able to explore layouts in the way described and to compare the different square areas to each other, we transform layout geometry shapes into square samples of the minimum resolution allowed by the technology node design kit. In our case we use a 90 nm design kit with 5 nm manufacturing grid. The codification used assigns a 0 value when the 5 nm per 5 nm square layout is empty and a 1 value to represent the layer material (e.g., polysilicon, oxyde diffusion). The whole layout layer is therefore codified as a matrix of 0's and 1's. To obtain this matrix we import our layouts in the EDIF textual format and transform the syntax used by EDIF into the 0 and 1 samples for the layout layer un-

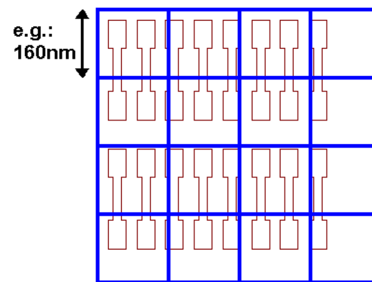

Figure 1. First approach to measure regularity: divide the whole layout in contiguous squares.

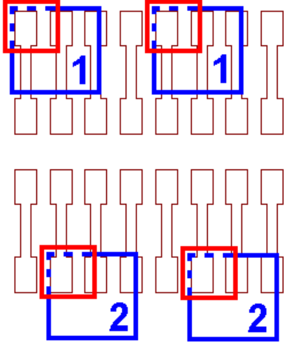

Figure 2. FOCSI methodology.

der study. Then, we find all upper left shape corners from where square areas are defined. Finally, these squares are compared sample by sample against each other square area in order to calculate the number of different generators the layout layer has. Two layout areas are considered identical only if all their samples are identical. The result of this step of FOCSI metric is the number of different generators needed for the layout layer under study (R_{layer}) and for the different square area sizings. Therefore the lower R_{layer} is the higher regularity is.

2.5 Single Layout Layer FOCSI Measurements

For a single layout layer like polysilicon or metal 1, FOCSI provides different measurements depending on the square layout area sizings considered. These measurements represent the different regularities spanning from micro to macro-regularity [16]. A layout can be defined as micro-regular if it has a reduced number of layout patterns generators, where a pattern occupies a small area in the layout, for instance a few polysilicon polygons if we are measuring the polysilicon layer (160 nm sizing in our examples for the 90 nm technology node). On the other hand a layout can be defined as macro-regular if few patterns exist at coarse granularity (e.g., considering squares whose geometry is similar to that of one or few standard cells).

As stated before, the granularity to be used will depend on the particular application of FOCSI.

2.6 Complete Layout FOCSI Formulation

The final step that has to be done to obtain a comprehensive complete layout regularity value (R_{layout}) is to combine all different layout layers regularity values (R_{layer}) calculated. Defining M as the number of layout layers considered, we propose to combine these M measurements assigning weights to each one of them. In general, the layout regularity R_{layout} can be then parameterized as follows:

$$R_{layout} = \sum_{j=1}^{M} \beta_j . R_{layerj} \tag{1}$$

where β_j are layout layers weights and R_{layerj} are the regularities measured for the M layout layers considered. In order to enable the comparison of the R_{layout} measures from different layouts the β_j parameters must also fullfill the following property:

$$\sum_{j=1}^{M} \beta_j = 1 \tag{2}$$

Again depending on the FOCSI application each of the M layer regularities will have a different β_j weight. R_{layout} can be considered as the final FOCSI metric result. As for R_{layer}, the lower R_{layout} is the higher regularity is. Note that this final R_{layout} is not needed if the objective is the evaluation of a particular layer regularity at a concrete square sizing. FOCSI can be adapted to measure regularity at different layers and granularities. We have presented the broadest definition of FOCSI in order to illustrate the possibilities offered by our metric.

3 Case Study: FOCSI Oriented to Lithography Enhancement Techniques

3.1 FOCSI Square Sizing and Optical Interaction Length

Lithography enhancement techniques correct subwavelength lithography failures taking into account a given layout area determined by the photolithography system used to manufacture the design. The corrected features need to be considered with their layout neighborhoods to obtain satisfactory results. Neighborhoods are bounded by the optical interaction length defined as the range of distance in which layout features have a non-negligible effect one on the other [17]. For our regularity measurements oriented to lithography enhancement techniques square sizing will be, therefore, also bounded by this optical interaction length. It makes no sense to consider layout regularity of areas higher than the ones defined by the optical interaction length because the regularity measured at this level will not

affect the lithography enhancement techniques. Therefore, the concrete sizing of squares for the R_{layer} measurement is defined by the optical interaction length of the manufacturing process.

According to [16] the optical interaction length is from 2 to 6 times the light source wavelength. [18] defines the radius of influence of lithography as 5 times the minimum technology feature size. In [17] it is approximately 600 nm for a 193 nm wavelength illumination source. Finally in [19] we have found that it is 500 nm for the 65 nm technology node. Therefore, in the 90 nm technology node, with a 193 nm illumination source, the optical interaction length has a value between 386 nm and 1158 nm. In our examples we use a maximum radius of influence of approximately 1000 nm that translates into a maximum square sizing of approximately 2000 nm for FOCSI.

In particular, we show regularity measurements for 160 nm, 320 nm, 640 nm, 1280 nm and 2560 nm square sizes in order to see the evolution of regularity of the designs under study for the whole range defined by the optical interaction length. The concrete R_{layer} that we will use to calculate R_{layout} for FOCSI oriented to lithography enhancement techniques is the measure for 2560 nm, that covers our maximum optical interaction length. The 160 nm minimum square size is chosen to ensure that at least 1 or 2 material polygons are present in the area considered to be able to measure micro-regularity.

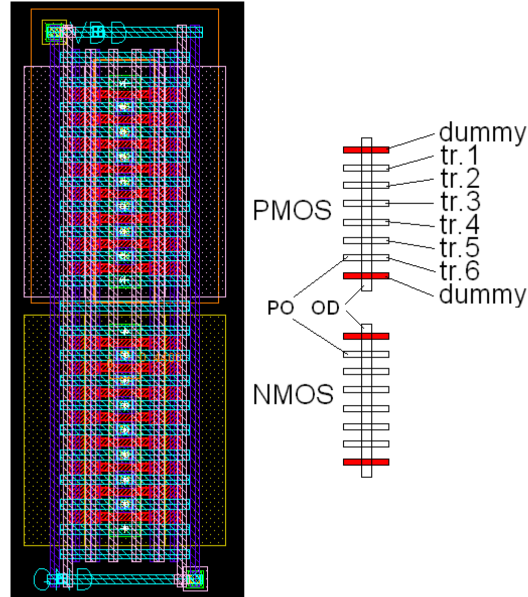

Figure 3. VCTA basic cell [15].

3.2 VCTA and Standard Cell Layouts under Study

3.2.1 Standard Cell Layouts

Standard Cell designs are based on the reuse of logical function layout cells (e.g, AND cell, OR cell) to implement the desired circuit. These layout cells have fixed height bounded by the power supplies. However they can have different widths and depending on the function implemented they can include transistors and interconnects in very dissimilar configurations. Moreover, Standard Cell libraries can include more than 1000 different cells, and therefore a huge number of placing and routing configurations are possible. Resulting Standard Cell layouts are therefore expected to have a low degree of regularity.

3.2.2 VCTA Layouts

Via-Configurable Transistor Array (VCTA) is a regular layout design technique based on a single basic cell (Figure 3). VCTA reduces process variations in silicon and metal as much as possible at manufacturing time pushing to the limit circuit layout regularity for devices and also for interconnects in order to maximize regularity benefits.

VCTA is a very fine-grain device regular structure, similar to a Sea-of-Transistors [20–22] including a Transistor Array. In order to ensure interconnect regularity and to reduce routability problems due to prefabricated contacts or vias, VCTA is a Via-Configurable structure where all contacts and vias can be configured depending on the function synthesized. On one hand, regarding the intra-cell routing, all the routing channels and the MOS devices are implemented inside the VCTA basic cell but only connected depending on the needs. On the other hand, the inter-cell routing between VCTA basic cells is also configurable, in this case without using contacts or vias but by the extension of the metal lines in the frontiers of the VCTA basic cells. In fact, contacts, vias and these inter-cell metal interconnections are the only source of layout irregularity of the VCTA design. Further details on VCTA can be found in [15].

3.2.3 Adders Layout Generation

IC chips typically consists of three types of cells: I/O cells, mega cells (memory or micro-controllers, etc.), and standard cells (AND gates, OR gates, and flip-flops, etc.) [23]. As one of the core blocks are standard cells we will focus on combinational logic circuits like binary adders to illustrate our regularity metric.

In particular, we have developed complete layouts in the 90 nm technology node for a 32-bit Carry-Ripple adder (CR32) and for a 32-bit Carry-Lookahead adder (CLA32) using the VCTA structure and also the Standard Cell approach (STD).

Our adder designs Bitwise PG Logic, Group PG Logic and Sum Logic require 6 different types of logic functions: an inverter, a XOR, a 2-input NAND, a 4-input NAND, a AND-OR and a OR-AND [24].

For the STD layout generation, we have used the public standard cell layouts provided in [25] that offers a complete set of portable CMOS libraries that has been used for research projects such as the 875,000 transistors StaCS superscalar microprocessor and 400,000 transistors IEEE Gigabit HSL Router.

For the VCTA layout generation the same logic gates have been used, mapped inside the VCTA basic cells.

3.3 Single Layout Layers FOCSI Results

Table 1 shows the results obtained for polysilicon (PO), oxide diffusion (OD) and metal 1 (M1) layout layers for the different granularities of regularity and for CR32 and CLA32 STD and VCTA layouts. Figures 4, 5, 6 and 7 depict captures of regions of the different layout layers for both CR32 and CLA32 implemented using STD and VCTA designs. We have chosen these three layout layers because they are the most representative of the front-end and back-end process. On one hand PO and OD define the transistor active areas, and the polysilicon gate critical dimension variation have a tremendous impact on the timing and energy consumption of digital ICs. On the other hand M1 layer is representative of the interconnect structure.

We obtain that for all layers and both adders, VCTA designs are more regular than STD because a lower number of generators are found. This result can be graphycally supported by the inspection of the layout layers captures. Note also that the difference in regularity between VCTA and STD increases with square size. For instance, if we compare the polysilicon layer of the CLA32 adder for 160 nm and 2560 nm square sizes, we observe that regularity ratio grows from 4X (4 vs 1) to almost 25X (99 vs 4). Micro-regularities considering very few patterns are comparable but macro-regularities are very distant because VCTA layouts are based on a single basic cell in front of a set of different cells for STD.

VCTA CR32 and CLA32 adder results show that PO and OD layers have the same number of generators and thus the same regularity. As shown in Figures 5 and 7 these layout layers are identical. However, M1 layers differ and that is why regularities are slightly different

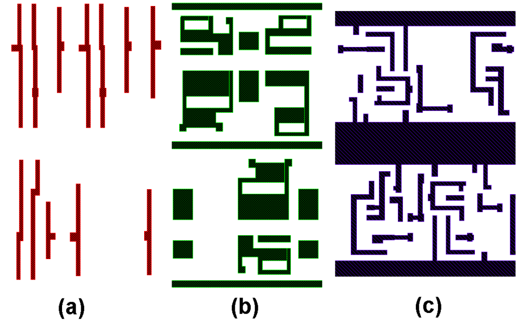

Figure 4. STD CR32 Layout Layer Captures (a) PO (b) OD (c) M1.

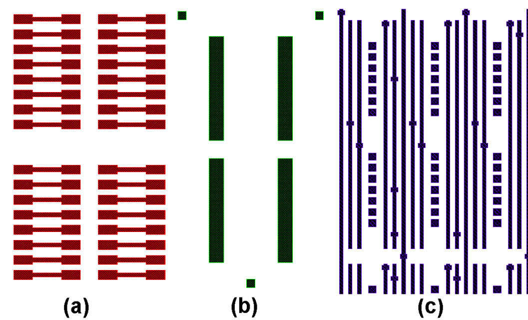

Figure 5. VCTA CR32 Layout Layer Captures (a) PO (b) OD (c) M1.

too. This is due to the Via-Configurable structure that involves M1 and not PO nor OD.

STD CR32 and CLA32 adder results show that STD CLA32 is more regular for OD and M1 layers, and that STD CR32 is more regular for PO layer. However, both adders are highly irregular. In fact, since STD layouts use different cells and routing configurations, elevate number of generators are detected.

For the complete layer regularity (R_{layer}), layouts developed with VCTA design technique are clearly more regular than the STD ones because we need fewer number of generators in all cases and for all layers. Using the two-dimensional Fourier transform confirms this result for instance for the PO layer when comparing VCTA and STD CR32 (Figures 8 and 9). We can see how the STD CR32 spatial analysis has more representative frequential components. In those comparisons where one layout is regular and the other one is not, both the two-dimensional Fourier transform and FOCSI can be used to identify the most regular layout.

However, when comparing layouts with a similar de-

Table 1. Adders Layout Regularity results for PO, OD and M1 layers

	PO generators				OD generators				M1 generators			
	CR32		CLA32		CR32		CLA32		CR32		CLA32	
Square Size	STD	VCTA	STD	VCTA	STD	VCTA	STD	VCTA	STD	VCTA	STD	VCTA
160 nm (micro)	3	1	4	1	2	1	1	1	13	3	5	3
320 nm	7	1	10	1	4	2	4	2	38	5	24	7
640 nm	22	2	19	2	15	2	7	2	100	7	70	16
1280 nm	87	3	44	3	61	2	22	2	286	17	124	36
2560 nm (R_{layer} - macro)	276	4	99	4	229	3	75	3	603	26	225	77

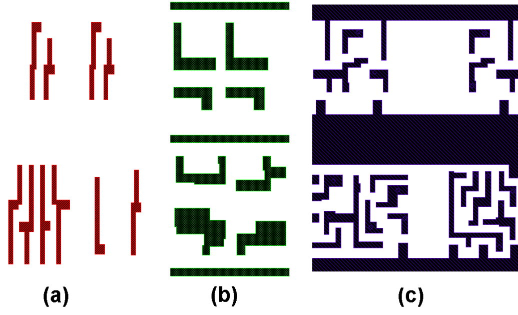

Figure 6. STD CLA32 Layout Layer Captures (a) PO (b) OD (c) M1.

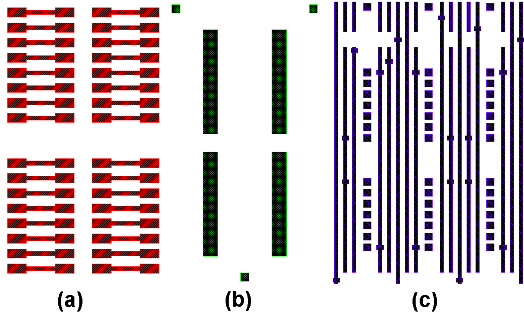

Figure 7. VCTA CLA32 Layout Layer Captures (a) PO (b) OD (c) M1.

gree of regularity the two-dimensional Fourier transform is ambiguous. For instance, if we compare the M1 layer for VCTA CR32 and CLA32 (Figures 10 and 11), we obtain Fourier graphs that look almost the same but with our metric, we can see that VCTA CR32 is more regular than VCTA CLA32. In fact, since the same VCTA basic cell is used for both designs, regularity is similar but M1 routings are not exactly the same. For CR32, inter-cell routing is repeated along all cells because its structure is the connection of 32 1-bit full adders. However, for CLA32 slightly different connections are required because of the carry calculation in groups of 4 bits. The difference can be seen comparing the layout captures presented for both designs (see 5 (c) and 7 (c)). Therefore, in this case, our metric is able to compare two layouts with similar

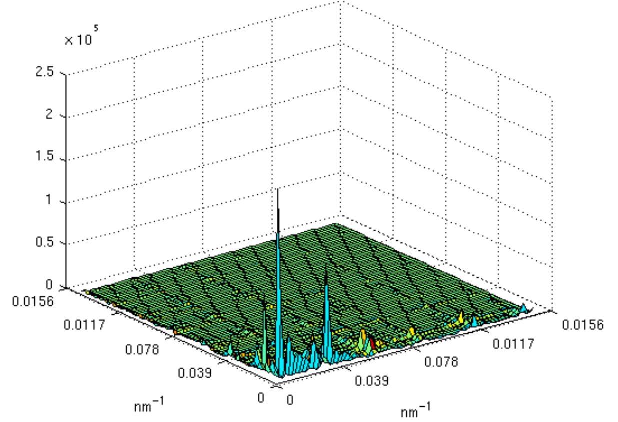

Figure 8. VCTA CR32 polysilicon layer spatial frequency analysis.

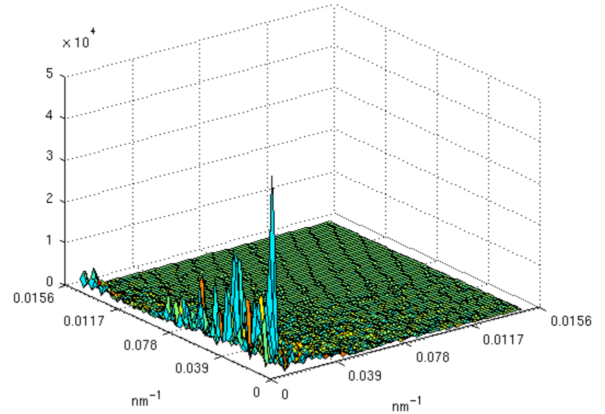

Figure 9. STD CR32 polysilicon layer spatial frequency analysis.

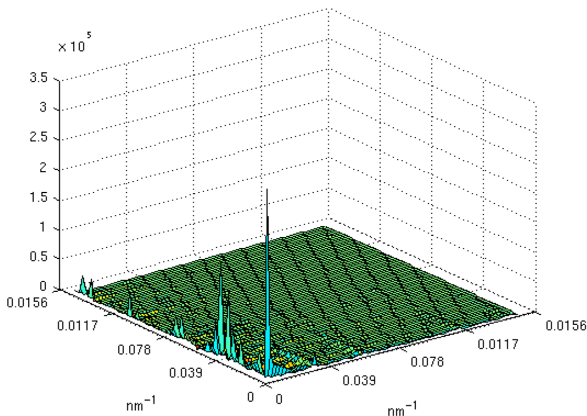

Figure 10. VCTA CR32 metal 1 layer spatial frequency analysis.

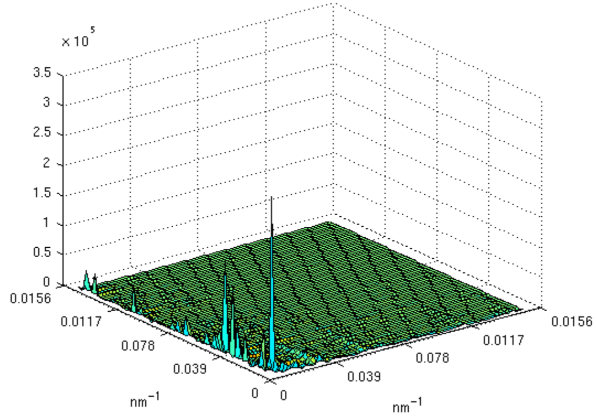

Figure 11. VCTA CLA32 metal 1 layer spatial frequency analysis.

regularities while the graphical inspection of the two-dimensional Fourier transform cannot. Note that M1 layer is the VCTA layer that is less regular because M1 is involved in inter-cell and also intra-cell routing that are the source of irregularity of the VCTA design technique.

3.4 Complete Layout FOCSI Results

For FOCSI oriented to lithography enhancement techniques the different β_j weights depend on the process conditions in what refers to layer manufacturability criticality. Using test structures for process control to monitor and control the fabrication line, manufacturers can know which of the layout layers is the most affected by systematic subwavelength lithography based failures. Provided that these results have statistical significance, these data can be used to select the weights. Simulations of the fabrication process can also be performed taking into account different lithography enhancement techniques. For instance, if the manufacturing process is weak on M1 layer, the highest weight will be for the M1 regularity. Usually, PO layer is the most critical, because the smallest features are printed on it, like critical gate dimension.

To illustrate our regularity metric proposal (see Table 2) we present the calculation of the complete layout regularity (R_{layout}) for the adders studied in previous subsection for PO, OD and M1 layers (M = 3). Considering that the manufacturing process is PO limited we have used 45%, 30% and 25% weights for PO, OD and M1 layers respectively. The case where OD is the most critical layer has been calculated using 30%, 45% and 25% weights. Finally, the case where M1 is the most critical layer uses 30%, 25% and 45% weights. Different results are obtained in each case, with small variations because only 3 layers are considered, however, as expected, VCTA designs are more regular than STD ones with all these particular calculations and using these 3 layout layers. As shown in Table 2, the regularity ratio between STD and VCTA designs decreases when M1 is the most limiting layer because VCTA is more irregular in this layer than in the other ones. The complete layout regularity value will be obtained by combining all of the layout layers involved in the designs and with more precise weighting values from the manufacturing process.

Table 2. Complete Adders Layout Regularity results

	CR32 R_{layout}		CLA32 R_{layout}	
	STD	VCTA	STD	VCTA
PO limited	343.65	9.20	123.30	21.95
OD limited	336.60	9.05	119.70	21.80
M1 limited	411.40	13.65	149.70	36.60

4 Conclusion and Future Work

FOCSI layout regularity metric is a new tool that can be parameterized by designers to evaluate the different impact that regularity has on specific applications. Moreover FOCSI can calculate the layout regularity in the degree of granularity desired quantifying and weigthing the number of layout generators. For

instance, FOCSI can be applied to study the regularity trade-off originated with the appearance of new regularity-based layout Design For Manufacturability techniques. It can be also used to study the impact of layout regularity while applying lithography enhancement techniques. In this last case study, we have shown that FOCSI provides an accurate comparison of layouts layers even if their regularity is similar.

Results for CR32 and CLA32 adders developed with the STD approach have been compared to the same adders developed with the regular VCTA design technique showing that FOCSI captures the higher regularity of the VCTA.

Future work will be to relate our new FOCSI layout regularity metric to other possible applications like a new systematic yield loss metric in order to evaluate how much regularity helps on reducing subwavelength lithography failures, or how regularity can impact the initial fabrication yield or the yield ramp over designs lifetime.

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