Fixed-switching frequency interleaved sliding mode 8-phase synchronous buck converter

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Abstract

This paper describes the design of an interleaved sliding mode control for a multiphase synchronous buck converter, which inherits the properties of the sliding mode control, operates with fixed switching frequency at steady-state and ensures current equalization among the phases. Moreover, a power management algorithm is added in order to decide the number of active phases as function of the power load demand, thus optimizing the converter efficiency. The systems uses a Master-Slave structure where each phase can actuate as the Master one in such a way that the overall system reliability is improved. Experimental results in a 1.5 kW 8-phase synchronous buck converter show that interleaving operation, robust output voltage regulation, phase current equalization, switching frequency regulation and power management are achieved.

Index Terms

sliding mode control, interleaving, fixed switching frequency, chattering reduction, current equalization, power management

I. INTRODUCTION

Interleaving is a common way of managing the power transistors in order to reduce the load current ripple in multiphase buck converters [1]–[9]. The multiphase structures were initially proposed for the DC/DC voltage regulator modules (VRM) [10], [11], used in integrated circuits and microprocessor power supplies. These applications require low voltage and high current, which restricts the use of single-phase converters. Lately, these structures have been applied as battery chargers [12], DC bus regulators [13] or in power line communications [14], among others.

The interleaving operation allows to cancel the current ripple through the output capacitor, which entails a reduction of the value, size, weight and cost of this component. Since the

current ripple is cancelled in the parallel connection, the reduction of the inductor values, size and cost, are also possible. Another advantage of the multiphase structure is the reduction of the components stress, due to the decrease of the power processed by each phase. Such reduction would allow to increase the switching frequency, which in turn, would lead to an additional reduction of the reactive components. Therefore, thanks to an interleaving operation, the designed multiphase converter can be smaller, lighter, cheaper and more efficient than the single-phase converter managing the same power. In ideal conditions, the different phases manage the same amount of power. However, structural differences among the phases, which can occur due to the component tolerances, tend to unbalance the power flowing by the phases. As the phases are designed maximizing the efficiency for a nominal power, the overall efficiency is decreased when the power flow is not equalized. To overcome this drawback, modular systems usually employ current equalization algorithms that ensure power sharing among phases [15]–[18]. In addition, the connection or disconnection of phases permit to optimize the converter performance. Depending on the desired feature to optimize, such as efficiency, reliability or transient response, different connection-disconnection rules should be derived [19]–[21].

Interleaving is typically implemented by Pulse Width Modulation (PWM) [5], [6], [15]. The controller, which regulates the converter output voltage, is usually designed from a small signal averaged model of the converter using linear control tools. Due to the small signal model usage, the system responses are degraded with parametric variations, as the modifications of the converter active phases. In order to get fast transient response, some authors have proposed hysteretic controllers for the multiphase converter [22], [23]. In [22] the interleaving operation is guaranteed by using fixed band hysteresis comparators and a digital circuitry, being the phases switching frequency variable. Fixed switching frequency and interleaving operation is achieved by synchronizing the duty cycle with an external fixed frequency clock reference in [23]. Nevertheless, this approach requires an external reference clock and a bandwidth changing loop for each converter phase.

Sliding mode control (SMC) stands out for its robustness with respect to parametric variations and external disturbances. It has been successfully applied in power electronics in [24], [25], among others. In 2009, Lee, Malinin and Utkin presented in [26] a technique which minimizes the ripple in a sliding mode voltage controlled multiphase converter, with an interleaving sliding mode. The proposed control method replaces the standard PWM interleaving approach of a multiphase converter. That technique was successfully implemented in a low power 4-

phase converter in [27], where a equalization algorithm was proposed in order to balance the power flowing through the phases. However, the SMC was implemented by means of hysteresis comparators and the switching frequency became variable and, hence, sensitive to the power converter parameters and the input voltage. Such variations complicate the reactive components design, since they are generally designed for a constant switching frequency. Furthermore, as the switching frequency harmonic content is not fixed, the output voltage filtering capability is degraded.

The work presented here follows the sliding mode control design procedure of [26] and [27]. The designed controller is applied to a 1.5 kW 8-phase synchronous buck converter, ensuring interleaving, current equalization among phases and robust output voltage regulation. Moreover, a power management algorithm deals with connect or disconnect phases depending on the delivered power to the load is included to improve the efficiency of the converter. Besides, in order to regulate the switching frequency of the phases, a switching frequency controller is designed following the procedure proposed in [28]. Such methodology does not require any synchronization clock signal and it is only applied to one of the converter phases.

The remainder of the paper is organized as follows. In Section II the dynamical model of the power converter is introduced. The description of the proposed controllers are presented in Section III. Section IV presents the developed prototype for experimental evaluation, followed by the experimental results of the converter in Section V. In the last section, the conclusions derived from this research are stated.

II. MULTIPHASE SYNCHRONOUS BUCK CONVERTER DESCRIPTION

A multiphase step-down power converter is composed by several synchronous DC/DC buck converters with a common output capacitor. As it is shown in figure 1, a m-phase converter supplies a single load assumed to be resistive and linear in this communication and can be modelled by the following set of differential equations:

$$\begin{aligned} L\frac{di_k}{dt} &= -r_{Lk}\ i_k - v_c + E\ u_k; \quad k = 1, .., m \\ C\frac{dv_c}{dt} &= \sum_{k=1}^{m} i_k - \frac{v_c}{R} \end{aligned} \tag{1}$$

where i_k is the current flowing through the k-phase, v_c is the output voltage and u_k is the k-phase control input which takes values in the set $\{0, 1\}$. The phase inductances (L_k) are assumed

to be identical and r_{Lk} denotes the unmatched resistive losses of the phases. The input voltage (E) has been considered common to all phases.

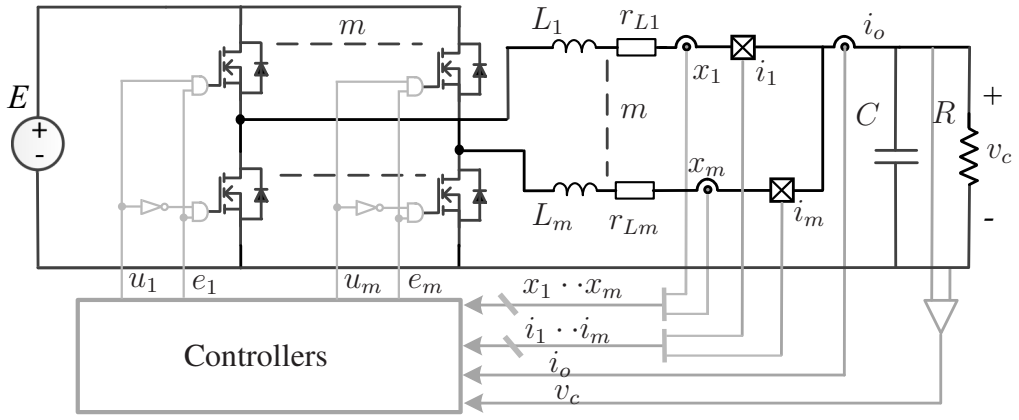


Fig. 1. m-phase synchronous buck converter circuit scheme.

Figure 1 also depicts the equivalent scheme of the switches drivers and the sensing elements. Each phase includes a driver that generates the control signals for the power switches, and allows to inhibit the corresponding leg with the enable signals $e_1 \cdots e_m$. The figure also shows the sensors used by the controllers. Both load current (i_o) and output voltage (v_c) are measured by the control system. Additionally, each phase uses two current sensors, a low cost current transformer ($x_1 \cdots x_m$ signals) and a Hall Effect one ($i_1 \cdots i_m$ signals). Using the current transformers and the Hall Effect sensor instead of shunt resistors preserves a good converter efficiency, keeping the capability of high frequency current measurement and improving the signal to noise ratio. Strictly speaking, the system could work with just two sensors: a current transformer (the one corresponding to the Master phase), and the output voltage sensor. A desired rotatory Master phase implies to add sensors in all the phases. Furthermore, the equalization algorithm requires the inclusion of Hall Effect currents sensors in each phase in order to measure their average current values.

III. CONTROL STRUCTURE

This work follows the design rules presented in [26], [29] but increases the number of the converter phases, regulates the steady-state switching frequency to a desired value and upgrades the controller with a Power Management Algorithm (PMA) able to select the number of enabled phases in order to maximize the efficiency. The control scheme is depicted in figure 2, uses

a Master-Slave control strategy and can be divided in several parts that are described in the following subsections.

A. Output Voltage Sliding Mode Control.

The voltage regulation is performed by the Master phase with the following switching surface:

$$\sigma_M := \psi_1 \left(v_c - v_c^*\right) + \psi_2 x_M = 0 \tag{2}$$

where v_c^* is the desired output voltage, $\psi_1, \psi_2 > 0$ are the switching surface parameters. As it can be seen in the figure 2, the variable x_M corresponds to the current transformer output of the phase that the PMA selects as the Master one.

Taking into account the magnetic coupling equations and knowing that the secondary of the transformer is loaded with a resistor R_b, the equation that relates the output variable x_M, which is the voltage through R_b, and the current flowing by the transformer primary side is given by:

$$L_x \frac{dx_M}{dt} = -R_b x_M + R_b M \frac{di_M}{dt}; \tag{3}$$

where i_M is the Master phase current and M and L_x are the mutual inductance and the secondary inductance, respectively.

Assuming identical phases and using the equivalent control method [24], which entails $\sigma_M = 0$ and $\dot{\sigma}_M = 0$, the ideal sliding dynamics is analysed. The equivalent control for the Master phase is:

$$u_{M_{eq}} = \frac{v_c}{E} + \frac{r_{L_M}}{E} i_M + \frac{L\psi_1}{EM\psi_2}(v_c^* - v_c) - \frac{\alpha L}{E}\dot{v}_c \tag{4}$$

where $\alpha = \frac{\psi_1 L_x}{\psi_2 R_b M}$. The sliding dynamics for the output voltage is:

$$C\frac{d^2 v_c}{dt^2} + \left[m\alpha + \frac{1}{R}\right]\frac{dv_c}{dt} + \frac{m\psi_1}{M\psi_2} v_c = \frac{m\psi_1}{M\psi_2} v_c^* \tag{5}$$

and for the currents flowing through the phases:

$$\frac{di_k}{dt} = v_c\left(\frac{\alpha}{RC}\right) + \frac{\psi_1}{M\psi_2}\left(v_c^* - v_c\right) - i_k \frac{\alpha\, m}{C} \quad k = 1, .., m. \tag{6}$$

Since all the coefficients of (5) and (6) are positive, the differential equations are asymptotically stable and the output voltage converges to the reference one at the steady-state. The control law that enforces sliding motion in $\sigma_M = 0$ is $u_M = 0.5\left[1 + sign\left(\sigma_M\right)\right]$.

Remark 1: The current ripple cancellation at the output capacitor produced by the interleaving operation, disable the possibility to use this current as the first time derivative of the output voltage in the Master switching surface (2). As a consequence, the inductors currents are measured employing current transformers.

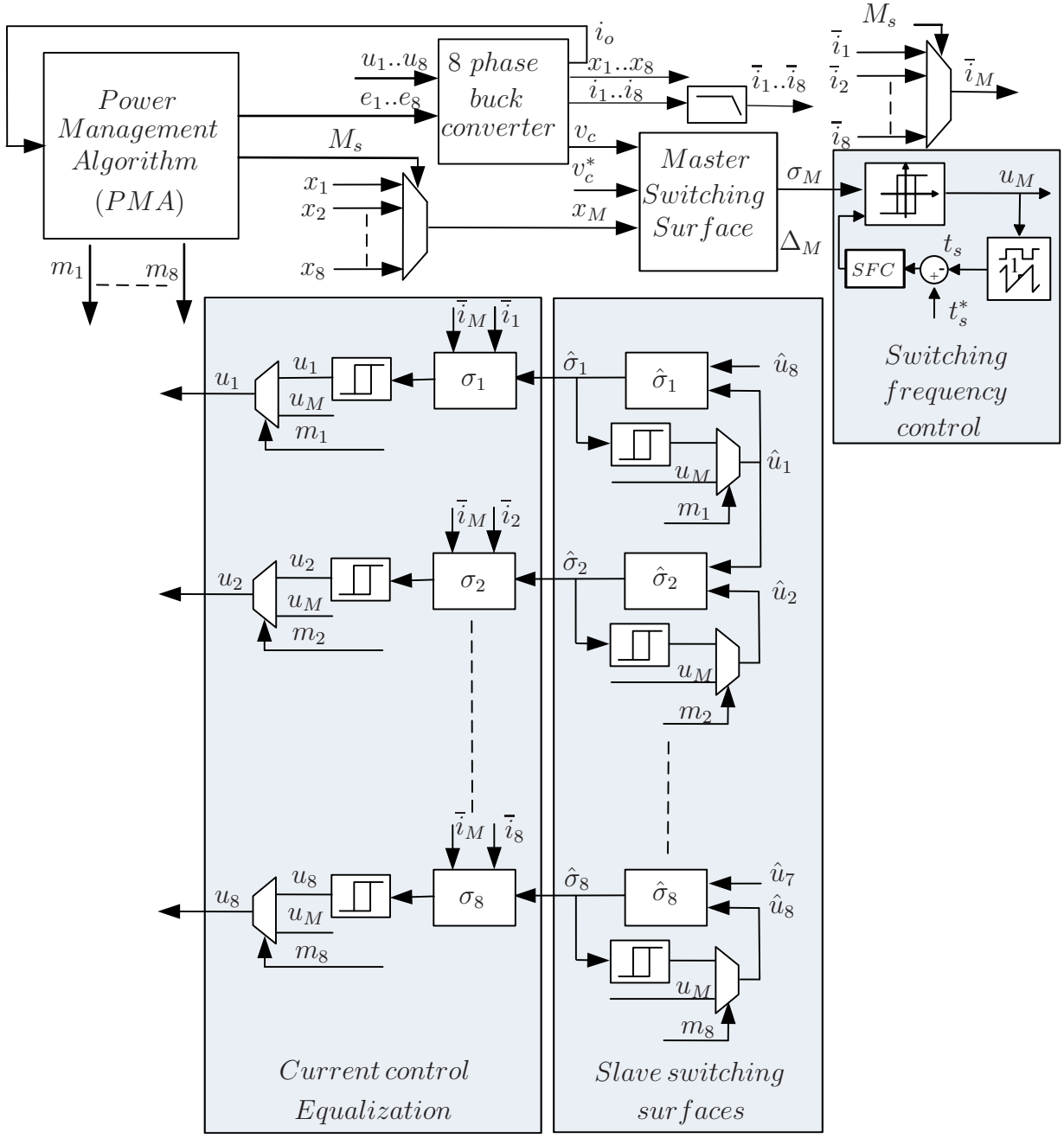


Fig. 2. 8-phase synchronous buck converter control scheme.

B. Interleaved Sliding Mode.

Assuming that the Master phase corresponds with the k-th phase, the interleaved sliding mode operation (proper phase shift among phases) is achieved by using the Master phase control signal, $u_k = u_M$, and the $(m-1)$ Slaves switching surfaces defined as follows:

$$\begin{gathered}
\hat{\sigma}_{k+1} := K \int (u_M - \hat{u}_{k+1})\, dt = 0 \\
\cdot \\
\cdot \\
\hat{\sigma}_m := K \int (\hat{u}_{m-1} - \hat{u}_m)\, dt = 0 \\
\hat{\sigma}_1 := K \int (\hat{u}_m - \hat{u}_1)\, dt = 0 \\
\cdot \\
\cdot \\
\hat{\sigma}_{k-1} := K \int (\hat{u}_{k-2} - \hat{u}_{k-1})\, dt = 0
\end{gathered} \tag{7}$$

being $\hat{u}_i = 0.5\,[1 + sign\,(\hat{\sigma}_i)]$ the control laws.

The proposed switching surfaces in (7) enforce the equalitzation of the average values of $u_{k_{eq}}$ and $u_{M_{eq}}$ under sliding motion. Additionally, the hysteretic control law $\hat{u}_i = 0.5\,[1 + sign\,(\hat{\sigma}_i + \Delta\hat{u}_i)]$ generates a phase shift among the phases, being Δ the hysteresis width of the comparator. The works [26] and [27] prove that this phase shift is given by $T_\phi = \Delta/K$. Obviously, the desired phase shift, $T_\phi = t_s/n$, depends on the switching period and the number of active phases. By equalling both expressions of T_ϕ, the value of K can be obtained as: $K = (\Delta n)\,/t_s$. Since the number of active phases, n, can vary according to the PMA algorithm decisions, the phase shift is adjusted on-line through K, measuring the Master phase switching period t_s.

C. Current Equalization Algorithm.

From an implementation point of view, it is difficult to obtain a set of identical phases. It can be proven that, when phases have different losses, the quiescent working point of a multiphase converter is given by

$$v_c = v_c^*; \quad i_k = \frac{r_{L1}}{r_{Lk}} \left[1 + \sum_{i=2}^{m} \frac{r_{L1}}{r_{Li}} \right]^{-1} \frac{v_c^*}{R}; \quad k = 1, .., m \tag{8}$$

where $r_{L1}, ., r_{Lm}$ are the resistive losses of the phases which include the series resistance of the inductors and the conduction resistance of the mosfets. Therefore the average currents through

the phases are different. Notice that the equilibrium is very sensitive to resistive losses and the phase currents are affected with the same ratio than the resistive losses as

$$\frac{i_k}{i_1} = \frac{r_{l1}}{r_{lk}}$$

To overcome this drawback, a current equalization algorithm has been designed.

The equalization is achieved employing a new set of switching surfaces for the Slaves phases, defined as σ_k, which uses $\hat{\sigma}_k$ as an input. The surface σ_k copies the control signal generated by $\hat{\sigma}_k$, $\hat{u}_k$, increasing or decreasing the effective duty cycle of u_k such that the average current error $(\overline{i_M} - \overline{i_k})$ converges to zero, being $\overline{i_M}$ and $\overline{i_k}$ the average values of the respective currents. In [27] it can be found a deeper explanation of the applied equalization method.

D. Switching Frequency Regulation.

The SMC implementation with fixed hysteresis band comparators instead of sign functions yields an inherently variable switching frequency. In order to regulate the switching frequency, this work follows the control scheme proposed in [28]. The technique adds a new loop which measures the switching period, in this application the Master phase, updates the hysteresis band value using a switching frequency controller (SFC), and enforces the measured switching period t_s to converge to a reference one t_s^*. For the multiphase configuration, the switching frequency regulation is just required for the Master phase, since the Slaves phases automatically replicate the Master one due to the interleaving operation. In this paper, an approach based on a continuous time integral action for the SFC is employed. The additional loop structure can be seen in the top right side of the system diagram shown in figure 2.

The analysis of the stability conditions for the switching frequency control loop and the design of the SFC are tackled at this stage. First at all, the expression which determines the value of Δ_M to be used for the hysteresis comparator of the Master switching surface is:

$$\Delta_M(t) = k_i \int e(\tau) d\tau \tag{9}$$

where k_i is the integral gain and $e = t_s^* - t_s$ is the switching period error. The expected behaviour of the Master switching function within a time variant hysteresis band is shown in figure 3. Notice that $\Delta_{M_{k-2}}$, $\Delta_{M_{k-1}}$ and Δ_{M_k} are the values of $\Delta_M(t)$ at the corresponding time instants. Although the hysteresis value is a continuous time signal, the corresponding switching periods,

t_{s_k}, and the switching period errors, $e_k = t_s^* - t_{s_k}$, yield in a sets of discrete values. From figure 3, the k-th switching period is found as:

$$t_{s_k} = \frac{2\,\Delta_{M_k}}{k_i e_{k-1} - \dot{\sigma}_{M_{u=0}}} + \frac{2\,\Delta_{M_{k-1}}}{\dot{\sigma}_{M_{u=1}} - k_i e_{k-1}}. \tag{10}$$

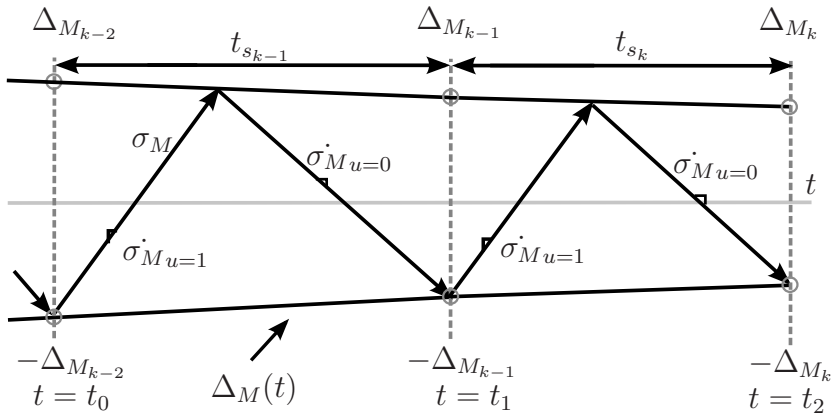


Fig. 3. Master Switching function behaviour within a variable hysteresis band.

According to the equivalent control method [24], the values of $\dot{\sigma}_M$ can be written as follows:

$$\dot{\sigma}_M = \beta E \left[u_M - u_{M_{eq}}\right] \tag{11}$$

being $\beta = \frac{\psi_1}{\alpha L}$ and $u_{M_{eq}}$ the equivalent control of the Master phase defined in (4). The expression provides the expected values of $\dot{\sigma}_M$ at steady-state sliding motion as:

$$\begin{aligned} \dot{\sigma}_{M_{u=1}} &= \beta\left[E - v_c^* - r_{L_M} i_M\right] \\ \dot{\sigma}_{M_{u=0}} &= -\beta\left(v_c^* + r_{L_M} i_M\right). \end{aligned} \tag{12}$$

As it was detailed in [28], replacing (9) into (10) generates a non-linear relationship between t_s and Δ_M. In order to linearize this expression, the following hypothesis was proposed in [28]:

$$|k_i e_k| << min\left\{|\dot{\sigma}_{M_{u=1}}|, |\dot{\sigma}_{M_{u=0}}|\right\} \;\forall\; k. \tag{13}$$

which entails that the time constant of the resulting Δ_M is much slower than the time constant of σ_M. Under this assumption, the redefined relation between t_s and Δ_M is found in (14) (see [28] for further explanations).

$$t_s = \lambda\,\Delta_M \tag{14}$$

where $\lambda = 2\left[\dot{\sigma}_{M_{u=1}}^{-1} - \dot{\sigma}_{M_{u=0}}^{-1}\right]$.

The control loop depicted in figure 4 corresponds to the linearized model of the proposed controller structure in the s domain. The transfer function shown in the feedback loop is the *padé* approximation of the delay in the switching period measurement.

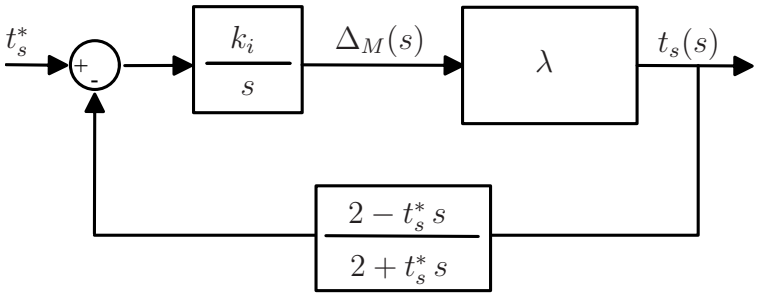


Fig. 4. Continuous time equivalent model of the regulation switching frequency control loop.

The stability conditions of the equivalent model can be easily derived using the characteristic polynomial of the closed loop system shown in figure 4, which is given by:

$$p(s) = t_s^* s^2 + (2 - k_i t_s^* \lambda)\ s + 2 k_i \lambda. \tag{15}$$

Therefore, recalling that $t_s^* > 0$ and $\lambda > 0$, the system is asymptotically stable when:

$$k_i < 2 \,/\, (t_s^* \lambda) \tag{16}$$

It has to be highlighted that the previous model can be used only when (13) is true. The system poles move towards the unstable region when k_i increases, but higher the value lower the compliance degree of (13). As a general design rule, it is recommended to choose a value of k_i such that (13) is completely ensured, and then check the stability condition deduced in (16).

E. Power Management Algorithm (PMA).

The control scheme includes a PMA in charge of selecting the enabled phases according to the output load. The PMA also decides the phase that will act as the Master one through the Master select signal (M_s), and properly configures the signals m_1 to m_8 (see figure 2). As it is stated in [26], there is a minimum number of active phases which guaranties interleaved sliding mode. Therefore the number of active phases (n) at any time should fulfil the following inequalities:

$$\text{if } u_{k_{eq}} < 0.5 \text{ then } u_{k_{eq}} > \frac{1}{n};\ \text{otherwise } u_{k_{eq}} < 1 - \frac{1}{n} \tag{17}$$

where $u_{k_{eq}}$ is given by (4). Since the input voltage of the multiphase converter considered in this work is of 48V, a minimum of three active phases are required to ensure the desired sliding mode interleaving operation in the case of 24V at the output voltage, whereas five phases are needed for a 12V regulation.

The criteria for connect or disconnect phases can vary depending on the converter desired performance. This work uses a connection rule which maximizes the efficiency. Another connection rules minimizing the active phases or improving the transient response could be applied similarly.

Moreover, the PMA performs a Master rotation among phases in order to improve the converter reliability. When a phase has to be disconnected, the Master phase is turned off and the subsequent phase is chosen as the new Master one. This procedure has the structure of a ring and distributes the operation time among the different phases.

Remark 2: In applications where the load demand varies with a large value of di_o/dt, all the phases should remain activated, otherwise the connected phase currents could exceed the maximum levels, thus compromising the converter reliability.

IV. MULTIPHASE CONVERTER IMPLEMENTATION

Table I shows the main data of the power converter built for experimental evaluation. The output voltage range, the input voltage and the desired switching frequency are defined among other interesting system data.

The multiphase converter consists on eight buck converters, a motherboard and a FPGA control board. A basic explanation of each part is presented in the following subsections.

A. Buck Converter Design.

Each buck converter is built in a different board (see figure 5). The phases are connected in parallel in the motherboard which accepts up to 8 phases (see figure 6). Each phase incorporates a voltage regulator for the switches drivers. The power switches (PSMN013100BS) are surface mount devices. This technology allows a high automatization level in the manufacturing process, reducing costs and increasing reliability. Furthermore, due to the power flow distribution related to the multiphase connection, the switches dissipate the power losses through the board copper path without any additional heatsink. Finally, each phase incorporates a power inductor (SER2918H-223), a current transformer and a Hall Effect current sensor (ACS711T).

TABLE I
MULTIPHASE BUCK CONVERTER PARAMETER

Parameter	Symbol	Value
Input Voltage Range	E	48-36 V
Desired Output Voltage Range	v_c^*	12-24 V
Output Capacitor	C	100 μF
Inductance	L	22 $\mu H \pm 10\%$
Resistance Inductance	r_L	2.6 $m\Omega \pm 10\%$
Power Switches resistance losses	r_{dson}	10.8-25 $m\Omega$
Load Range	I_o	0-65 A
Desired switching frequency	f_{sw}	100 kHz
Current transformer parameters	L_x, M	800 μH, 6.4 μH
Current transformer burden resistor	R_b	10 Ω
Sliding mode control parameters	ψ_1, ψ_2	0.078, 2.95
Switching frequency control parameter	k_i	$1.25e^8$

The current transformers are built in the laboratory using a gapped toroid which allows to hold the DC current values without saturating the core.

B. Motherboard Design.

The motherboard has eight DIM connectors (TMDSDIM100) where the buck converters are plugged in (see figure 6). In order to minimize the motherboard size, the converters has been designed making the inductor connection possible on both board sides. According to the maximum current value specified by the connector manufacturer (up to 0.5 A per pin), the 100 pins of each DIM connector have been distributed as follows: 16 pins for control signals and current measurements, 18 pins for the input voltage, 34 pins for the output voltage and 32 pins for the ground connection.

The motherboard contains the analogue circuit, shown in figure 7, that implements the Master switching surface defined in (2) and the variable hysteresis comparator. Additionally, the motherboard has a connector where the FPGA is plugged in. On the one hand, the FPGA receives

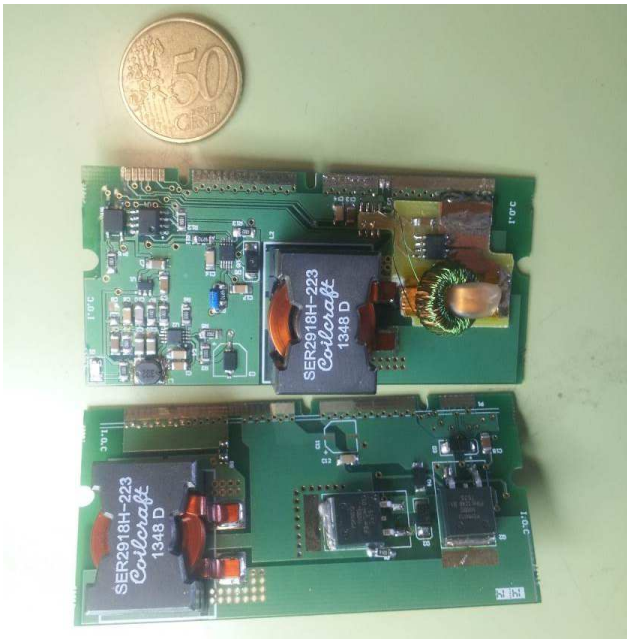


Fig. 5. Single Phase photograph.

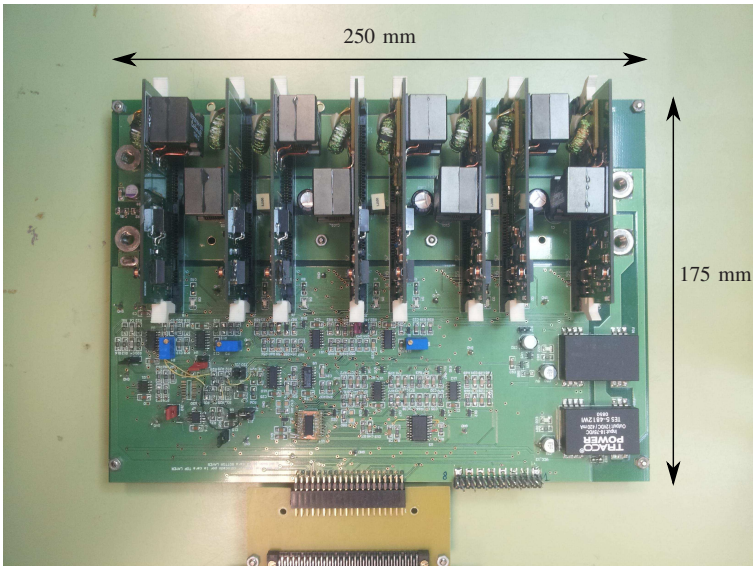


Fig. 6. Motherboard photograph.

the Master switching surface control signal and the current measurements through a analogue to digital converter (ADC) MAX1228. As it was previously stated, each phase incorporates a Hall Effect current sensor providing the measurements ($i_1 \cdot \cdot i_m$) through the DIM connectors to the motherboard, where they are filtered by analogue circuitry to get also the average values $\overline{i}_1 \cdot \cdot \overline{i}_m$.

The output current, i_o, is measured with a Hall Effect current sensor (ACS754-100) placed in the motherboard. All of these measurements, once converted by the ADC, are sent to the FPGA through the aforementioned connector. On the other hand, the FPGA uses this connector to deliver the enable and control signals ($e_1 \cdot \cdot e_m$, $u_1 \cdot \cdot u_m$) to the phases, and the Master select signal M_s. The Master control signal received by the FPGA is routed to the phase selected as Master by the PMA, and the signal (M_s) configures the multiplexer MAX382 (located in the motherboard) in order to connect the signal x_m to the Master switching surface.

The motherboard also includes the circuit that regulates the switching period of the Master control signal. The circuit scheme is depicted in figure 8. The switching period of u_M is measured by charging a capacitor with a constant current source. The voltage across the charging capacitor results in a sawtooth waveform, synchronised with u_M, since a monostable resets this voltage at any rising edge of u_M. Just before resetting the voltage the peak value of the signal is acquired, which provides a voltage proportional to t_s. The boxed areas in figure 8 *integral action* and *error signal* implement the controller defined in (9). Finally, the right part circuits in figure 8 generate the two values of hysteresis (Δ_M and $-\Delta_M$) for the Master phase hysteresis comparator shown in figure 7.

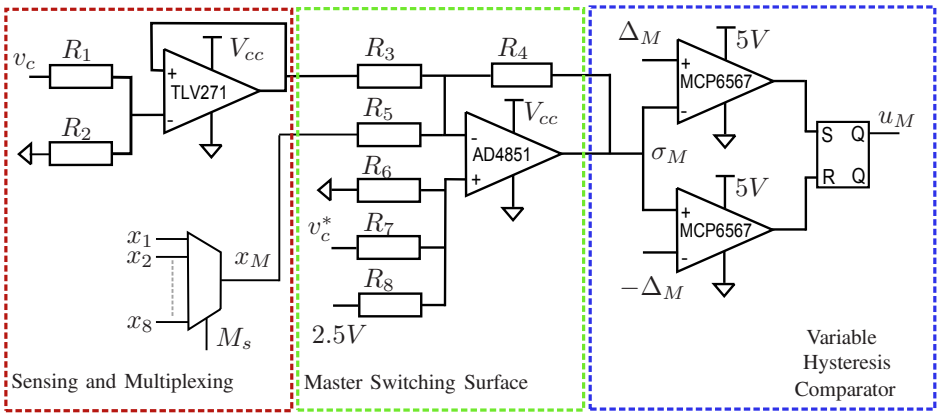


Fig. 7. Analogue electronic implementation of the Master switching surface and the variable hysteresis band comparator.

C. FPGA.

For the implementation of the Slaves switching surfaces, the PMA and the current equalization algorithm, the FPGA Spartan 3E-500 from Xilinx has been used. In this work, the evaluation

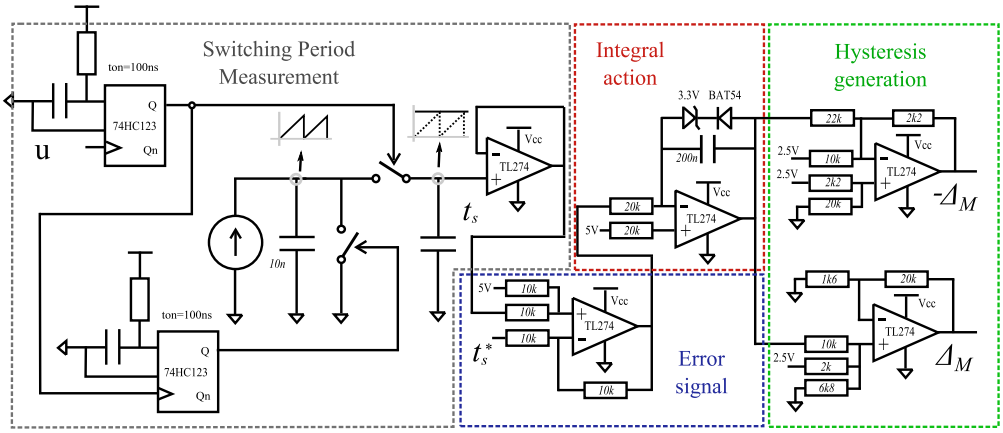


Fig. 8. Analogue electronic implementation of the Switching Frequency control.

board Nexys2 from Digilent has been selected. Figure 9 shows the system architecture employed for the implementation of the aforementioned controllers.

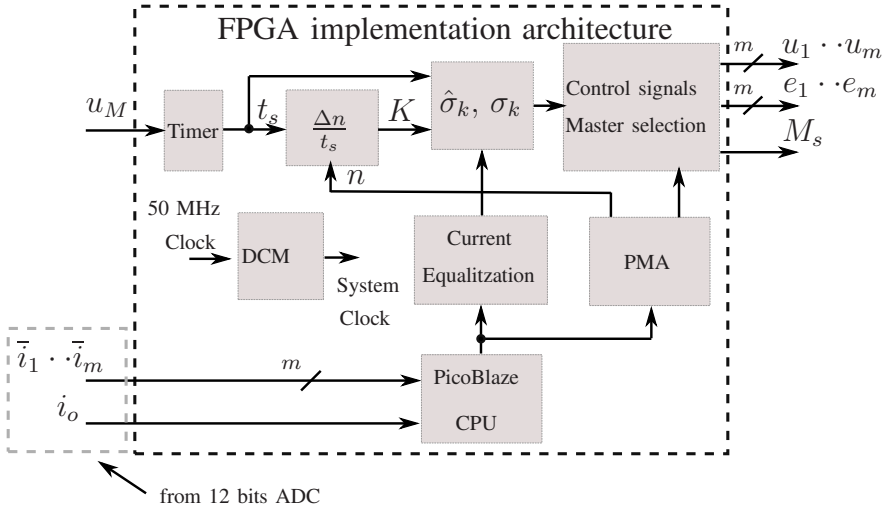


Fig. 9. FPGA block diagram implementation.

The block diagram of figure 9 points out how the Slaves surfaces $\hat{\sigma}_k$ are implemented, and how the PMA selects the active phases (n). Notice that the value of K, which provides proper interleaving operation, is updated according to the Master switching period (t_s). With regard to the current equalization algorithm, the system takes the measured current through the ADC, and using an emulated μprocessor (PicoBlaze), performs the calculations required for the surfaces σ_k.

V. EXPERIMENTALS RESULTS

Different tests have been performed to check the operation of the multiphase with the control algorithms designed in this work. Tests results are detailed in the next subsections. With regard to the controllers parameters, the switching surface parameters values (ψ_1 and ψ_2) have been selected in order to obtain an overdamped output voltage response with a time constant around $235\,\mu$s for the worst case (12 V, eight phases, $i_o = 65\,A$) evaluated using (5). For the switching frequency control loop, the gain k_i is designed to get real roots in the characteristic polynomial, shown in (15), for the overall working voltage range. The worst case corresponds to 12V at the output and yields a value of $\lambda = 2.068e^{-6}$. Using (16), the boundary value is $k_{i_{max}} = 9.67e^9$ and complex roots are obtained for values above $k_i = 1.66e^9$. According to these results, the implemented value is of $k_i = 1.25e^8$. Finally, the equalization algorithm is adjusted to get a slow dynamics in the current corrections, around 15 s, avoiding undesirable interaction with the rest of controllers.

A. *Efficiency, line regulation and load regulation.*

Table II presents the measured efficiency for different load values depending on the number of active phases and the output voltage. It has to be remarked that the efficiency considers both the control and the power stages. Notice also that due to the theoretical restriction required to ensure interleaving operation [26], [27], (see section III-E) the number of phases cannot be less than 3 for an output voltage of 24 V and must be greater than 4 in the case of 12 V. From the measured efficiency the number of active phases are selected (bold values in the table). Figure 10 shows the optimum efficiency of the power converter which achieves an efficiency of 95 $\%$ and 97 $\%$ for an output voltage of 12 V and 24 V, respectively. The second and third plots on figure 10 present the measured load and line regulations with the phases selection derived from Table II. Both measured indexes corroborate the good performance of the designed multiphase converter. On one hand, the load regulation is less than 1 $\%$ for both tested output voltages and on the other hand, the line regulation remains below 1.5 $\%$ for all the power levels.

B. *Interleaving.*

Figure 11 shows the behavior of the current transformer signals of the 8 phases in the start-up, when the converter supplies a load of 21 A and the output voltage is regulated to 24 V. As it can be seen in the oscilloscope capture, the interleaving operation is started from the second switching

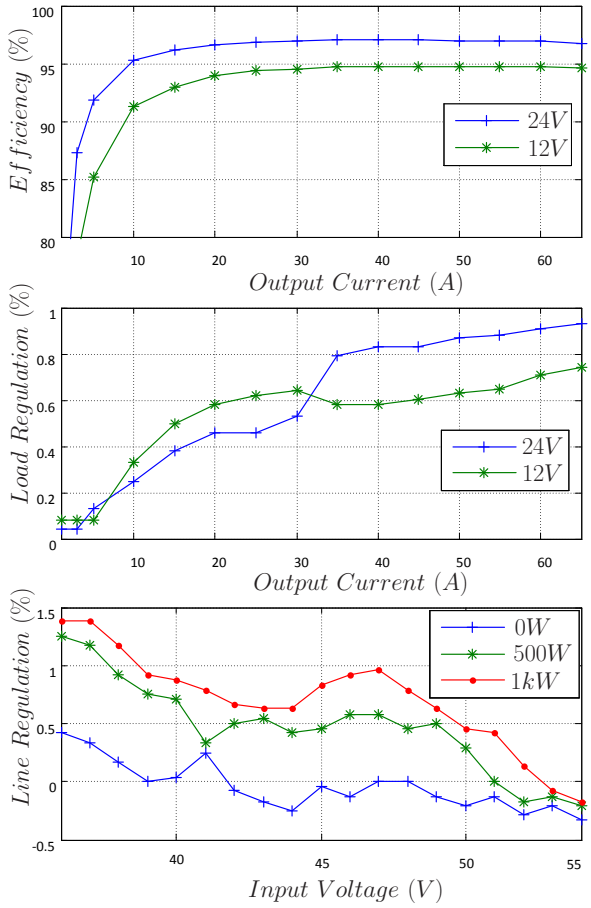


Fig. 10. Optimum efficiency and load regulation of the multiphase converter for 12 V and 24 V. Line regulation for an output voltage of 24 V.

period (see current waveforms on the left bottom window) and achieves the interleaving at the desired switching frequency of 100 kHz at steady-state (see right bottom window). Figure 12 shows the steady-state behavior of the current transformer signals of the 8 phases for a load of 65 A with an output voltage of 24 V. The current ripple flowing through the inductances can be calculated from the current transformer signals measurements. The peak to peak measured voltage value shown in the figure is of 400 mV approximately. Since the current transformer has a secondary winding of 125 turns, and this winding is loaded with a 10 Ω resistor, this voltage corresponds to a 5 A peak to peak current ripple, approximately.

C. Output voltage regulation test.

In this test the reference voltage is changed from 12 V to 24 V and reversely. The load is of 1 Ω and according to Table II the number of phases connected is 6. The figure 13 presents

TABLE II

MULTIPHASE BUCK CONVERTER EFFICIENCY (%)

$v_c \rightarrow (V)$	24	24	24	12	24	12	24	12	24	12
$phases \rightarrow$ / $i_o(A) \downarrow$	3	4	5		6		7		8	
1	**69,4**	68,0	66,7	**53,6**	65,5	52,7	64,4	51,6	63,1	50,7
3	**87,3**	86,6	85,9	**78,3**	85,3	75,4	84,6	72,2	83,9	70,6
5	**91,8**	91,4	91,0	**85,2**	90,6	84,8	90,1	84,3	89,7	83,8
10	95,0	**95.8**	95.0	**91,3**	94,9	91,1	94,6	91,1	94,4	90,8
15	96,0	96,1	**96,2**	**93,0**	96,1	92,8	96,1	92,9	95,9	92,9
20	96,3	96,5	96,6	**93,9**	**96,6**	93,8	96,6	93,8	96,6	93,8
25	96,3	96,7	96,7	94,0	**96,8**	**94,4**	96,8	94,3	96,8	94,2
30		96,7	96,7	94,2	96,9	94,4	**97,0**	**94,5**	97,0	94,5
35			96,8	94,2	97,0	94,5	97,1	94,6	**97,1**	**94,8**
40			96,8	94,1	96,9	94,5	97,1	94,7	**97,1**	**94,8**
45				93,9	96,9	94,4	97,0	94,5	**97,1**	**94,8**

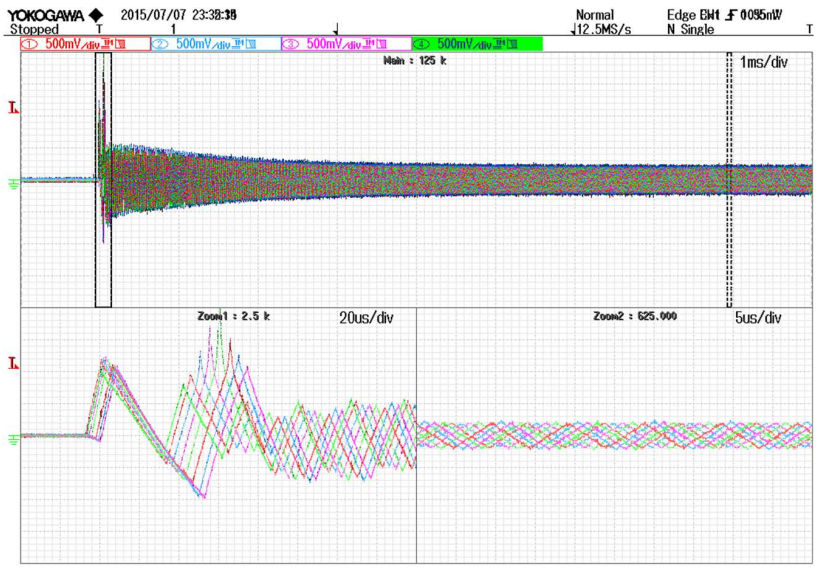


Fig. 11. Start-up of the current transformer signals of the 8 phases with a load of 21 A with a desired output voltage of 24 V.

the responses of the output voltage, the load current, the switching surface and the measured switching period (scaled by 0.5V/μs). The bottom windows show the transient behaviour when the output voltage reference changes from 12 V to 24 V (on the left window) and when it behaves from 24 V to 12 V (on the right window). Notice how the output voltage behaves with

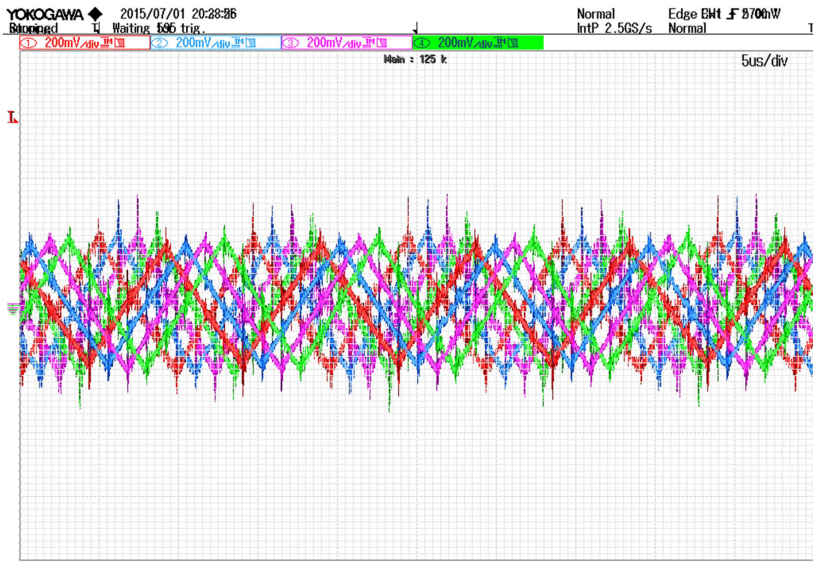


Fig. 12. Steady-state of the current transformer signals of the 8 phases for a load of 65A with an output voltage of 24V.

a smooth transient response, which corresponds to the ideal sliding motion, and the hysteresis values are adapted such that the switching frequency achieves the desired value at steady-state.

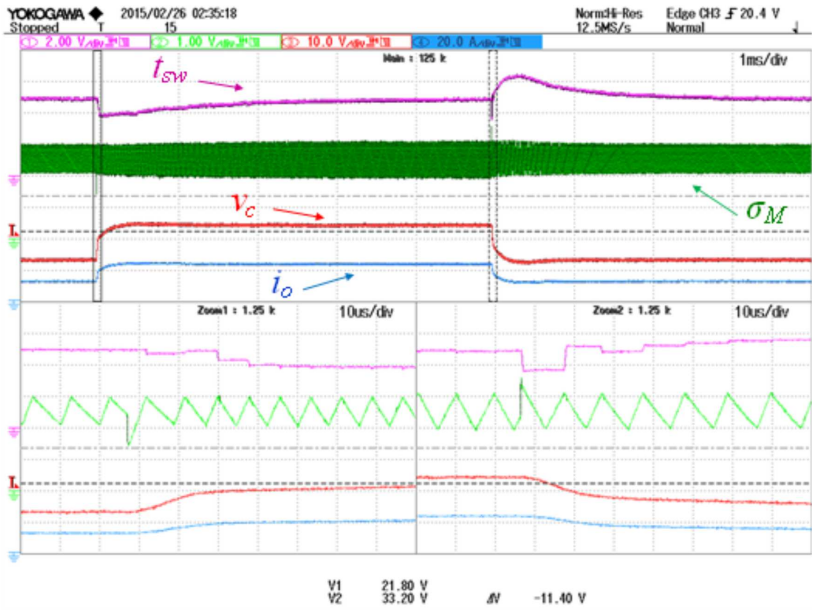


Fig. 13. Reference change 12V-24V-12V for 6 phases and a load of 1 Ω.

D. Transient response for a load change.

The following figures depict the responses of the output voltage, the switching function and the switching period (scaled by 0.5V/μs) when the load changes from 21 A to 65 A (figure 14) and from 65 A to 21 A (figure 15). In both cases, the output voltage reference is set to 24 V. Since the load is changed suddenly, all the phases are connected during this tests. From these figures it can be inferred how the converter recovers the desired output voltage after a smooth transient response and the switching frequency is not affected by the load change.

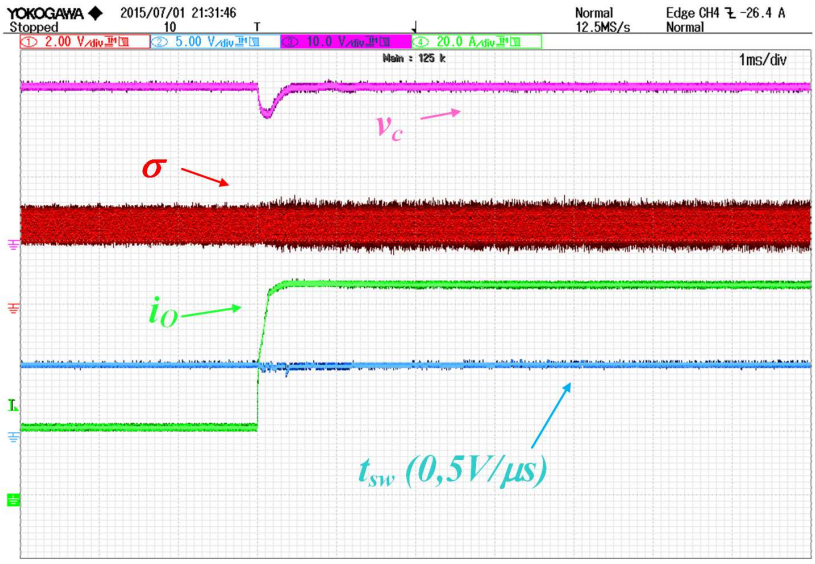


Fig. 14. Load change from 21 A to 65 A for a regulated output voltage of 24V.

E. Switching frequency regulation test.

Two different tests have been performed to show the proper switching frequency regulation. The first one consists in a start-up of the multiphase converter for an output voltage reference of 24 V delivering 21 A to the load. The results are presented in figure 16. The figure shows the behaviours of the output voltage, the switching function, the Master control signal and the measured switching period. The bottom windows details the waveforms in the transient state (left window) and in the steady-state (right window). As it can be seen in the figure, the output voltage reaches the desired voltage with a smooth transient and with a small overshoot, the hysteresis bands are adapted such that the steady-state switching frequency achieves the desired value of

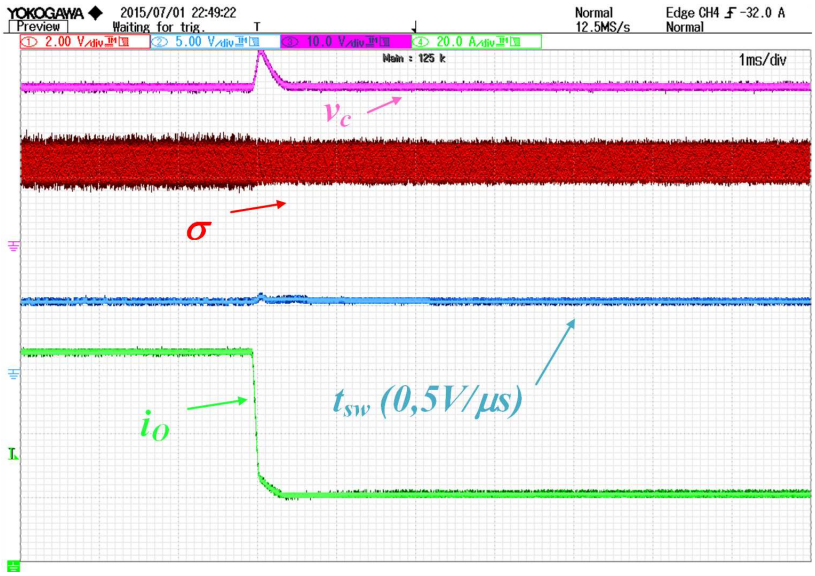


Fig. 15. Load change from 65 A to 21 A for a regulated output voltage of 24V.

100 kHz and the theoretically predicted overdamped response is observed in the switching period transient motion.

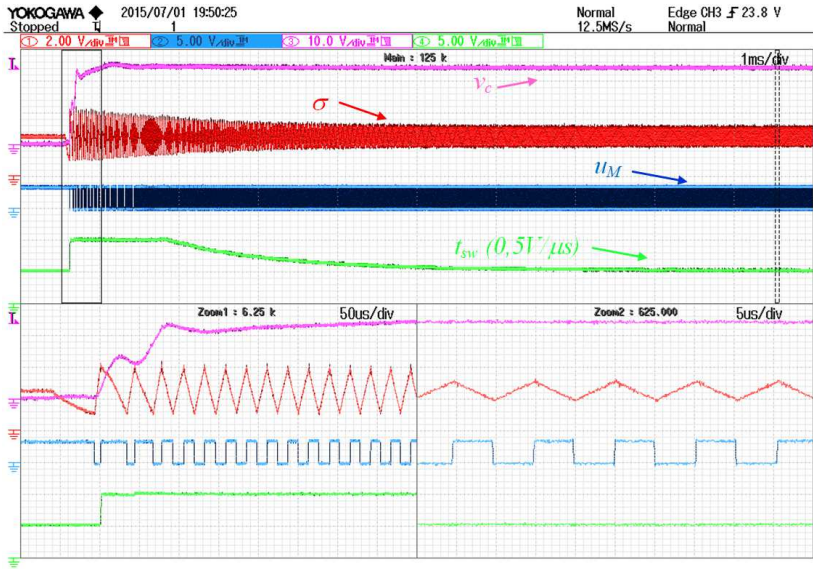


Fig. 16. Start-up with a load of 21A with a desired output voltage of 24V.

The second test is devoted to highlight the switching frequency tracking of a step type references. The switching period reference varies from 8 μs to 12 μs and vice versa. The output voltage is regulated to 24 V and the load is in open circuit. Figure 17 shows the behaviours of

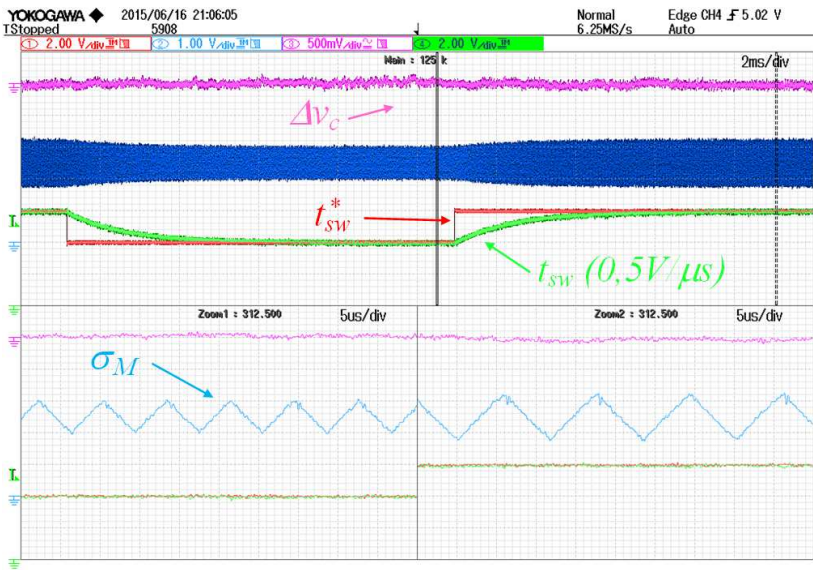


Fig. 17. Switching frequency variation from 8 s to 12 s with a desired output voltage of 24V and no load.

the output voltage ripple, the switching function, the switching period, and the switching period reference. The SFC adjusts the hysteresis band value in order to achieve the desired steady-state switching period with the expected motion according to the model derived in section III-D. Notice also that the switching function does not leave the bounds given by the hysteresis band and therefore the multiphase converter remains in interleaving operation and the output voltage is not affected by the switching frequency reference variation. This effect can be inferred from the low output voltage ripple (Δv_c) observed along the entire test. The waveforms detailed in the bottom windows correspond to the steady-state dynamics at 8 μs (left window) and at 12 μs (right window).

F. Current equalization test.

Figure 18 shows the effect over the phase currents when the equalization algorithm is enable and disable. Specifically, the figure details both transients for the eight average currents. The sensitivity of the Hall current sensors used to measure the average current is of 160 mV / A. The equalization test has been performed for the full load case and 24 V regulated at the output. When the algorithm is enabled the values of the currents flowing through each phase are around the expected value of 8.125 A with a maximum difference among them of 0.625 A. In the time frame where the equalization algorithm is disabled, the unbalance among the phases reaches the

value of 3.75 A. The result confirms the good behaviour of the algorithm, and all the average current values converge to the same value at steady-state. It has to be remarked that in the original configuration the phases present similar losses and the current unbalance becomes negligible. In order to show the good behaviour of the equalization algorithm, the phases were deliberately unbalanced adding a 10 mΩ resistor in the phases 4 and 7.

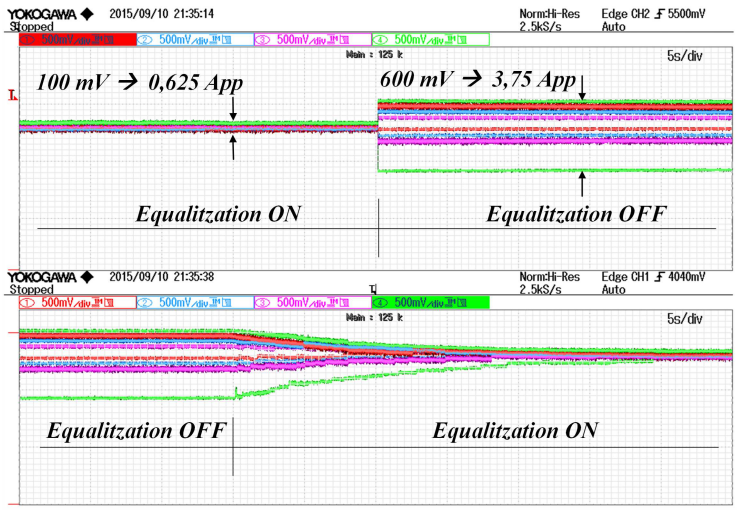
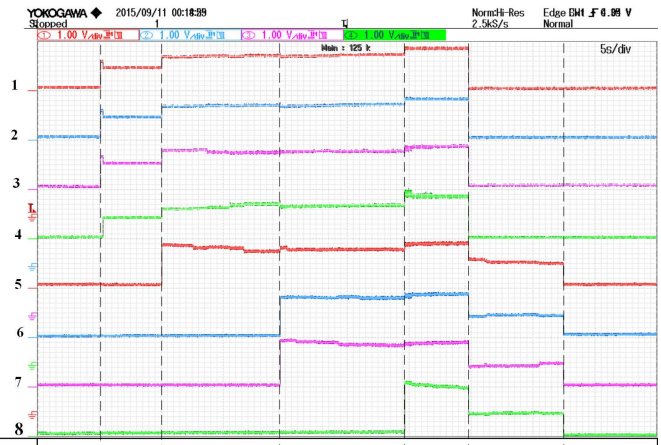


Fig. 18. Current equalization for 24 V / 65 A.

G. *Power management test.*

Figure 19 presents the currents waveforms of the 8 phases when the reference voltage is set to 24 V and the multiphase converter supplies a specific load profile. As it has been stated in the section III-E at minimum of three active phases are required to guarantee interleaving sliding mode. The figure shows how the different phases are sequentially connected (disconnected) as the load demand increases (decreases). The connection and disconnections points are selected according to the results shown in Table II. The rotating assignment of the Master phase among the converter phases can also be checked in the figure. The figure 19 also displays the number of active converters, which one is the Master phase and the values of the current supplied to the load at any time range.

Figure 20 presents the output voltage transient when a change of active phases happens. In the figure it can be seen how the system changes from 4 active phases to 3, delivering 18 A to the load. Notice how being the phase 4 the Master one, it is disabled (see the zoomed area in the



Master Phase	*1*	*1*	*1*	*1*	*1*	*5*	*6*
Phases Enabled	*3*	*4*	*5*	*7*	*8*	*4*	*3*
Output Current	*0 A*	*10 A*	*20 A*	*30 A*	*40 A*	*10 A*	*0 A*

Fig. 19. Power management. Average phase currents when the output voltage is regulated to 24V.

bottom part of figure 20) and the system selects the phase 3 as the new Master. The green signal of the figure corresponds to the output voltage. The output voltage transient has an undershoot smaller than 1 V.

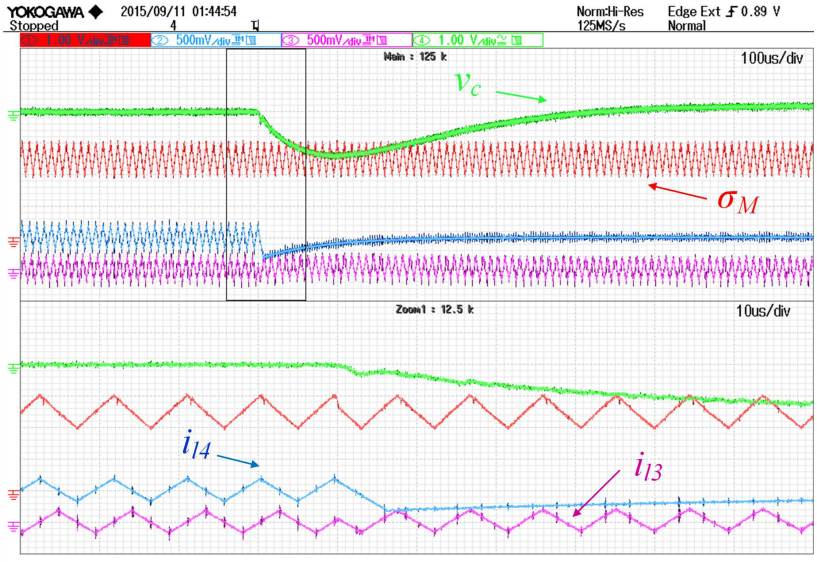


Fig. 20. Transient response of the output voltage when the system changes the number of active phases and the Master phase.

H. Thermal test.

Figure 21 shows a thermal capture of the converter when 65 A is delivered to the load with a regulated output voltage of 24 V. From the figure, a proper losses dissipation is confirmed, since the temperature remains below 60°C in the hottest parts without any type of active cooling.

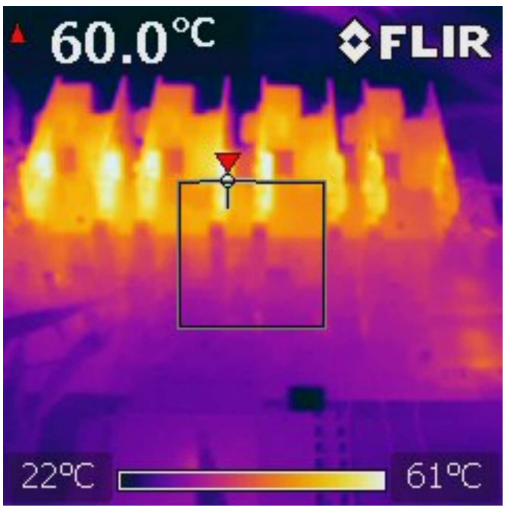


Fig. 21. Thermal image of the converter with 65 A delivered to the load with a regulated voltage of 24 V.

VI. CONCLUSIONS

In this paper an interleaved sliding mode control for a multiphase synchronous buck converter has been presented. The designed algorithm guaranties interleaving operation in all the cases. Besides of the interleaving operation, the sliding mode control includes an algorithm which enforces current equalization among the phases. Moreover, a switching frequency regulation is performed at steady-state, using an additional loop which acts over the hysteresis band value of the Master surface. Furthermore, a power management algorithm has also been added in order to select the number of active phases as function of the load demand. A set of experimental test have been carry out on an 8-phase converter built for this purpose. The controllers have been implemented using analogue circuitry together with a FPGA. The experimental results corroborate the robustness, interleaving operation, output voltage regulation, current equalization, power management and fixed switching frequency at steady-state provided by the designed controllers.

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