In situ-Doped Amorphous $Si_{0.8}C_{0.2}$ Emitter Bipolar Transistors

A. Orpella, D. Bardés, R. Alcubilla, L. F. Marsal, and J. Pallarès

***Abstract*—The fabrication and characterization of *in situ*-doped amorphous $Si_{0.8}C_{0.2}$ emitter transistors are presented. Emitter Gummel numbers exceeding 10^{14} s/cm^4 are reported for the first time in this type of structure. The high values obtained for G_E are believed to be due to the valance band discontinuity between the $Si_{0.8}C_{0.2}$ layer and the crystalline part of the emitter, which effectively blocks the minority carrier injection from the base into the noncrystalline part of the emitter.**

I. Introduction

SEVERAL attempts have been made to use amorphous $Si_{1-x}C_x$ as emitter material in silicon heterojunction bipolar transistors (HBT's) [1]–[3], arguing that a wide gap emitter should effectively block the carriers injected from the base leading to increased device performances. In particular, it should be possible to increase the base doping improving the maximum oscillation frequency without loosing gain. Two main problems have to be solved before this technology may reach a commercial success. On one hand, amorphous silicon carbon alloys present a high resistivity and high contact resistances leading to high values of the emitter resistance limiting the usefulness of the whole device. This issue is usually addressed by using a double layer emitter; a thin $Si_{1-x}C_x$ is followed by an amorphous or microcrystalline Si layer [1], [3]. On the other hand, the strong nonideality of the base currents, produced in last term by the interface between the crystalline base and the amorphous emitter and the recombination herein [1]. A possible solution, suggested in [3], is to drive-in the dopant impurities from the amorphous layer into the crystalline silicon base through a thermal treatment. In this way, the junction is located within the crystalline silicon. High emitter efficiencies have been reported for this structure [3], though some of the potential benefits of the heterojunction are lost. This work further explores this approach and reports the fabrication and experimental results of *in situ*-doped annealed amorphous $Si_{0.8}C_{0.2}$ emitter bipolar transistors showing for the first time emitter Gummel numbers over 10^{14}s/cm^4.

II. Device Fabrication

The fabricated structures are very simple. The base is produced by a boron implantation in a 1 $\Omega \cdot$ cm n-type Si wafer. The energy of the implant is 100 KeV and the dose 2×10^{13} cm^{-2}. The implantation is done through a 250-nm thick oxide in order to achieve a peak concentration of 10^{18} cm^{-3} at the surface. The resulting base width is 0.35 μm. Before the emitter deposition, an HF cleaning is done in order to minimize the native oxide layer formed at the surface of the silicon substrate. The amorphous phosphorous-doped $Si_{1-x}C_x$ layer is deposited by PECVD at 400 °C for 10 min. The gas mixture consists of 15 sccm of CH_4 and 20 sccm of SiH_4/PH_3 (20:1) and the RF power is 31 mW/cm^2. The carbon content measured by XPS is 0.2 and the thickness of the deposited layer is 300 nm. An annealing is performed at 500 °C for 60 min followed by 15 min at 870 °C. Finally, ohmic contacts are obtained by Al evaporation.

The objective of the thermal annealing is twofold. The first objective is to increase the conductivity of the $Si_{0.8}C_{0.2}$ deposited layer. An increase in more than seven orders of magnitude is achieved going from 10^{-6} (Ωcm)$^{-1}$ before the annealing to 25 (Ωcm)$^{-1}$ after the annealing. The second objective is to diffuse phosphorous from the deposited layer into the base. In that way, the electrical junction would be located within the crystalline Si and consequently the space charge recombination current would be drastically diminished. Electrical characteristics of n-type amorphous $Si_{0.8}C_{0.2}$ on p-type crystalline Silicon heterojunctions without annealing can be found in [4] for comparison.

The optical bandgap, measured by optical transmission spectroscopy, is around 2 eV before annealing. The annealing reduces the optical bandgap of the deposited layer to 1.4 eV. If we neglect the discontinuity in the conduction band [5] and we assume that both electrical and optical bandgap are similar, the resulting bandgap difference with Silicon can be found as a valence-band offset of $\Delta E_g = \Delta E_v \cong 0.28$ eV. This value is believed to be large enough to have a noticeable effect on the electrical characteristics.

III. Results and Discussion

Fig. 1 shows the Gummel plot at 300 K for a 100-μm^2 emitter structure. The collector–emitter (C–E) voltage is 4 V. Both collector and base currents are nearly ideal. The ideality factors are 1.02 and 1.03 for the collector and base current, respectively. The common emitter gain is around 1000 flat over four current decades for a 10 KΩ/sq. pinched base resistance (R_B). A significant figure of merit is the emitter Gummel

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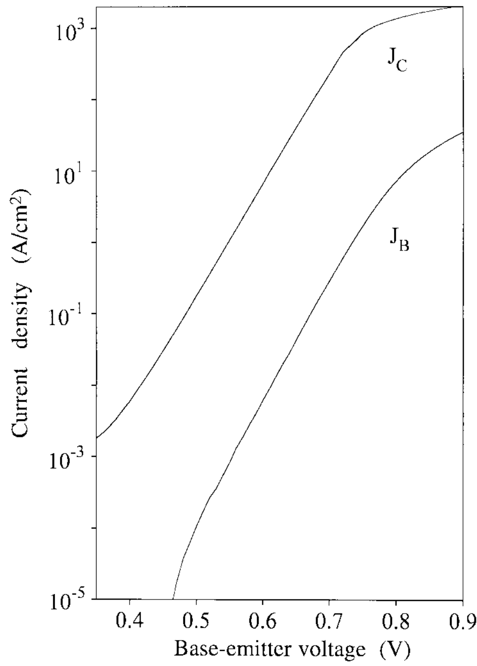

Fig. 1. Gummel plot for 100-μm^2 emitter transistor measured at 290 K, $V_{ce} = 4$ V, $R_b = 10$ KΩ/sq.

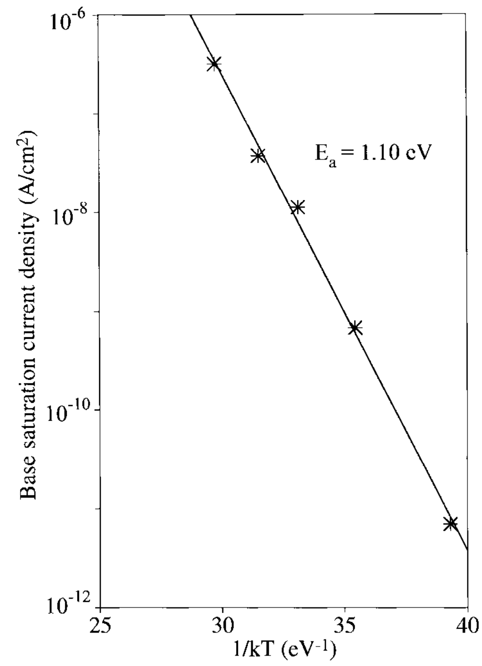

Fig. 2. Arrhenius plot of the base saturation current density.

number [6]

$$G_e = \frac{qn_i^2 h_{\text{FE, max}}}{J_{co}}. \quad (1)$$

This figure of merit reflects the emitter efficiency better than J_{BO} because it avoids ambiguities in the value of the saturation base current density due to small deviations from the ideality in the base characteristics.

Measurements done in our devices give $G_e > 10^{14}$ s·cm^{-4} and $\frac{h_{\text{FE}}}{R_B} \approx 100$ sq./KΩ. These results compare favorably with previous values obtained in amorphous $\text{Si}_{1-x}\text{C}_x$ emitter transistors [1]–[3], and also with conventional polysilicon emitter transistors with HF treatment prior to emitter deposition [7]. From SIMS measurements, both the emitter width and peak concentration have been estimated to 200 nm and 10^{20} cm^{-3}. In order to verify the physical origin of the base current, in Fig. 2 we plot the base saturation current J_{BO} as a function of 1/kT. The obtained activation energy is $E_a \cong 1.10$ eV, confirming the diffusion origin of the base current. Consequently, as is the case in polysilicon emitter transistors, the base current in the ideal range should be the addition of several components [8] represented in the band diagram of Fig. 3:

a) recombination in the neutral base (J_{rb});
b) recombination in the crystalline part of the emitter (J_{re});
c) recombination in the depletion region (J_{rd});
d) recombination at the interface between the crystalline silicon and the amorphous emitter (J_{rs});
e) injection into the amorphous layer (J_t), which may be limited by tunneling through the residual native oxide, by thermionic emission if doping segregation results in an interficial potential barrier, or by diffusion into the amorphous layer.

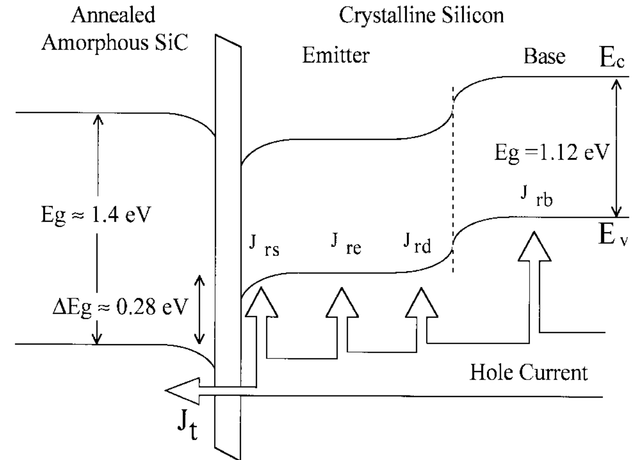

Fig. 3. Energy band diagram for the $\text{Si}_{0.8}\text{C}_{0.2}$ emitter transistor.

Differences with conventional polysilicon emitter transistors arise from the larger bandgap of the deposited layer resulting on a valence band discontinuity. This discontinuity is responsible of a strong reduction in the injected current into the noncrystalline emitter. Either tunneling through the residual oxide and thermionic emission over the barrier will reduce in a factor $\cong e^{-\Delta Ev/kT}$. As a consequence, recombination at the interface and within the crystalline emitter are expected to be the dominant components of the base current. Therefore, the injected current into the noncrystalline emitter diminishes and the total base current should be reduced on its turn, leading to increased emitter Gummel numbers.

The total emitter resistance in our devices, measured by the procedure outlined in [9], is 760 Ω μm^2. However, the emitter contact resistance measured using Cross Bridge Kelvin Resistor (CBKR) is 720 Ω μm^2, confirming that a clear

benefit may be obtained by using an additional amorphous silicon layer. For comparison, we have fabricated an identical structure, but covered with a phosphorous-doped amorphous silicon layer maintaining the annealing conditions. The obtained conductivity for the a-Si layer is 300 $(\Omega\ \mathrm{cm})^{-1}$. A total emitter resistance of 200 $\Omega\ \mu\mathrm{m}^2$ has been obtained without losing performances.

IV. Summary

We have shown that annealed amorphous $\mathrm{Si}_{0.8}\mathrm{C}_{0.2}$ on crystalline silicon junctions may be an interesting approach when high emitter efficiencies are of interest. Emitter Gummel numbers over 10^{14} s cm^{-4} have been obtained for the first time in $\mathrm{Si}_{1-x}\mathrm{C}_x$ emitter transistor structures. A theoretical framework explaining the physical origin of the reported high values for G_e has been proposed.

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