Integrated HVDC Circuit Breakers with Current Flow Control Capability

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***Abstract*— Two key problems in meshed high voltage direct current (HVDC) transmission grids are managing line power flows and protection against dc faults. Current flow controllers (CFC) will be required to balance cable currents in meshed dc grids, in order to prevent individual line power capacity limits restricting overall power flow in the grid. Direct current circuit breakers (DCCBs) will be also required to protect HVDC grids from dc faults. This paper demonstrates that the current flow controller functionality can be added into a hybrid circuit breaker's design. The article proposes to integrate an interline CFC into the load commutation switch (LCS) of a hybrid DCCB. The integrated design LCS/CFC is analyzed and a state space model is derived. The control of the CFC is designed and the performance of the LCS/CFC during normal operation is verified by means of MATLAB Simulink and PSCAD simulations. A comparison of the integrated LCS/CFC and the separate design is given. The case studies show a reduction in total power losses and improved protection operation times can be achieved.**

***Index Terms*— HVDC, grid, protection, dc, circuit breaker voltage source converter, modular multi-level, current flow controller.**

I. INTRODUCTION

HIGH voltage direct current (HVDC) multi-terminal grids are presently receiving significant attention from both academia and industry, as a mechanism to transmit bulk power over long distances [1]. Recently, several multi-terminal projects have been constructed in China, with several other multi-terminal projects being proposed in the USA and Europe [2-5].

When additional interconnections are built in these multi-terminal dc grids, the concept of meshed HVDC grids arises. Meshed dc grids face a number of additional technical challenges, such as power flow control and vulnerability to dc faults. These challenges can be tackled by using current flow controllers (CFCs) and dc circuit breakers (DCCB), respectively.

On one hand, CFCs will be required in meshed dc grids in order to prevent cables from being over loaded [6]. Using power electronics they insert variable voltage sources in series with the selected lines, thus modifying its current flow. Several topologies have been presented so far [7-9], ranging from variable resistors, dc/ac converters and dc/dc converters [9]. CFCs based on dc/dc converters provide reasonable possibilities and isolation transformers are not required for dc/ac conversion [9].

On the other hand, DCCBs are likely to be required for grid power ratings that exceed the ac systems' maximum infeed loss limits. Advanced circuit breakers designs are so-called *hybrid* dc breakers incorporate power electronics into their designs [10]. The development of both CFC and DCCB is an important step on the road to meshed HVDC grids.

While the two functional aspects of CFCs and fault protection exist separately, there is opportunity to integrate the functionality into the same equipment. This paper investigates how CFC functionality can be integrated into a hybrid circuit breaker's design if it contains a line commutation switch (LCS), or equivalent, in its primary branch.

First, an overview of the two systems under investigations is given showing a high level view of integrating CFCs into DCCBs.

Then this paper discusses hybrid circuit breakers, with specific attention given to the proactive hybrid circuit breaker (PHCB) developed by ABB [10], followed by the operation of a CFC, based on the topology of a dc/dc converter presented in [9], which consists of two H-bridge converters joined through a capacitor, where each H-bridge is connected in series with a dc line. By charging and discharging the capacitor, the CFC applies voltages on the lines that can increase or reduce the current flow.

It is then shown how the CFC can be integrated into the PHCB by changing the orientation of the switches within the LCS. This new layout is then discussed and a state space analysis is performed on the circuit breaker's commutation process. This analysis shows that the LCS/CFC design provides a reduction in the time it takes to reduce the primary branch fault current. It also shows that the LCS/CFC topology proposed in this paper has inherent advantages when compared to the traditional circuit breaker design. Then, the controller of the LCS/CFC is designed based on the state space model of the meshed dc grid, and is tested in both MATLAB Simulink and PSCAD normal operation simulations. Case studies are then performed to verify the protection operation of the LCS/CFC and the descriptive equations. The performance of the combined LCS/CFC and separate designs are also compared. A detailed system

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diagram and state space matrixes have been printed in Section XI for ease of reading.

The major contribution of this paper is the novel concept of integrating CFCs into the PHCB, the control, and the associated analysis of this novel idea.

II. DC CIRCUIT BREAKERS WITH CURRENT FLOW CAPABILITY

CFCs are used to overcome the limitations imposed on the power transmitting capability of a meshed dc system due to differences in line impedance, whereas the CBs are required in meshed HVDC grids to protect the system from dc faults.

Both the CFC and hybrid circuit breaker require power electronic elements which are permanently exposed to the dc line current. The structure of the technology that is in series with the line is similar in each case. Due to the similarities in these two pieces of equipment, it is possible to integrate the CFC capability into the circuit breaker's design. Therefore, space, power loss and material costs can be saved.

The initial meshed HVDC grid under study with the CFC located at station 1 is shown in Fig. 1(a). The meshed HVDC grid is composed of 4 stations based on voltage source converters (VSC) interconnected with four cables where a hybrid circuit breaker is included at each end of the cables.

Fig. 1(b) illustrates the same HVDC system with the proposed concept which integrates the CFC functionality into the two dc CBs in station 1.

First, the CB considered for this study is introduced in Section III and the CFC is also detailed in Section IV. Then, Section V presents the proposed integrated design and describes its operation and analysis.

III. PROACTIVE HYBRID CIRCUIT BREAKER

The PHCB was developed by ABB and is shown in Fig. 2. This circuit breaker design has been proposed as one potential design for future HVDC circuit breakers. This type of circuit breaker uses a LCS to divert current out of a mechanical switch into a semiconductor breaker. The operation of this circuit breaker is discussed in [10], with a more detailed analysis given in [11-13]. Other circuit breaker designs also contain LCSs or equivalent switches [14, 15].

The circuit breaker's LCS is a small matrix of semiconductors which are placed permanently in series with the dc line. The LCS normally remains in the conducting state and passes the line current, incurring several kilowatts of losses. Once a fault is detected the current is diverted into a main breaker by turning off the LCS.

The LCS could be a single device, but due to the voltage, current, redundancy, and power loss requirements, the LCS will likely be made up from several devices [12].

The circuit breaker is modeled representing each power electronic switch as a single switch model, parameterized for the desired voltage rating. The mechanical switches have been modeled as ideal switches with a fixed delay to replicate the opening of the mechanical switch. The circuit breaker has been parameterized for a 300 kV application using the information given in Table 1, [10, 12], and analysis in [11].

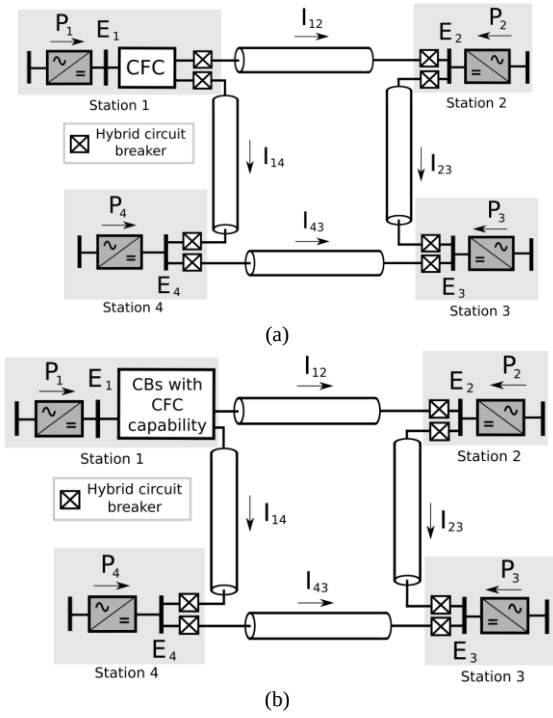


Fig. 1. Meshed HVDC grid under study. (a) CFC and CBs in a separate design (b) Proposed integrated CBs with CFC functionality

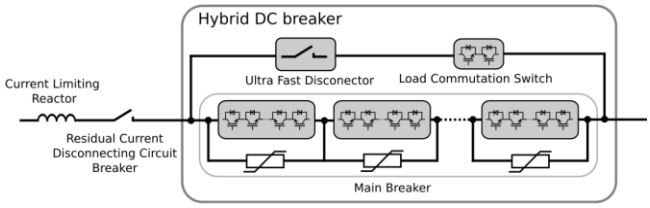


Fig. 2. The Proactive Hybrid Circuit Breaker [10].

TABLE 1
CIRCUIT BREAKER PARAMETERS. MB = MAIN BREAKER

Parameters	Values	Parameters	Values
L_1 / L_s	0.1 H / 30 µH	Snubber capacitance	0.234 µF
V_{on}	904 V	Mech. Opening Time	2 ms
R_{on}	0.1 Ω	Detection Time	1 ms
Series devices per direction	149	Knee Voltage	320 kV
		K_v	2

IV. CURRENT FLOW CONTROLLER

A diagram of the CFC is presented in Fig. 3. The CFC topology used in this paper is presented in [9] and its operation and control methodology are described in [16]. The CFC is based on two H-bridge converters joined through a capacitor and each bridge connected to a different dc line in the meshed HVDC grid. The CFC extracts power from one cable and feeds the other, thus, applying variable voltage sources in the lines. By doing so, it is able to reduce or increase the dc currents circulating through the lines of the HVDC grid. The proposed dc/dc converter can be used for any current direction, though for this analysis, I_1, I_{12} and I_{14} are considered

to be positive during normal operation. Considering the aforementioned current configuration, the active switches that are able to operate are: S_{A1}, S_{B1}, S_{A2} and S_{B2} and according to [16], S_{A1} and S_{A2} are operated with the same signal; the other switches are always off. The operation states of the CFC are summarized in Table 2, considering I_1, I_{12}, $I_{14} > 0$. "1" means the switch is on and "0" means the switch is off.

A. *CFC modelling*

Table 2 illustrates the switching states of the CFC and the voltage that they are applying in both lines 12 and 14. Combining some of the states depicted in Table 2, the CFC is able to apply a positive voltage in one line and a negative voltage in the other so that the line current of one line can be diverted to the other. The converter average model can be derived as two voltage sources in series by combining adequately some states in Table 2 as explained in [16]. Considering [16], the average voltages applied by the CFC are:

$$\bar{V}_{1\_cfc} = (1 - D)\bar{E} \qquad \bar{V}_{2\_cfc} = -D\bar{E} \qquad (1)$$

D is the current relation between I_{12}/I_1 which is equivalent to the duty cycle of the switch S_{A1} and S_{A2} when the CFC is reducing current I_{12} compared to the initial conditions. When the CFC is reducing current I_{14}, D corresponds to the duty cycle of the diodes in S_{D1} and S_{D2}. $\bar{E}$ is the average voltage of the CFC capacitor when the CFC is reducing I_{12}. When the CFC is reducing I_{14} it corresponds to the negative value of the average capacitor voltage. The previous average model derivation is explained in detail in [16]. For the MATLAB and PSCAD simulations the CFC is modelled in detail using a switch model composed of 8 insulated-gate bipolar transistors (IGBTs), allowing the conduction losses in the devices to be calculated. The switching frequency of the CFC is 2 kHz and its capacitance, C, is set to 10 mF. The average model of two voltage sources is used only for the controller design.

V. INTEGRATED LCS WITH CFC CAPABILITY

The LCS structure of the PHCB shares many similarities with the CFC topology presented in Section IV, therefore, the CFC capability is integrated in the PHCB using the LCS of the two CBs in the same Station 1.

An example of LCS structure is shown in Fig. 4(a). This topology allows bi-directional current breaking in the primary branch. Bi-directional capability will be required when the circuit breaker provides backup protection.

Taking the same switches and rearranging their orientation allows the LCS to act as a CFC during normal operation, as shown in Fig. 4(b). The LCS now resembles one half of the traditional CFC structure given in Fig. 3.

Neighboring circuit breakers can then have their LCSs connected together as shown in Fig. 5. During normal operation the main breakers within each circuit breaker will be turned off and the mechanical switch (M_1) must be in on state. The required dc side inductor (L_{DC}) must be placed on the cable side rather than the converter side of the circuit breaker.

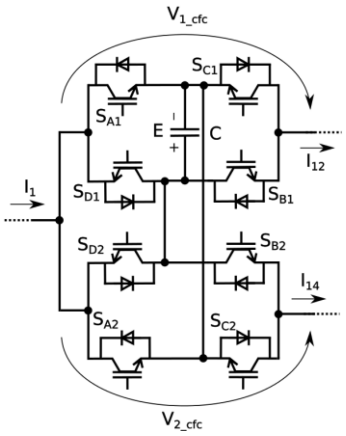


Fig. 3. Dual H-bridge CFC topology.

TABLE 2
SWITCH STATES OF THE CFC

$I_1, I_{12}, I_{14} > 0$								
$S_{A1,2}$	0	0	0	0	1	1	1	1
S_{B1}	0	0	1	1	0	0	1	1
S_{B2}	0	1	0	1	0	1	0	1
V_{1_cfc}	+E	+E	0	0	0	0	-E	-E
V_{2_cfc}	+E	0	+E	0	0	-E	0	-E

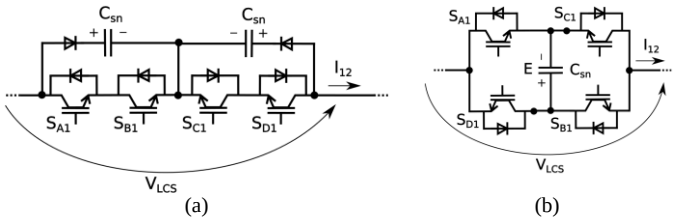


Fig. 4. (a) LCS structure. (b) LCS Structure with CFC capability.

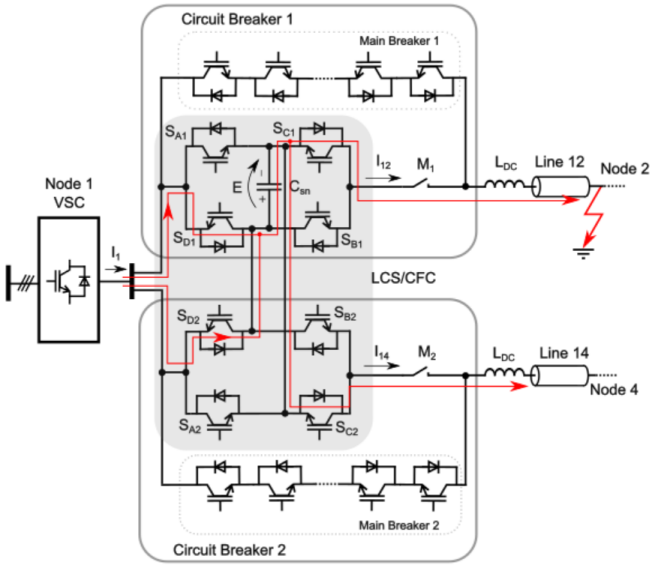


Fig. 5. LCSs interconnected with CFC capability. Current flow considering a fault on Line 12 with the LCS/CFC switches in off state and the main breakers turned off.

This allows the LCS/CFC to have the common node required for CFC operation. The LCS/CFC is operated following the same procedure of the single CFC [16]. When a fault occurs, current starts to flow from the converter and other lines towards the fault location as can be seen in Fig. 5.

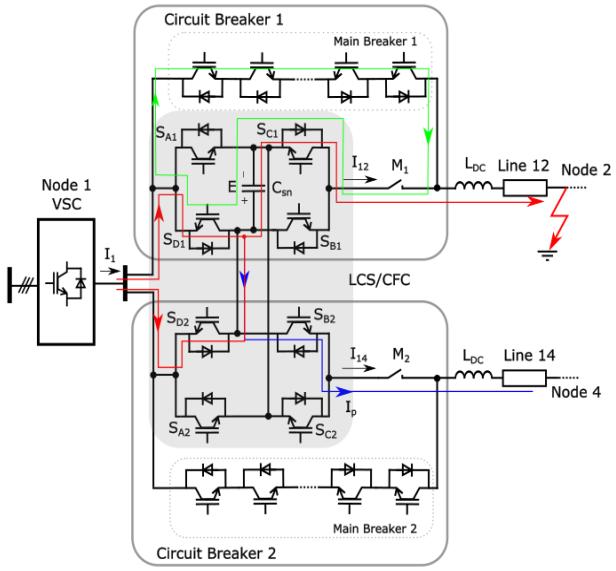


Fig. 6. Shows the current flow path within the LCS/CFC once the Main Breaker is turned on.

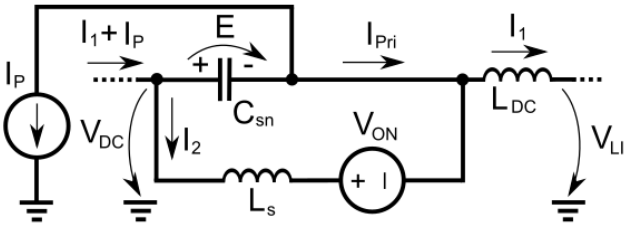


Fig. 7. Equivalent circuit during commutation.

When the circuit breaker is required to open, the switches in both LCS/CFCs are turned off and the main breaker of the faulted line is turned on. The current flowing through the LCS/CFC diodes charges the LCS/CFC capacitor, as shown in Fig. 6. Current starts to flow through the Main Breaker as it now provides a low impedance path allowing current to be diverted away from the mechanical switch (M1) by the voltage across the LCS (V_{LCS}). This allows the mechanical switch to be opened without an arc, and once the switch is fully open the main breaker can be turned off to break the flow of current [9].

The switches in the CFC/LCS can be driven by using the CFC capacitance as a floating voltage supply. The CFC capacitance will naturally charge once a DC line current starts to flow in either direction. The current will flow through the CFC/LCS's diodes and pass through the CFC capacitance. Once charged this can be used to provide the gate drives voltages to allow switching to start.

The LCS/CFC design also requires the circuit breaker's inductance to be on the cable side of the circuit breaker, rather than the converter side. While the authors can see no reason why this would be a negative to this design, there may be a practical limitation that prevents this.

The circuit breaker is able to operate in this fashion for pole-to-pole and pole-to-ground faults. The circuit breaker can still operate without a fault as the CFC/LCS voltage can be used to push the load current into the secondary branch. Providing that there is a DC current flowing or if the CFC is sufficiently charged, the circuit breaker will be able to operate as described.

A. State space analysis of LCS/CFC Commutation

A state space analysis of the circuit breaker with CFC capability has been performed using the equivalent circuit during commutation given in Fig. 7. This analysis works for circuit breakers on the positive or negative poles of the DC link, as well as for pole-to-ground faults.

This equivalent circuit was developed based on a reduction of the physical circuit layout, where: C_{sn} is the capacitance of the LCS/CFC; L_{DC} is the circuit breaker's series dc side inductor; L_s is the parasitic inductance of the secondary branch; I_P is the partner line current, V_{on} is the total on-state voltage of the semiconductors in the secondary branch and R_{on} the total on-state resistance. V_{DC} is the voltage across the converter's terminals and V_{LI} is the line voltage. Starting with:

$$\begin{bmatrix} L_{DC} & 0 & 0 \\ 0 & L_s & 0 \\ 0 & 0 & C_{sn} \end{bmatrix} \dot{\boldsymbol{X}} = \begin{bmatrix} 0 & 0 & -1 \\ 0 & 0 & 1 \\ 1 & -1 & 0 \end{bmatrix} \boldsymbol{X} + \begin{bmatrix} 1 & 0 & 0 \\ 0 & -1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \boldsymbol{U} \tag{2}$$

and the matrix layout given as:

$$\boldsymbol{X} = \begin{bmatrix} I_1 \\ I_2 \\ \mathrm{E} \end{bmatrix}, \boldsymbol{X_0} = \begin{bmatrix} I_0 \\ 0 \\ V_0 \end{bmatrix}, \boldsymbol{U} = \begin{bmatrix} V_{DC} - V_{LI} \\ V_{ON} \\ I_P \end{bmatrix} \tag{3}$$

The primary branch current can be solved for as the difference between the two current state variables in the s-domain, yielding:

$$I_{pri}(s) = I_1(s) - I_2(s) = \frac{[I_0 + I_P]s + G}{s^2 + \frac{L_{DC} + L_s}{C_{sn} L_{DC} L_s}} - \frac{I_P}{s} \tag{4}$$

Converting this to the time domain:

$$I_{pri}(t) = \left[\sqrt{[I_0 + I_P]^2 + G^2}\right] \cos(\omega_{com} t - \emptyset) - I_P \tag{5}$$

where:

$$G = \left[\frac{[L_s V_{DC} + L_{DC} V_{ON}] - V_0 [L_{DC} + L_s]}{L_{DC} L_s \omega_{com}}\right] \tag{6}$$

$$\omega_{com} = \sqrt{\frac{L_{DC} + L_s}{C_{sn} L_{DC} L_s}} \tag{7}$$

$$\emptyset = tan^{-1}\left[\frac{G}{I_0 + I_P}\right] \tag{8}$$

Then, solving for the state variable that describes the LCS voltage:

$$E(t) = A + [V_0 - A]\, cos(\omega_{com} t) + \left[\frac{I_0 + I_P}{C_{sn} \omega_{com}}\right] sin(\omega_{com} t) \tag{9}$$

where:

$$A = \frac{L_s V_{DC} + L_{DC} V_{ON}}{(L_{DC} + L_s)} \quad (10)$$

Manipulating (5), the commutation time (the time when I_{pri} = 0) is given by:

$$t_{com} = \frac{1}{\omega_{com}} \left[\cos^{-1} \left[\frac{I_P}{\sqrt{[I_0 + I_P]^2 + G^2}} \right] + \emptyset \right] \quad (11)$$

Based on the analysis presented in [11] the commutation time of the PHCB is normally bounded between $\frac{\pi}{2\omega_{com}}$ and $\frac{\pi}{\omega_{com}}$ for a fixed capacitance value. The combined LCS/CFC does not have this limitation as the commutation time can be reduced below $\frac{\pi}{\omega_{com}}$.

Fig. 8 shows comparison of simulations of the traditional LCS (Case 3), a CFC/LCS (Case 1), and the analysis presented in this section. Details of the simulations can be found in Section VI; where a case study has been performed. The analysis is compared to the simulations which show a strong agreement.

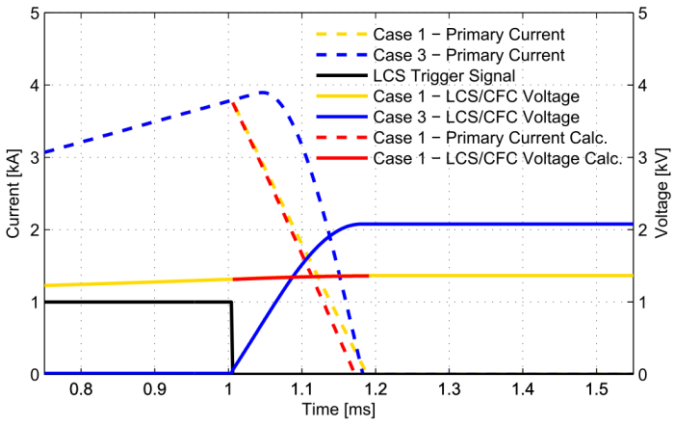


Fig. 8. Verification of commutation analysis for combined and separate cases. PSCAD results and calculations.

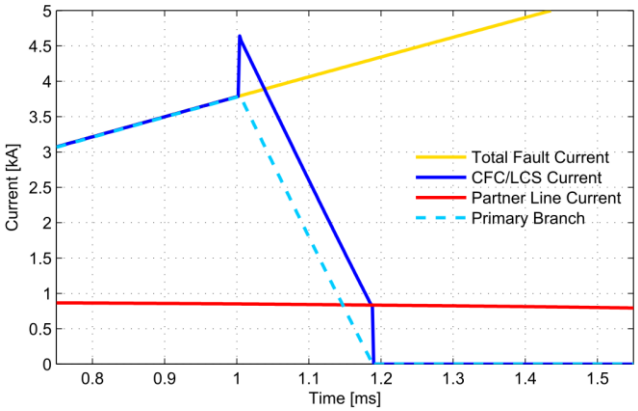


Fig. 9. Commutation process with LCS/CFC. Partner line current = Ip. PSCAD Results.

This shows the difference in the circuit breaker currents and voltages during commutation for the LCS and CFC/LCS. When the LCS is turned off the LCS voltages increase in both cases, and start to force the primary branch current into the Main Breaker. The CFC/LCS s able to commutate the current quicker and with a lower peak voltage; for the examples given.

This fundamental difference comes from the pre-charged nature of the CFC/LCS and the coupling from the partner line current; the latter is shown in Fig. 9. The CFC/LCS current is the current that flows through the CFC/LCS capacitor. As the partner line current can be quickly diverted into this capacitor, this is able to contribute to the commutation voltage; resulting in a shorter commutation time.

VI. PSCAD MODELING

In the PSCAD simulations, the HVDC system in Fig. 1(b) is modeled using the full 4-terminal model shown in Fig. 18 at the end of the paper in Section XI. During normal operation, the offshore wind farm, Station 4, is delivering 0.2 GW into HVDC system and Station 1 delivers 1 GW. Converter stations 2 and 3 receive 0.7 GW and 0.5 GW, respectively.

The onshore two-level converters are modelled with switched IGBTs, phase reactors, transformers and dc link capacitors. The converters are controlled using voltage droop control [17]. Based on [18], Station 4 is configured to provide the offshore ac grid voltage and frequency.

The wind farm is modeled aggregately, with the back-to-back converter in each wind turbine modelled using an averaged model. The offshore side transformer configuration is based on [19].

DC choppers have been used in each onshore converter's terminal to regulate the dc voltage within the normal voltage range, with the parameters from [20].

The MMC model here uses the detailed equivalent model (DEM) [21]. In the DEM used in this paper, each phase arm consists of 30 sub-modules which can provide 31 voltage levels. The MMC station is set to control active and reactive power. Fig. 10 illustrates the control diagram for the MMC.

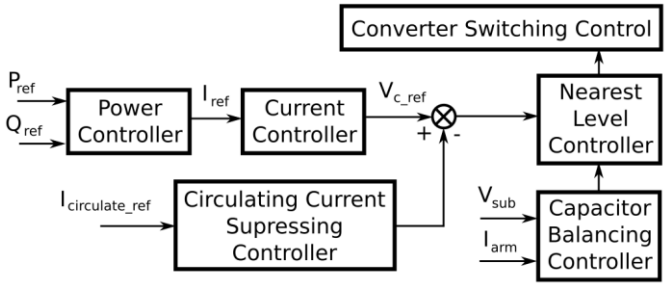


Fig. 10. Control structure of the MMC system.

VII. SIMULINK MODELING

The system presented in Fig. 1(a) is modeled in Simulink. Two models are employed: First, a linearized state space model of the dc grid with the average model of the CFC for controller design purposes is derived. A second model, with the switching model of the CFC is utilized to validate the control design methodology and it is compared with the full model in PSCAD from Section VI. The Simulink models are used to verify the controller design and only consider half the pole. These are then compared to the PSCAD simulations to provide a cross simulation verification of design.

A. *Linearized state space model*

The linearized model of the meshed HVDC grid is derived following the same strategy as in [16]. The model is shown in Fig. 11 and where only the upper half of the symmetrical monopole of the system is considered due to its symmetry. Following this approach only one CFC needs to be modelled in the system. The CFC is modeled as two voltage sources. Cable capacitance is neglected due to its reduced value compared with node capacitance; only the inductance and resistance of the cable are considered. L_{ij} gathers the inductance of cable between node i and node j and the two dc limiting reactors of each line (L_{DC}). R_{ij} comprises the resistance of the cable and C_i is the power converter capacitance of node i. The system is linearized as [22]:

$$X_i \approx X_{i0} + \Delta X_i \tag{12}$$

where, X_i is a general variable, X_{i0} is its linearization point and ΔX_i is the increment over the linearization point. Terminal 1 and 2 are operating in dc voltage droop control and terminal 3 and 4 in constant power injection mode:

$$I_1 = \frac{P_1}{E_{base}} + \frac{k_d P_{base}}{{E_{base}}^2}({E_1}^* - E_1) \tag{13}$$

$$I_2 = \frac{P_2}{E_{base}} + \frac{k_d P_{base}}{{E_{base}}^2}({E_2}^* - E_2) \tag{14}$$

$$I_3 = \frac{P_3}{E_3} \qquad I_4 = \frac{P_4}{E_4} \tag{15}$$

where, P_i are the powers of node i, I_i are the currents of node i, E_i are the voltages of node i. ${E_i}^*$ are the voltage droop references of node i. k_d is the droop constant and P_{base} and E_{base} are the base power and voltage. The meshed HVDC grid and the previous equations are linearized following the same approach as in [16] and the following state space model is obtained; **A** and **B** are given in (18) in Section XI. The parameters of the Simulink models are illustrated in Table 3.

$$\frac{d\Delta x}{dt} = \boldsymbol{A}\Delta x + \boldsymbol{B}\Delta u \tag{16}$$

Where:

$$\Delta x = (\Delta E_1, \Delta E_2, \Delta E_3, \Delta E_4, \Delta I_{12}\Delta I_{14}, \Delta I_{23}, \Delta I_{43}, \Delta E,)$$
$$\Delta u = (\Delta P_1, \Delta P_2, \Delta P_3, \Delta P_4, \Delta D) \tag{17}$$

B. *CFC switching model*

The second model of the HVDC grid and the CFC also only considers the upper half of the symmetrical monopole, but in this case the cables are modelled as PI equivalent and two dc limiting inductors (L_{DC}) are placed in each line. The modelling of the converter terminals are the same as in Section VII.A. The CFC is modelled as two H-bridges as shown in Fig. 3 and the system model is depicted in Fig. 12.

VIII. LCS/CFC CONTROL DESIGN METHODOLOGY

The control design methodology is based on the state space representation of the 4-terminal HVDC system, presented in Section VII.A. The same procedure as [16] is applied.

The variable to be controlled is set to be dc current I_{12} and the control action is the duty cycle of the operating switch ($S_{A1,2}$). Based on the state space model, a transfer function relating the current I12 and duty cycle D is obtained (GI12-D). For this work, a Proportional Integral (PI), a 2nd order compensator and a low pass filter are used for the controller. It is tuned to achieve a closed loop time response of 0.6 s and no overshoot in capacitor voltage. The controller parameters are presented in Table 4, considering that current I12 is measured in Amps. Fig. 13 illustrates the control scheme.

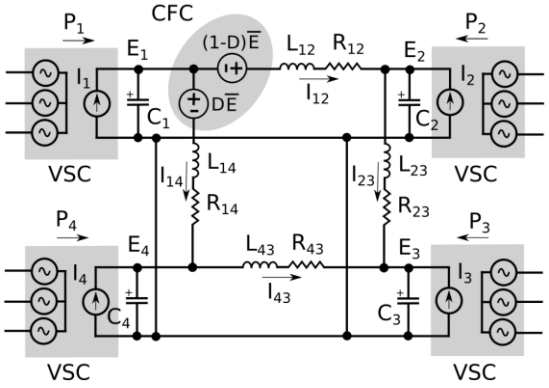


Fig. 11. Equivalent model of the 4-terminal HVDC system with CFC used for linearization.

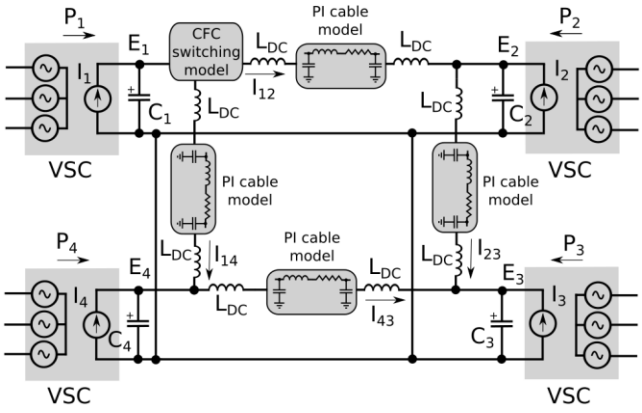


Fig. 12. Equivalent model of the 4-terminal HVDC system with the CFC switching and PI cable models.

TABLE 3
SIMULINK MODEL PARAMETERS

Cable parameters				
Resistance [Ω/km]	0.0113	Inductance [mH/km]	2.777	Capacitance [μF/km]	0.2635
Lines	12	14	23	43
Distance [km]	100	60	100	60
VSC parameters				
Nodes i	1	2	3	4
Power P_i [MW]	1000	-700	200	-500
Capacitance C_i [μF]	200	200	200	200
Voltage ${E_i}^*$ [kV]	298	298	-	-
Droop k_d [pu/pu]	2	2	-	-
Base values				
Node voltage [kV]	Node Power [MW]	Line current [kA]	CFC voltage [kV]	
300	1200	2	4	

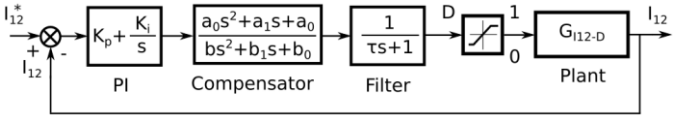


Fig. 13. Control scheme of the CFC

TABLE 4
CONTROLLER PARAMETERS

PI Controller		2nd order compensator			L.P. Filter	
K_p	$2.48 \cdot 10^{-5}$	a_2	a_1	a_0	τ	0.03
		522	1094	29889		
K_i	$6.29 \cdot 10^{-4}$	b_2	b_1	b_0		
		1	746	18616		

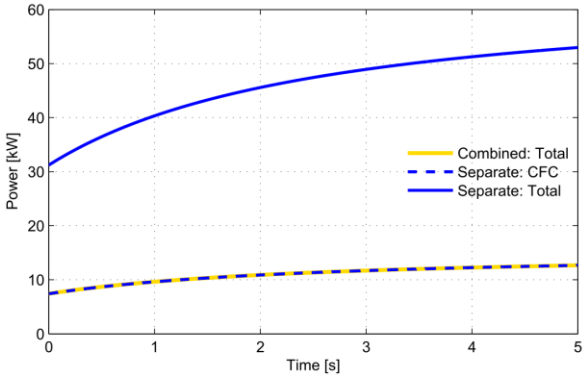
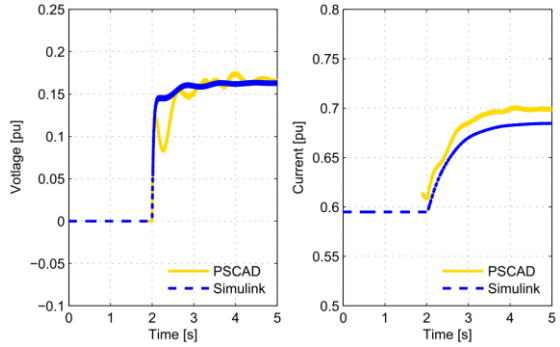


Fig. 14. Comparison of power losses for combined and separate designs. The power losses time vary as the power is gradually increased to the set point.



(a) (b)

Fig. 15. Comparison of Normal operation case study results from Matlab and PSCAD simulations. (a) LCS/CFC voltage V_{LCS}. (b) Current I_{12}.

A. *Normal operation of the LCS/CFC*

The first study performed is a normal operation analysis of the LCS/CFC, to ensure that its CFC operation is conserved. The results of the CFC in the Simulink and PSCAD models are shown in Fig. 14. Comparison of power losses for combined and separate designs. The power losses time vary as the power is gradually increased to the set point., respectively, and indicate a good match. In both cases, the I_{12} is increased by approximately 0.1 pu as seen in Fig. 15(b) and the CFC/LCS voltage is shown in Fig. 15(b). The voltage dip seen in the PSCAD simulations is due to the different cable models used; however, the dominant dynamics of the response are very similar, which verifies the control design.

The losses calculated from the PSCAD simulations are shown in Fig. 14. The combined case considers the integrated LCS/CFC, whereas the separate design takes into account the single CFC and the two PHCB (per pole) in both lines presented in Fig. 1(a). The results show the combined case losses are significantly lower than the separated design case.

B. *Protection simulations*

A second study was undertaken to assess the differences in protection performance of combined and separate designs. The study aimed to show that the circuit breaker is still capable of operating when the CFC is integrated into the LCS and verify the analysis performed in Section V.

TABLE 5
COMPARISON OF COMBINED AND SEPARATE LCS AND CFC DESIGNS

Case		C_{sn} [µF]	LCS Voltage V_{LCS} [kV]	CFC Voltage E [kV]	Com. time [µs]
Combined	1	10000	1.32		184
Separate	2	10000	1.02	5.89	2286
	3	160	3.84	3.32	104
	4	11	6.81	3.28	30

The major design choices for an LCS are the peak voltage, and commutation time. These two attributes are heavily dictated by the snubber circuit capacitance used. For the combined LCS/CFC, the capacitance is fixed based on the acceptable ripple voltage in the CFC. This capacitance is several orders of magnitude larger than what is thought to be used in the LCS. In order to compare the separated and integrated approach properly, several different LCS capacitance values were chosen (10 mF, 160 µF and 30 µF).

A protection study was undertaken for a fault located between converter station 1 and 2, 50 km along the line. Four different design cases were assessed. Case 1 is the case where the CFC and LCS are combined. The commutation circuit capacitance is defined by the design of the CFC, which was 10 mF. In Case 2 the CFC and LCS exist separately and the LCS capacitance is chosen to be the same as Case 1. Case 2 was chosen to show that the commutation time is drastically impacted if the LCS's capacitance is increased to reduce the peak LCS voltage. In Case 3 the capacitance is designed to have a similar commutation time in Case 1. Case 4 uses a low value of capacitance to show a fast commutation time. For the separated designs the CFC capacitance is 10 mF.

Fig. 16 compares the performance of the four case studies during a protective action and it shows the current through the primary branch and the total current of the line for each case. Cases 1,3 and 4 all maintain a reasonable circuit breaker operation time, due to the commutation times being kept in the order of microseconds. Case 2 has a commutation time of 2.2 ms, which extends the operation time of the protection beyond a reasonable time frame. This shows that reduction in peak voltage obtained from this design, cannot be achieved by simply increasing the LCS's capacitance; without compromising protection performance.

Fig. 17 shows a plot of the governing equations for commutation time and peak voltages across the inline power electronics (LCS and CFC) [11]. This shows that there is a fundamental difference in the governing equations due to the LCS/CFC's capacitor being pre-charged and the coupling between the DC lines (I_P). As there is less variation in commutation time when the LCS/CFC capacitance is increased, a higher capacitance can be used, which results in a significantly lower peak voltage across the LCS.

A summary of the commutation times, voltages across the power electronic elements and the case parameters is given in Table 5. The results show that even though the LCS/CFC has a significantly larger capacitance, the commutation time is not detrimentally extended and is within the experimental times

stated in [10]. The peak voltages across the CFC and LCS are also significantly reduced compared to the other cases.

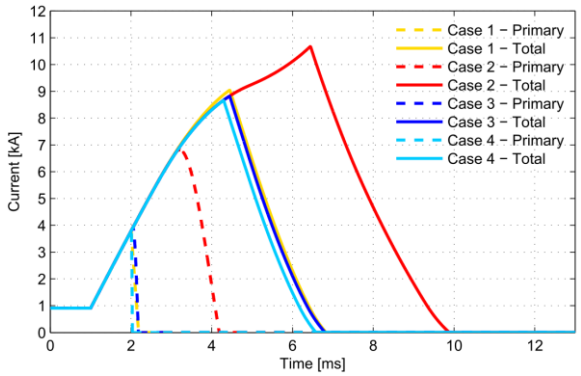


Fig. 16. Fault Current Comparison for each case. Total fault current (solid lines). Primary branch current (dashed lines) - PSCAD Results.

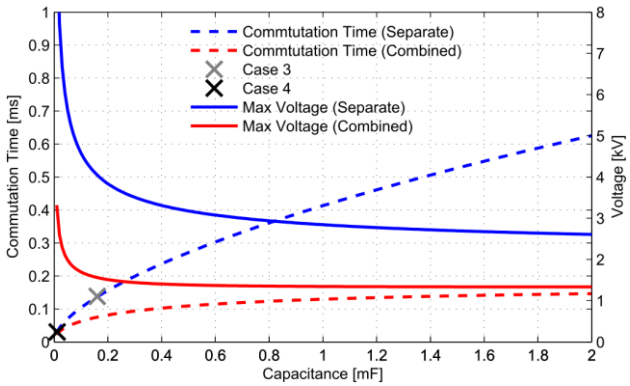


Fig. 17. Comparison of combined and separate cases.

The CFC voltage will start to increase naturally in the separated design as the diodes become forward biased and result in the CFC's capacitor charging, for which it must be designed.

IX. CONCLUSIONS

The integration of CFC functionality into hybrid circuit breaker designs can provide significant advantages. This concept has been verified using two independently developed simulations of a mixed converter topology 4-terminal VSC-HVDC grid.

The normal operation case study has shown that the CFC operation can be conserved when integrated in to the circuit breaker's design, and details of the control used in this work have been given.

The protection case study has shown that the circuit breaker's operation is not significantly affected by the LCS/CFC, as a reasonable commutation time is maintained, even with the increased primary branch capacitance. This has the added benefit of reducing the peak voltage across the LCS significantly. The breaker also provides over voltage protection for the CFC, as current is diverted away from the CFC during a dc fault transient. This voltage reduction should allow for a significant reduction in power losses, for the case study in this paper, the losses are reduced to 20% of the separate system. Further power losses reduction may be achieved if a LCS/CFC design that only requires single current direction control is considered.

The pre-charged nature of LCS/CFC's capacitance and the coupling between the two branches allows the limitations of the original LCS design to be overcome, potentially resulting in faster breaking times.

The CFC/LCS may also provide a useful power source for other power electronics that require a power source, such as the secondary branch of dc circuit breakers and a trickle charge mechanism for the mechanical switch actuators.

The limitations of the design are the re-start capability in the event the CFC is discharged. In such an event, there is a need to recharge the CFC's capacitance, which will cause a delay or a short disturbance in the DC line power flow.

Backup protection cannot immediately start to act once the fault is detected. This results in a delay equal to the commutation time.

There will also need to be a more complex controller that sits around the CFC controller to ensure that protection functionality is maintained under all scenarios.

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X. ACKNOWLEDGEMENTS

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XI. OVERSIZED IMAGE AND MATRICES

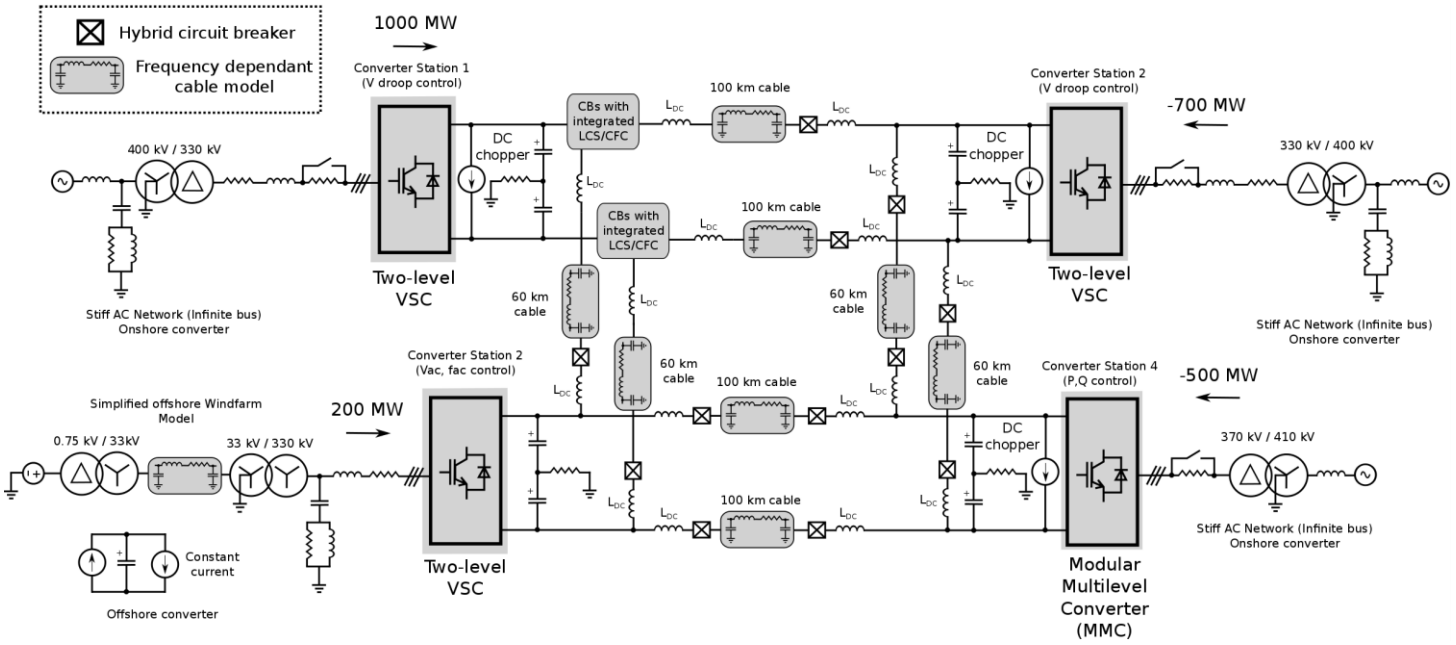

Fig. 18. Full PSCAD Simulation Model

$$\boldsymbol{A} = \begin{pmatrix} \frac{-k_d P_{base}}{C_1 {E_1}^2} & 0 & 0 & 0 & -\frac{1}{C_1} & -\frac{1}{C_1} & 0 & 0 & 0 \\ 0 & \frac{-k_d P_{base}}{C_2 {E_2}^2} & 0 & 0 & \frac{1}{C_2} & 0 & -\frac{1}{C_2} & 0 & 0 \\ 0 & 0 & \frac{-P_{30}}{C_3 {E_{30}}^2} & 0 & 0 & 0 & \frac{1}{C_3} & \frac{1}{C_3} & 0 \\ 0 & 0 & 0 & \frac{-P_{40}}{C_4 {E_{40}}^2} & 0 & \frac{1}{C_4} & 0 & -\frac{1}{C_4} & 0 \\ \frac{1}{L_{12}} & -\frac{1}{L_{12}} & 0 & 0 & \frac{-R_{12}}{L_{12}} & 0 & 0 & 0 & \frac{1-D}{L_{12}} \\ \frac{1}{L_{14}} & 0 & 0 & -\frac{1}{L_{14}} & 0 & \frac{-R_{14}}{L_{14}} & 0 & 0 & \frac{-D}{L_{14}} \\ 0 & \frac{1}{L_{23}} & -\frac{1}{L_{23}} & 0 & 0 & 0 & \frac{-R_{23}}{L_{23}} & 0 & 0 \\ 0 & 0 & -\frac{1}{L_{43}} & \frac{1}{L_{43}} & 0 & 0 & 0 & \frac{-R_{43}}{L_{43}} & 0 \\ 0 & 0 & 0 & 0 & \frac{D_0 - 1}{C} & \frac{D_0}{C} & 0 & 0 & 0 \end{pmatrix}$$

$$\boldsymbol{B} = \begin{pmatrix} \frac{1}{C_1 E_{base}} & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{C_2 E_{base}} & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{C_3 E_{30}} & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{C_4 E_{40}} & 0 \\ 0 & 0 & 0 & 0 & \frac{-E_0}{L_{12}} \\ 0 & 0 & 0 & 0 & \frac{-E_0}{L_{14}} \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{I_{12} + I_{14}}{C} \end{pmatrix} \qquad (18)$$