Optimal Inductor Current in Boost DC/DC Converters Regulating the Input Voltage applied to Low-Power Photovoltaic Modules

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***Abstract*— In energy-harvesting applications, inductor-based switching dc/dc converters are usually employed to regulate the operating voltage of the energy transducer and to transfer the harvested energy to a storage unit. In such a context, this paper analyses the optimal inductor current of the converter that leads to maximum power efficiency. This is evaluated assuming a low-power photovoltaic (PV) module connected to a boost dc/dc converter operating in burst mode so as to reduce the switching losses. The theoretical analysis and the experimental results reported herein prove that this optimal inductor current does not depend on the power generated by the PV module provided that the control circuit is powered from the output, but it does on the output voltage level of the storage unit. Experimental tests with a commercial boost dc/dc converter show that the use of this optimal inductor current provides up to 10% increase in efficiency.**

***Index Terms*— Boost converter, burst mode, DC/DC converter, efficiency, energy harvester, photovoltaic module.**

I. Introduction

ALTHOUGH switching dc/dc converters are generally employed to regulate their output voltage, they can also be used to regulate their input voltage, which is of interest in energy harvesters that power, for instance, the nodes of a wireless sensor network in smart cities and buildings. In the first case, the dc/dc converter is placed between the energy source (e.g. a battery) and the electronic circuitry (e.g. sensors, amplifiers, microcontrollers and/or transceivers) with two objectives: (i) to power the electronics with a stable supply voltage, and (ii) to transfer the energy from the battery to the electronics in an efficient way. In the second case, the dc/dc converter is placed between an energy transducer (e.g. a PV module) and a storage unit (e.g. a rechargeable battery) with again two goals: (i) to maintain the operating voltage of the energy transducer around its maximum power point (MPP) [1], and (ii) to transfer the energy from the transducer to the storage unit efficiently.

For dc/dc converters regulating their output voltage, the control strategy applied to the switching transistors is selected according to the output power demanded by the electronic circuitry. Under light-load conditions (i.e. for load currents of a few mA), which is quite usual in sensor nodes, the well-known pulse-width modulation (PWM) is not recommended because the fixed switching frequency causes significant switching losses and, hence, reduces the efficiency [2]. Such efficiency can be increased by dynamically adjusting the gate driving voltage [3], the size of the switching transistors [4,5], and the number of active phases in multiphase dc/dc converters [6]. Another way to improve the efficiency is the use of a hybrid control whereby the converter operates in PWM at heavy loads, but it switches to a variable-frequency mode at light loads so as to reduce the switching losses. A first example of that is the pulse-frequency modulation (PFM) where the switching frequency is scaled down with the load current. Constant [7] or adaptive [8] on-time, and constant peak inductor current [9] are two common control techniques based on PFM. A second example is the burst mode (BM) where the transistors are cyclically switched on and off at a fixed frequency (the same as in PWM) during an active period, but they are permanently in off-state during an inactive period, which becomes longer as the load current decreases [10]. During the active period, it is advisable to transfer the energy from the battery to the electronics at an optimal value of inductor current that can offer an efficiency increase of 10% [11].

For dc/dc converters regulating their input voltage in energy harvesters, the selection of the control strategy does not depend on the output power, but on the input power provided by the energy transducer. Converters operating in PWM have been proposed for medium- and high-power PV modules [12, 13], but other modulations are more appropriate for low input power levels (e.g. for subwatt PV modules) in order to reduce the switching losses, as also happens when regulating the output voltage. For instance: (i) a PFM control with a switching frequency that is scaled down with the PV current [14], and (ii) a BM control with an inactive period that increases as the PV current decreases [15, 16, 17]. The power processing circuits in [15, 16, 17] employed a commercial dc/dc converter (LT1303 [18], MAX1675 [19], and MAX1795 [20]) that adjusted the inductor current around 1 A, 0.5 A, and 0.25 A during the active period, respectively. However, the value of that current was not selected in terms of efficiency

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maximization, as proposed in [11] for the regulation of the output voltage.

This paper focuses on dc/dc converters operating in BM and regulating their input voltage. At the input, we assume a low-power energy transducer modelled by a DC current source, such as a PV module [12], that must operate around its MPP; the maximum power point tracking (MPPT) method that determines the MPP voltage is out of the scope of this work and can be found elsewhere [1, 12-17, 21]. On the other hand, at the output, we assume rechargeable batteries that are charged through the dc/dc converter. Following the method suggested in [11], which was applied to dc/dc converters regulating their output voltage, this paper aims to improve the power efficiency of the converter by selecting an optimal value of the inductor current employed to transfer the energy from the transducer to the batteries. Such a case requires a novel study of the dc/dc converter because the independent input/output variables are not the same as in [11]. Whereas in [11] these variables were the output power (voltage and current) demanded by the load and the input voltage provided by the battery, here these are the input power (voltage and current) generated by the energy transducer and the output voltage provided by the battery. Furthermore, in comparison with [11], this paper also contributes with the following. First, two scenarios are considered and compared: control circuit powered from either the input or the output. Second, the concept of optimal inductor current is experimentally proved for dc/dc converters having different levels of fixed, conduction and switching losses. And third, experimental results of efficiency when a low-power PV module operating at its MPP is connected to a dc/dc converter operating at its optimal inductor current are reported and discussed.

II. Operating Principle

A power processing circuit for a PV module based on a synchronous boost dc/dc converter is shown in Fig. 1. The converter relies on an inductor (L) and two power MOSFET transistors (MN and MP). The corresponding gate control signals (v_{c1} and v_{c2}) are generated by a control circuit with two loops [13]: (i) a voltage loop that monitors the input voltage (v_{in}) using a comparator with a hysteresis of $\pm V_{hys}$ and with a reference voltage (V_{in}) equal to the MPP voltage determined by a MPPT controller [1], and (ii) a current loop that monitors the inductor current (i_L) by either a shunt resistance in series with L or the voltage drop across MN or MP. At the input of the converter, the PV module provides a DC current (I_{in}) and has a high-value input capacitor (C_{in}) in parallel that temporarily stores the energy. On the other hand, the output of the converter is connected to a rechargeable battery in parallel with an output capacitor (C_{out}) that filters out the high-frequency components of the output current. Assuming no losses, the average output current injected to the battery is $V_{in}I_{in}/V_{out}$, where V_{out} is the DC voltage level of the battery.

The input voltage (v_{in}) in Fig. 1 is regulated around the desired DC voltage (V_{in}) by operating in BM. This operating principle involves two stages (inactive and active) that last $t_{inactive}$ and t_{active}, respectively, and an overall duty cycle

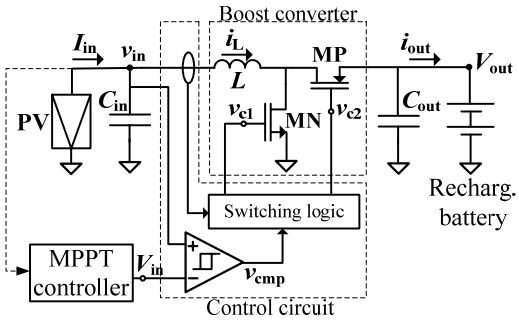


Fig. 1. Power processing circuit for a PV module based on a synchronous boost dc/dc converter.

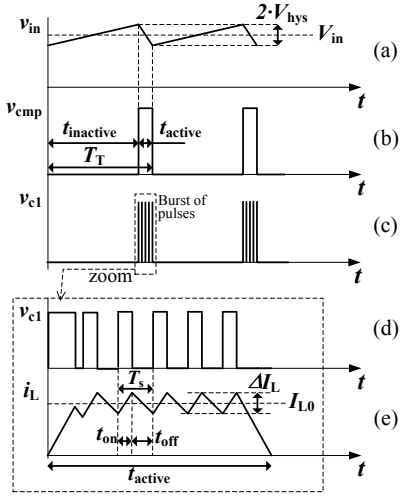


Fig. 2. Waveforms of interest from the circuit in Fig. 1 operating in BM-CCM.

$D_T = t_{active}/T_T$, where $T_T = t_{inactive} + t_{active}$, as shown in Figs. 2(a) and 2(b). In the inactive stage, the converter is deactivated (i.e. MN and MP are off) and I_{in} charges C_{in}, thus increasing v_{in}. When $v_{in} = V_{in} + V_{hys}$, the comparator output (v_{cmp}) changes to a high logic level and brings the converter to the active stage. Then, the energy accumulated in C_{in} is transferred to the output and v_{in} decreases. When $v_{in} = V_{in} - V_{hys}$, v_{cmp} toggles to a low logic level, the converter is deactivated and the process starts again. This operating principle based on initially storing the energy in C_{in} is very appropriate for low-power PV modules since (i) the converter remains inactive most of the time, which reduces the power losses, and (ii) C_{in} provides an operating voltage equal to the MPP voltage, which ensures a good impedance matching with the equivalent impedance of the PV module regardless of the operating conditions of the converter in active mode. Power processing circuits without a high-value C_{in} where the converter is always activated and the impedance matching is carried out by adjusting the duty cycle of the switching transistors [22] are more appropriate for medium- and high-power PV modules.

In order to transfer the energy from the input to the output during the active stage, a burst of on/off pulses under PWM control is applied to the gate of the transistors, as shown in Fig. 2(c) and with more details in Fig. 2(d) for v_{c1}; v_{c2} is the same as v_{c1} but with some dead time between them to prevent cross conduction of the transistors. As represented in Fig. 2(d),

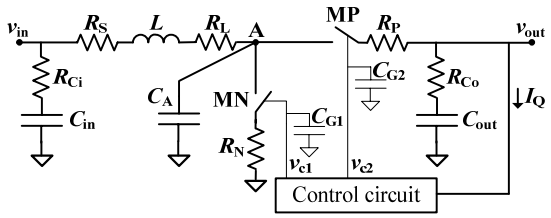


Fig. 3. Equivalent circuit model for the analysis of power losses in the circuit shown in Fig. 1.

v_{c1} has an on-time (t_{on}), an off-time (t_{off}), a switching period T_s (= t_{on} + t_{off}), a switching frequency f_s (= $1/T_s$) and a duty cycle D (= t_{on}/T_s). During t_{on} (MN on, MP off), the energy previously accumulated in C_{in} is stored in L and i_L increases, whereas during t_{off} (MN off, MP on), the energy accumulated in L is transferred to the output and i_L decreases. A current-programmed mode control in continuous conduction mode (CCM) is assumed so that i_L has an average of I_{L0} and a ripple of ΔI_L, as shown in Fig. 2(e). In such an operating mode, we have $D = 1-\eta V_{in}/V_{out}$, η being the efficiency. The optimal value of I_{L0} to carry out such energy transfer at maximum efficiency is analyzed next considering the main power losses.

III. Theoretical Analysis

The power efficiency of the circuit in Fig. 1 is theoretically analyzed using the same equivalent circuit model proposed in [11] and represented in Fig. 3. This circuit includes the parasitic resistance (R_L, R_{Ci}, R_{Co}, R_N, and R_P) of the main components (L, C_{in}, C_{out}, MN, and MP, respectively), and the parasitic capacitance (C_A, C_{G1}, and C_{G2}) of the main nodes (node A, gate of MN and MP, respectively); R_S is a shunt resistance employed in some dc/dc converters to sense i_L. Moreover, the control circuit has a current consumption of $I_{Q,a}$ in active mode and $I_{Q,i}$ in inactive mode, where $I_{Q,i} << I_{Q,a}$.

The optimal inductor current is theoretically found in two different scenarios that take into account the trade-off between conduction losses and gate-driving losses at different gate-driving voltages [3]. First, we assume that the control circuit is powered from the output, as shown in Fig. 3. This involves a high gate-driving voltage (i.e. V_{out}) that decreases the on-resistances of MN and MP and, hence, the conduction losses. Second, we consider that the control circuit is powered from the input. In such a case, the gate-driving voltage is lower (i.e. V_{in}) and, therefore, losses related to the charge-discharge process of C_{G1} and C_{G2} are also lower.

A. Control circuit powered from the output

Table I summarizes the power losses (fixed, conduction, and switching losses [11]) present in Fig. 3 in both active and inactive modes when the control circuit is powered from the output. In active mode, the equivalent parasitic resistance is $R_{eq,a} = R_{Ci} + R_S + R_L + R_N D + (R_P + R_{Co})(1-D)$. This is assuming that i_L is mostly provided by C_{in} since $I_{L0} >> I_{in}$, and that the current through MP is much higher than the average output current injected to the battery. In inactive mode, the equivalent parasitic resistance is $R_{eq,i} = R_{Ci} + R_{Co}\left(V_{in}/V_{out}\right)^2$,

TABLE I
Power Loss Components of the Circuit in Fig. 3 When the Control Circuit Is Powered from the Output

Power losses	Active mode	Inactive mode
Fixed	$V_{out} I_{Q,a}$	$V_{out} I_{Q,i}$
Conduction	$R_{eq,a} I_{L0}^2$ [a]	$R_{eq,i} I_{in}^2$
Switching	$f_s\left(C_{eq} V_{out}^2 + V_{out} I_{L0} t_c\right)$	0

[a] The RMS value of i_L is approximated to I_{L0} since $\Delta I_L < I_{L0}$ [23].

which assumes that the current extracted from C_{out} is $V_{in}I_{in}/V_{out}$. The capacitances C_{G1}, C_{G2}, and C_A are lumped in one equivalent capacitance, $C_{eq} = C_{G1} + C_{G2} + C_A$, because they have the same charging voltage (i.e. V_{out}) when the control circuit is powered from the output. As for the switching losses caused by the voltage-current overlap in MN, t_c is the average of the turn-on and turn-off transition times.

The overall power losses in active and inactive modes ($P_{L,active}$ and $P_{L,inactive}$, respectively) can be calculated by adding the three components indicated in Table I. Then, the average power losses over a whole period (i.e. T_T in Fig. 2) can be expressed and approximated (assuming $P_{L,active} >> P_{L,inactive}$) as

$$\begin{aligned} P_L &= P_{L,active} D_T + P_{L,inactive}\left(1-D_T\right) = \\ &\left(P_{L,active} - P_{L,inactive}\right) D_T + P_{L,inactive} \approx P_{L,active} D_T + P_{L,inactive} \end{aligned} \quad (1)$$

Since the charge accumulated in C_{in} in inactive mode is equal to that extracted from C_{in} in active mode, we have $I_{in} t_{inactive} = \left(I_{L0} - I_{in}\right) t_{active}$ and then D_T can also be written as I_{in}/I_{L0}. Using this relation in (1), the efficiency can be estimated as

$$\begin{aligned} \eta = \frac{P_{in} - P_L}{P_{in}} = 1 - \frac{1}{V_{in}} \Bigg[& R_{eq,a} I_{L0} + \frac{V_{out} I_{Q,a} + C_{eq} V_{out}^2 f_s}{I_{L0}} \\ & + V_{out} t_c f_s + \frac{V_{out} I_{Q,i}}{I_{in}} + R_{eq,i} I_{in} \Bigg] \end{aligned} \quad (2)$$

where P_{in} is the input power defined as $V_{in}I_{in}$. From (2), the higher V_{in} and/or the lower V_{out}, the higher the efficiency, as in [11]. The effects of I_{in} depend on which of the last two terms inside the brackets predominates. If we assume capacitors with a low equivalent series resistance (ESR), the last term in (2) is negligible and then η should increase with increasing I_{in}.

The efficiency predicted by (2) strongly depends on the selected value of I_{L0}. According to the first term inside the brackets corresponding to conduction losses in active mode, η decreases with increasing I_{L0} at high values of I_{L0}. However, according to the second term corresponding to fixed losses and switching losses due to C_{eq} in active mode, η increases with increasing I_{L0} at low values of I_{L0}. Therefore, there is a

maximum of efficiency at a certain value of I_{L0} that can be calculated from (2) by equating $\partial\eta/\partial I_{L0}$ to zero, thus resulting in

$$I_{L0,opt} = \sqrt{\frac{V_{out} I_{Q,a} + C_{eq} V_{out}^2 f_s}{R_{eq,a}}} \tag{3}$$

which is independent of both I_{in} and V_{in} and, hence, of the power generated by the energy transducer, but it increases with increasing V_{out}. Replacing (3) in (2) yields the maximum efficiency

$$\eta_{max} = 1 - \frac{1}{V_{in}} \left[2\sqrt{R_{eq,a} \left(V_{out} I_{Q,a} + C_{eq} V_{out}^2 f_s \right)} + V_{out} t_c f_s + \frac{V_{out} I_{Q,i}}{I_{in}} + R_{eq,i} I_{in} \right] \tag{4}$$

B. Control circuit powered from the input

Table II summarizes the power losses in both active and inactive modes when the control circuit is powered from the input. In comparison with Table I, we have three main changes: (i) fixed losses are lower since they depend on V_{in} instead of V_{out}; (ii) conduction losses in active mode are caused by a higher parasitic resistance, $R'_{eq,a} > R_{eq,a}$, because the on-resistances of MN and MP are higher; and (iii) switching losses due to the charge-discharge process of the gate capacitances, $C_G = C_{G1} + C_{G2}$, are lower since the gate voltage swing is lower. Following now the same procedure explained in Section III.A, we can find a new expression for the efficiency, the optimal value of I_{L0} and the maximum efficiency defined in (5), (6), and (7), respectively.

$$\eta' = 1 - \frac{1}{V_{in}} \left[R'_{eq,a} I_{L0} + \frac{V_{in} I_{Q,a} + f_s \left(C_G V_{in}^2 + C_A V_{out}^2 \right)}{I_{L0}} + V_{out} t_c f_s + R_{eq,i} I_{in} \right] - I_{Q,i} / I_{in} \tag{5}$$

$$I'_{L0,opt} = \sqrt{\frac{V_{in} I_{Q,a} + f_s \left(C_G V_{in}^2 + C_A V_{out}^2 \right)}{R'_{eq,a}}} \tag{6}$$

$$\eta'_{max} = 1 - \frac{1}{V_{in}} \left[2\sqrt{R'_{eq,a} \left[V_{in} I_{Q,a} + f_s \left(C_G V_{in}^2 + C_A V_{out}^2 \right) \right]} + V_{out} t_c f_s + R_{eq,i} I_{in} \right] - I_{Q,i} / I_{in} \tag{7}$$

In comparison with (2), the efficiency resulting from (5) is expected to be higher at low values of I_{L0} due to lower fixed and gate-driving losses, but lower at high values of I_{L0} due to higher conduction losses, as shown in Fig. 4. Comparing (3) and (6), we also realize that $I'_{L0,opt} < I_{L0,opt}$. Furthermore and unlike what happens in (3), now $I'_{L0,opt}$ depends on V_{in} and, hence, on the operating point of the energy transducer. This means, for a PV module, that $I'_{L0,opt}$ should be tuned at each irradiance and temperature level so as to achieve the maximum efficiency of the power processing circuit

TABLE II
POWER LOSS COMPONENTS OF THE CIRCUIT IN FIG. 3 WHEN THE CONTROL CIRCUIT IS POWERED FROM THE INPUT

Power losses	Active mode	Inactive mode
Fixed [a]	$V_{in} I_{Q,a}$	$V_{in} I_{Q,i}$
Conduction	$R'_{eq,a} I_{L0}^2$ [b]	$R_{eq,i} I_{in}^2$
Switching	$f_s \left(C_G V_{in}^2 + C_A V_{out}^2 + V_{out} I_{L0} t_c \right)$	0

[a] It is assumed the same quiescent current considered in Table I.
[b] The RMS value of i_L is approximated to I_{L0} since $\Delta I_L < I_{L0}$ [23].

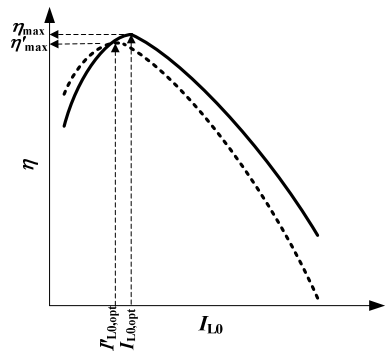


Fig. 4. Efficiency versus I_{L0} when the control circuit is powered from either the output (in continuous line) or the input (in dashed line).

Neglecting power losses due to $I_{Q,i}$, which are expected to be the lowest, (4) and (7) can be compared through the terms inside the square root defined in (8) and (9), respectively.

$$\text{Term 1} = R_{eq,a} \left(V_{out} I_{Q,a} + C_{eq} V_{out}^2 f_s \right) \tag{8}$$

$$\text{Term 2} = R'_{eq,a} \left[V_{in} I_{Q,a} + f_s \left(C_G V_{in}^2 + C_A V_{out}^2 \right) \right] \tag{9}$$

In order to compare these terms, we propose to express, in a first approximation, the parasitic resistances as $R_{eq,a} \approx R_A + k / V_{out}$ and $R'_{eq,a} \approx R_A + k / V_{in}$, where R_A is a resistive component independent of the gate-driving voltage due, for instance, to L, C_{in}, and C_{out}, whereas k is a constant that depends, among others, on the dimensions of MN and MP. Using these, the difference between (8) and (9) can be expressed as

$$\Delta = R_A I_{Q,a} \left(V_{out} - V_{in} \right) + R_A f_s C_G \left(V_{out}^2 - V_{in}^2 \right) - f_s k \left(\frac{V_{out}}{V_{in}} - 1 \right) \left(C_A V_{out} - C_G V_{in} \right) \tag{10}$$

If the value of R_A is significant, then the two first terms in (10) dominate, Δ becomes positive and, consequently, $\eta'_{max} > \eta_{max}$.

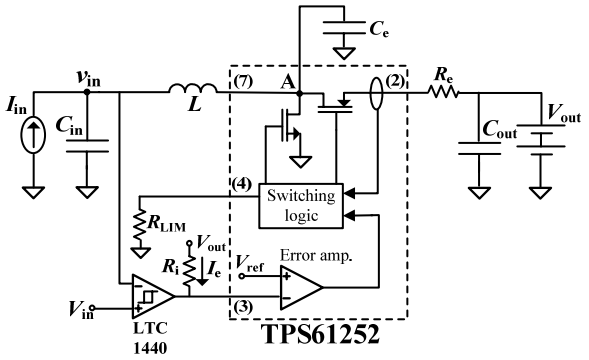


Fig. 5. Application circuit based on the TPS61252 employed to prove the concept of optimal inductor current; the numbers given in brackets are the pin numbers of the TPS61252.

However, if the value of R_A is low enough thanks to the use of capacitors and inductors with a very low ESR, the last term in (10) dominates. If we also have $C_A V_{out} > C_G V_{in}$, then Δ becomes negative and, therefore, $\eta_{max} > \eta'_{max}$, as represented in Fig. 4. In summary, if the components around the dc/dc converter are selected with a low enough parasitic resistance, it seems preferable to power the control circuit through the output so as to achieve a higher efficiency when operating at the optimal inductor current. Furthermore, in those conditions, the optimal value of I_{L0} does not change with the power generated by the energy transducer, which facilitates the control.

IV. Materials and Method

A commercial boost dc/dc converter, TPS61252 from Texas Instruments [24], has been employed to experimentally prove the concept of optimal inductor current. This converter has a control circuit powered from the output and its I_{L0} is adjustable from 100 to 1500 mA by an external resistor (R_{LIM}). The inductor current is measured during the off-time through the voltage drop across MP, and a valley current-mode control is applied that cleverly adjusts the valley current limit to achieve the desired average inductor current. In order to have the BM-CCM operation shown in Fig. 2, an external ultralow-power comparator, LTC1440 from Linear Technology, with $V_{hys} = 50$ mV was placed before the feedback (FB) input of the converter, as shown in Fig. 5. Using this circuit, when v_{in} becomes higher than the desired voltage, the comparator output changes to a low level, which brings the converter to active mode and, then, i_L is regulated around I_{L0}. Otherwise, when v_{in} becomes lower than the desired voltage, the comparator output toggles to a high level and the converter enters into inactive mode.

The circuit in Fig. 5 was tested using the operating conditions, instrumentation, and components indicated in Table III. The values of I_{in} and V_{in} were selected using as a reference a commercial ultra-thin low-power PV module, SP3-37 from PowerFilm, that will be under test in Section VI. At standard test conditions (STC) involving a solar irradiance of 1000 W/m^2, this PV module has a typical MPP current/voltage/power of 22 mA/3 V/66 mW, which is adequate to power, for instance, a microcontroller-based autonomous sensor [27]. Note that the maximum MPP current generated by the PV module (22 mA) is clearly lower than the minimum value of I_{L0} that can be regulated (100 mA), so the approximation indicated in Section III.A is valid. The input power was calculated as $V_{in}I_{in}$, whereas the average output power (P_{out}) was measured by a power analyzer, Yokogawa WT310, with a sampling frequency of 100 kSa/s and an update rate of 5 s.

With the aim of generalizing the concept of optimal inductor current to other dc/dc converters with different power losses, we also added some external components around the TPS61252, as shown in Fig. 5, so as to raise its fixed, conduction and switching losses. Fixed losses were increased by connecting a resistor (R_i) between V_{out} and the comparator

TABLE III
Operating Conditions, Instrumentation, and Components Employed to Test the Circuit Shown in Fig. 5

Variable or component	Value
I_{in}	5.5, 11, and 22 mA[(a)] provided by Agilent B2901
V_{in}	2.5, 2.75, and 3 V[(b)] provided by Agilent E3631A
V_{out}	4, 5, and 6 V[(c)] provided by Agilent E3631A[(d)]
L	2.2 µH, low-ESR
C_{in}	1 mF, tantalum, low-ESR
C_{out}	2×1 mF, tantalum, low-ESR

[a] Emulating the MPP current at 25%, 50%, and 100% of the irradiance at STC, respectively.
[b] Emulating the change of the MPP voltage due to changes of both irradiance and temperature [25]
[c] Emulating the different states of charge of four cylindrical NiMH secondary batteries in series.
[d] With a resistor in parallel to operate in the fourth quadrant [26].

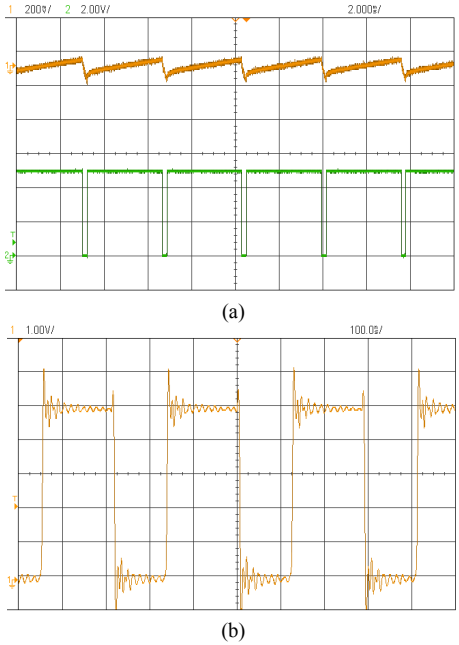


Fig. 6. From the circuit in Fig. 5, experimental waveforms of (a) the input voltage (channel 1 in AC coupling) and the comparator output (channel 2) for several active and inactive periods, and (b) the voltage at the switching node A within one active period.

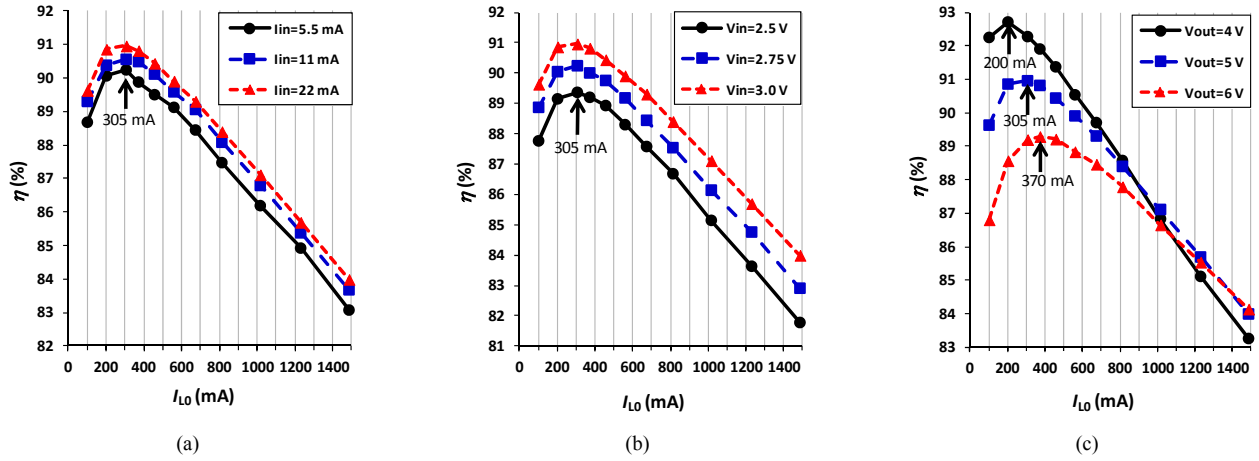


Fig. 7. Experimental efficiency versus I_{L0} for different values of (a) I_{in}, (b) V_{in}, and (c) V_{out}.

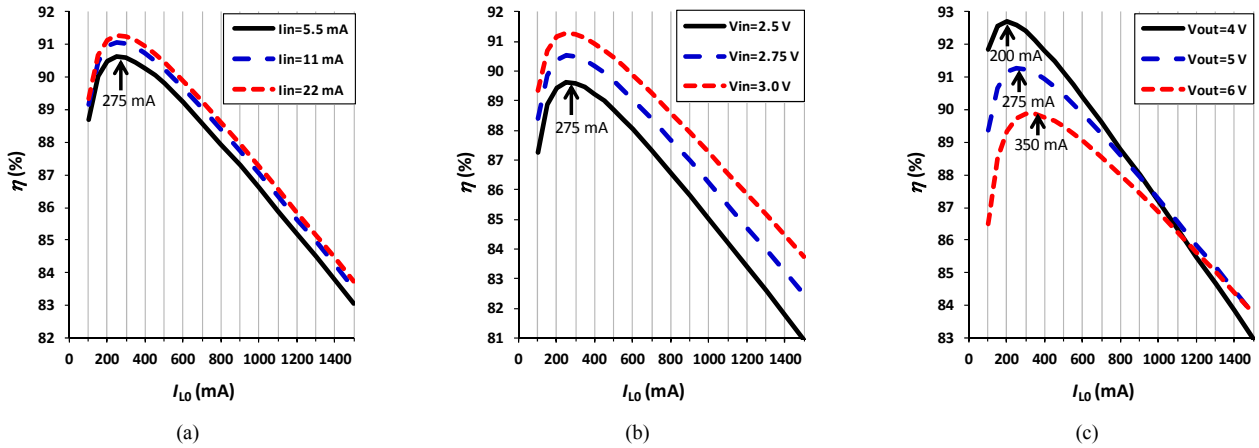


Fig. 8. Efficiency calculated from (2) versus I_{L0} for different values of (a) I_{in}, (b) V_{in}, and (c) V_{out}.

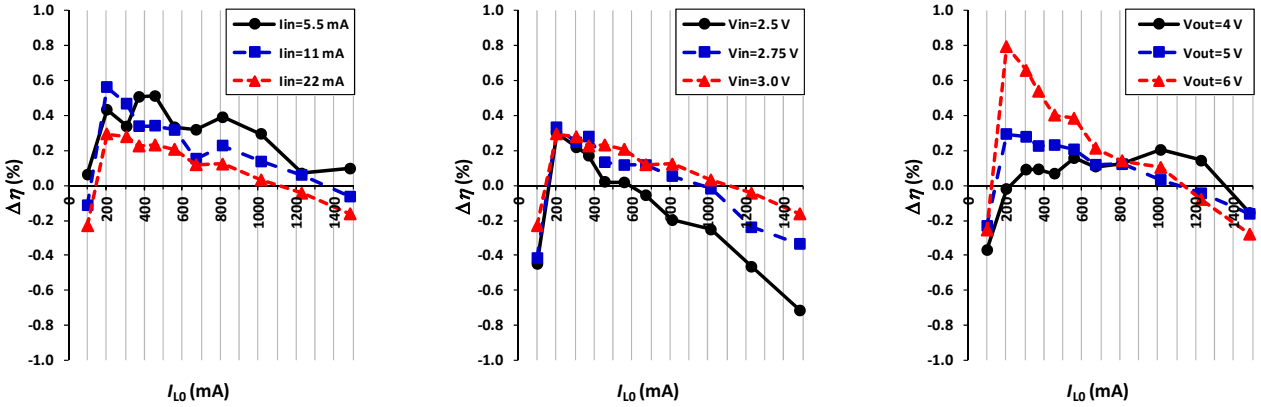
output, thus generating an extra current consumption of I_e ($= V_{out}/R_i$) in active mode. Conduction losses were increased by placing a resistor (R_e) at the output of the dc/dc converter, whereas switching losses were increased by connecting a capacitor (C_e) at the switching node A. All these tests were conducted at $V_{in} = 3.0$ V, $I_{in} = 22$ mA, and $V_{out} = 5.0$ V.

V. Experimental Results and Discussion

Before evaluating the efficiency of the circuit in Fig. 5, we tested its operating principle by monitoring the voltage waveform at the main nodes, as shown in Fig. 6 for $V_{in} = 3.0$ V, $I_{in} = 22$ mA, $V_{out} = 5.0$ V, and $I_{L0} \approx 305$ mA. Fig. 6(a) shows the input voltage and the comparator output for several active and inactive periods; the latter is the complementary of that represented in Fig. 2(b) because this signal is then inverted by the on-chip error amplifier. According to the comparator output, we had $D_T = 6\%$, which fairly agrees with that predicted by I_{in}/I_{L0}. On the other hand, Fig. 6(b) shows the voltage at the switching node A within one active period; this signal is also the complementary of that represented in Fig. 2(d) since it is inverted through MN. In Fig. 6(b) we measured $f_s = 3.5$ MHz, instead of the nominal value of 3.25 MHz, and $D = 44\%$, which agrees with that calculated by $1 - \eta V_{in}/V_{out}$ assuming $\eta = 91\%$ (reported later in Fig. 7). Furthermore, D was very stable during the active period, which means that the inductor current was well regulated around I_{L0}.

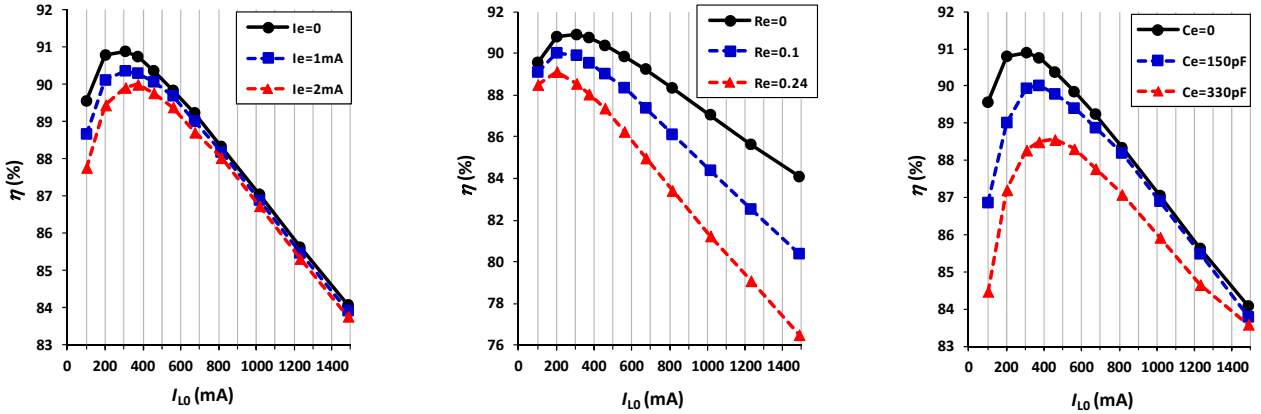
Fig. 7 shows the experimental results of efficiency versus I_{L0} for different values of (a) I_{in}, (b) V_{in}, and (c) V_{out}, using $I_{in} = 22$ mA, $V_{in} = 3.0$ V, and $V_{out} = 5.0$ V as default values. The higher the value of both I_{in} and V_{in}, the higher the efficiency, although the effects of the latter were clearly major. However, the higher V_{out}, the lower the efficiency. Such effects of I_{in}, V_{in}, and V_{out} on the efficiency agree with (2). Moreover, $I_{L0,opt}$ was independent of both I_{in} [Fig. 7(a)] and V_{in} [Fig. 7(b)], but it increased (from 200 to 370 mA) with increasing V_{out} [Fig. 7(c)], which was already predicted by (3). With respect to the case with minimum efficiency that was found at the maximum value of I_{L0}, the efficiency increased by 7%, 8%, and 10% in Figs. 7a, 7b, and 7c, respectively, when $I_{L0,opt}$ was applied.

In order to quantitatively evaluate the model proposed in Section III, the efficiency was also calculated from (2) and represented in Fig. 8 for the same operating conditions discussed before. Note that C_{eq} and t_c were unknown and were extracted by fitting (2) to a set of experimental results, and that R_N and R_P were assumed to be dependent on the gate-



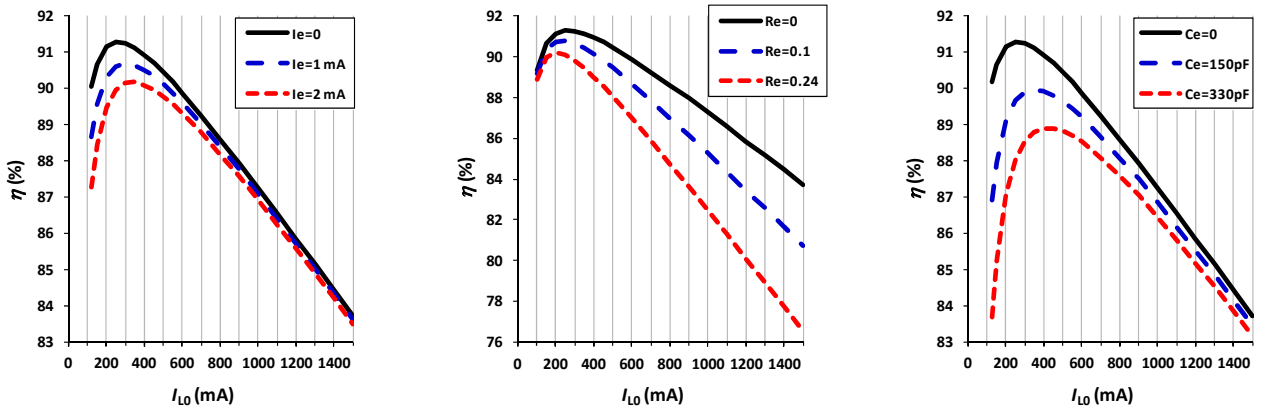
(a) (b) (c)

Fig. 9. Difference between the predicted (Fig. 8) and the experimental (Fig. 7) values of efficiency.



(a) (b) (c)

Fig. 10. Experimental efficiency versus I_{L0} for different values of (a) I_e, (b) R_e, and (c) C_e.



(a) (b) (c)

Fig. 11. Efficiency calculated from (2) versus I_{L0} for different values of (a) I_e, (b) R_e, and (c) C_e.

driving voltage of the transistors (i.e. V_{out}) in Fig. 8(c) [3,4]. The difference ($\Delta\eta$) between the predicted (Fig. 8) and the experimental (Fig. 7) values of efficiency is shown in Fig. 9. In most of the cases under test, $\Delta\eta$ is smaller than 0.5 %, which is small enough to consider the proposed model valid to estimate the efficiency of dc/dc converters regulating the input voltage in BM-CCM. Such a small discrepancy can be ascribed to limitations of: (i) the model, which disregards fixed losses due to the leakage current of transistors and capacitors, and switching losses due to the body diode of MP and to the inductor core; and (ii) the measurements, especially those performed by the power analyzer at low power levels.

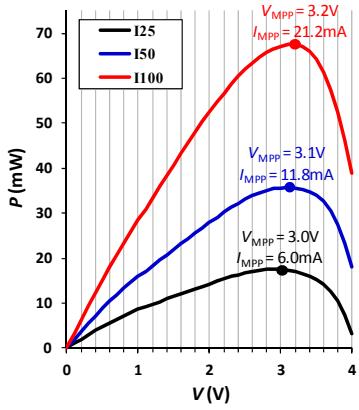
The experimental results of efficiency at other values of

power losses emulated by the external components are represented in Fig. 10. When the dc/dc converter was subjected to extra fixed losses through I_e (of 1 and 2 mA) or extra switching losses through C_e (of 150 and 330 pF), the efficiency decreased but especially at low levels of I_{L0}, as shown in Figs. 10(a) and 10(c), respectively. This is because, at low levels of I_{L0}, the converter remains longer in active mode and, therefore, the effects of both fixed and switching losses are higher. On the other hand, when the converter suffered from extra conduction losses through R_e (of 0.1 and 0.24 Ω), the efficiency also decreased but mainly at high levels of I_{L0} [see Fig. 10(b)] where conduction losses are more significant. Fig. 10 also shows that $I_{L0,opt}$ increases with increasing I_e and C_e, but decreases with increasing R_e, as predicted by (3). In the worst case tested [i.e. Fig. 10(b) with R_e = 0.24 Ω], the efficiency increased by 13% when $I_{L0,opt}$ was applied. For the same testing conditions, we also calculated the efficiency through (2) and the results (see Fig. 11) completely agreed with the experimental data shown in Fig. 10.

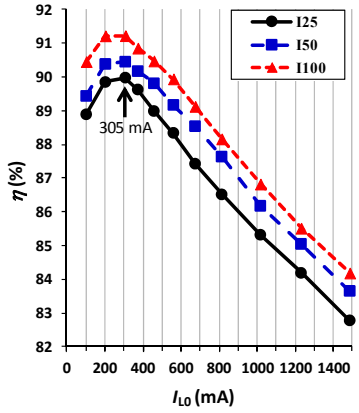
In a practical implementation, taking into account that the exact value of some variables involved in (3) or (6) can be unknown, the optimal value of I_{L0} can be automatically determined through a control algorithm, such as the perturb and observe method [17], carried out by a microcontroller. The basic idea would be to slightly perturb the value of I_{L0} and then observe how the output power changes, assuming the input power constant during the control cycle. If the output power increases, the perturbation should be kept in the same direction; otherwise, it should be reversed. For the TPS61252 under test, the value of I_{L0} could be perturbed using a digital potentiometer instead of R_{LIM} in Fig. 5. On the other hand, the output power could be observed by sensing: (a) the average output current via a shunt resistor and an amplifying low-pass filter [15,28], or (b) the increment of voltage across a small output capacitor connected in parallel with the main storage device that would be disconnected for a short and known time interval [29].

VI. Application to a Low-Power PV Module

The concept of optimal inductor current has been further proved using a commercial low-power PV module, SP3-37 from PowerFilm. This was first characterized under irradiance-controlled laboratory conditions to achieve the power-voltage (*P-V*) curve as follows. The PV module was subjected to three irradiance levels (identified as I25, I50, and I100) through a LED array, BXRA-C1202 from Bridgelux, powered at different DC currents and placed at 3 cm [17]. The levels I25, I50, and I100 approximately correspond to an irradiance of 250, 500, and 1000 W/m^2, respectively, in terms of power generated by the PV module at the MPP. At each irradiance level, the current generated by the PV module was measured at different applied voltages (from 0 V to 4 V in steps of 100 mV) using a source-measurement unit, Agilent B2901. The experimental results of such a characterization are represented in Fig. 12(a) showing the MPP at each irradiance level. As expected, the current (I_{MPP}) and the power at the MPP were quite proportional to the irradiance level, whereas the voltage (V_{MPP}) slightly increased with increasing the irradiance level.



(a)



(b)

Fig. 12. (a) Experimental *P-V* curves of the PV module under test for different irradiance levels. (b) Experimental efficiency of the circuit versus I_{L0} for different irradiance levels when the PV module operates at the V_{MPP} indicated in Fig. 12(a).

After characterizing the PV module, this was connected to the power processing circuit shown in Fig. 5 instead of the ideal input current source. Using the same methodology explained in Section IV, the efficiency of the circuit was measured at different values of I_{L0} and for the three irradiance levels indicated before. At each irradiance level, V_{in} in Fig. 5 was set to the V_{MPP} value indicated in Fig. 12(a) so as to extract the maximum power from the PV module. The experimental results of efficiency are shown in Fig. 12(b) for V_{out} = 5.0 V. Note that the efficiency increased with increasing the irradiance level. This is because the higher the irradiance, the higher the value of both V_{MPP} and I_{MPP} (and, hence, V_{in} and I_{in} in Fig. 5) and, therefore, the higher the efficiency, as shown before individually in Figs. 7(a) and 7(b). The resulting value of $I_{L0,opt}$, which was around 305 mA, was the same for the three irradiance levels. Accordingly, as previously suggested in Section III.A, the value of $I_{L0,opt}$ seems to be independent of the power generated by the energy transducer, thus facilitating the control strategy.

VII. Conclusion

This work has gone a step further in the field of power processing circuits based on switching dc/dc converters by proposing an optimal inductor current to carry out the energy transfer from a low-power energy transducer to a storage unit. If the control circuit is powered from the output, this optimal inductor current is independent of both the input voltage and the input current. Consequently, this optimal current does not depend on the power generated by the energy transducer, which has been experimentally proved using a commercial low-power PV module subjected to different irradiance levels. However, such a current depends on the output voltage, i.e. the voltage level of the output batteries. Experimental tests with a commercial boost dc/dc converter have shown that the use of this optimal inductor current provides up to 10% increase in efficiency. Therefore, this is a simple but effective way to improve the autonomy of sensor nodes powered by a low-power PV module.

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