Lithography Aware Regular Cell Design based on a Predictive Technology Model

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***Abstract*—As semiconductor technology advances into the nanoscale era, optical effects such as channel narrowing, corner rounding or line-end pullback are critical to accomplish circuit yield specifications. It is well-demonstrated that layout regularity reduces the increasing impact of process variations on circuit performance and reliability. The purpose of this paper is to present the layout design of a regular cell based on 1-D elements which reduces lithography perturbations (ALARC). We depict several undesirable lithography effects and how these effects determine several layout parameters in order to achieve the required line-pattern resolution.**

I. Introduction

Over the years, CMOS technology has not ceased to scale down and has enabled the production of increasingly complex products at lower cost, as Moore's Law predicted. However, deep sub-micron technologies has entailed an increase of the design-process interdependencies and systematic variations that are influencing both integrated circuit (IC) performance and yield [1]. In order not to jeopardize circuit quality, these variations must be mitigated or at least taken into account during the circuit and layout design stage to fully realize its potential.

In the nanoscale era, one major source of circuit performance degradation comes from lithography imperfections; printability becomes highly hampered and neighborhood-pattern dependent due to lithography tools are being pushed to operate at their resolution limit. This has led to hot-spots, line-end pull-back or poor Across Chip Line-width Variation (ACLV) among other undesirable perturbations. Resolution Enhancement Techniques (RETs) are currently used to correct pattern distortion and reduce variability. For instance, Optical Proximity Correction (OPC) and Phase Shift Mask (PSM) techniques are two examples of post-layout enhancement methods. However, existing design rules cannot guarantee a design that fully exploits the benefits of RETs since it is difficult to perform an efficient analysis of layout patterns during the design optimization stage.

As lithography advances into the 45nm technology node and beyond, a paradigm shift in design style is required to drive higher performance with smaller circuit features. Regular cell designs has emerged as an alternative to traditional 2-D standard cells toward a more lithography-friendly design style [2] [3] [4] [5] [6]. 2-D refers to layouts with jogged polygons, while regular or 1-D refers to a layout with parallel straight lines (in vertical or horizontal direction), with gaps (or commonly called cuts) as required to implement circuit functions. Thereby, using 1-D layout style several lithography induced perturbations can be dramatically decreased and manufacturability is enhanced due to the reduced number of geometry patterns and lithography interactions that must be analyzed. For instance, in [6] a similar regular strategy is proposed although the lithography constraints are not as precisely depicted as herein.

While the benefits for manufacturability of layout regularity have been clearly demonstrated [7], a regular design does not directly imply that all lithography imperfections have been eliminated. Hence, in order to model lithography perturbations and identify places in a layout where optical effects may affect functionality, we use a Calibre Litho-Friendly Design (LFD) rule deck [8] provided by North Carolina State University (NCSU) based on an open-source 45nm technology Physical Design Kit (PDK) [9]. This PDK uses a Predictive Technology Model (PTM) that provides customizable and predictive model files for future transistor and interconnect technologies. Note that in the provided LFD deck, only *active*, *contact*, *poly*, and *metal1* layers are currently supported, which correspond to the smallest features in this technology.

In [10], some litho-effects applied to conventional standard cells were discussed. The aim of our paper is to provide a more comprehensive outline on lithography-aware and regular cell design style. Thus, an adaptive lithography-aware regular cell design structure (ALARC) based on 1-D elements which reduces lithography perturbations is presented in this article.

The remainder of the paper is organized as follows. In section II insights on lithography-aware design style are provided. The characteristics of the ALARC design structure are outlined in section III. In section IV it is detailed how to build a common logic function (AND2 gate) using the ALARC structure. The paper concludes in section V providing some interesting future avenues of research.

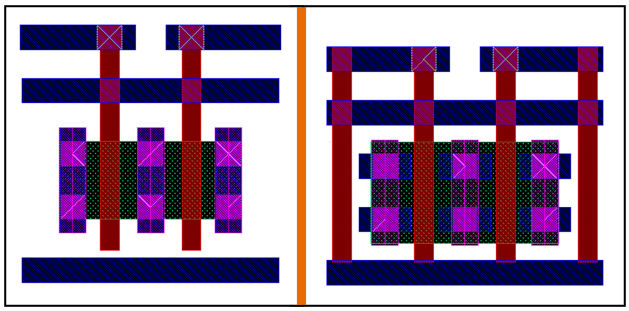
II. Lithography effects

As stated in the introduction, lithography effects determine cell layout style. In this section, this assertion is illustrated through lithography simulations, outlining the effects of some

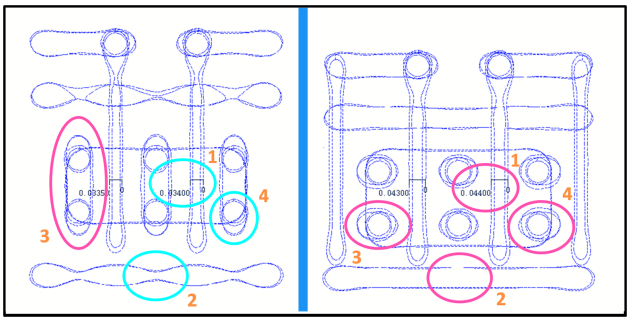
lithography perturbations and how to correct them or at least how to minimize their undesirable effects. Based on common layout situations where this optical effects are highlighted, the potential lithography constraints that have to be taken into consideration during the design stage to minimize lithography variations are here described.

A. Isolated Gates: Gate narrowing

At sub-wavelength transistor size with small Rayleigh k_1 lithography factor, the line-width is critically determined by its proximity to neighboring lines, in other words, the pattern density across the chip. This proximity might benefit or deteriorate the line-width of layers and thus causing the phenomenon commonly called across-chip line-width variation (ACLV) which results in systematic yield losses. Thereby, spacing between poly gates must be adjusted properly to reduce the ACLV. In this section, we analyze this feature from the point of view of isolation, more specifically, the poly line (gate) isolation problem which is in fact the most critical layer. Two cases might occur to consider that a gate is isolated: 1) gates that are not surrounded side by side by poly lines (transistors placed on the end of an active region) or 2) excessive pitch between contiguous poly lines. Both situations produce the gate narrowing phenomenon; the poly line width variation is highly incremented, producing a considerable width size reduction all along its length dimension and consequently the unwanted channel narrowing.



(a) Layout design



(b) Lithography

Fig. 1. (1) Left: No dummy lines employed; right: dummy lines utilized to reduce the gate narrowing effect (2) Undulating-line effect; (3) Line-end pullback; (4) Active region enclosure.

The gate narrowing problem can be solved by adding dummy poly lines. While the use of dummy elements may in principle imply a penalty in area, this is not necessarily the case when all lithography constraints are considered jointly (poly spacing restriction detailed in section II-C allows enough room to place the dummy poly lines). Hence, a dummy poly line has to be placed at both ends of each active region in order to avoid the undesirable gate narrowing. Note that the dummy poly lines are not placed in a continuous active region in order to give more flexibility to the gate ordering and because jogged oxide strips are not allowed in our regular design. Figure 1(a) depicts an example of a regular layout with and without dummy poly lines. Lithography simulations reveal that the width of isolated poly lines are reduced up to approximately 26% with respect of the desired poly line width (45 nm) when dummy lines are not employed, as it is highlighted in figure 1(b) (region 1). Note that from now on, all lithography figures have two drawn lines which represents the maximum and minimum lithography pattern expected. Finally, it must be stated that a dummy poly line can be shared by two consecutive active regions as illustrated in figure 4.

B. Source/Drain (SD) contacts: Proximity effect

The proximity effect is the lithography perturbation caused by lack of space between two elements in the same layer when one of them or both has a sharp shape. SD contacts are likely to suffer or cause this perturbation if spacing, size and placement of the required layers to create an SD connection (metal1, contact, via1 and optionally metal2 layers) are not adjusted properly. Figure 1 depicts two different regular strategies to connect the metal1 layer which evinces the proximity effect. On the left side of fig. 1(b) (region 2), it is shown a weakened metal line more likely to pinch due to the *undulating-line* effect. This perturbation affects the interconnect reliability causing either a broken wire or an increase on the expected wire resistance and thus the electrical behavior of devices might be off target. Increasing the spacing between sharp elements and other lines would alleviate this problem, but it would also produce an increase of area.

An alternative implementation is illustrated on the right side of fig. 1(a) that solves this perturbation. In this case, metal1 lines suffer from *line-end pullback* due to the proximity of metal1 lines from contiguous SD contacts, as illustrated in fig. 1(b) (region 3). Although both lithography perturbations might cause a systematic yield loss due to a size reduction of the expected pattern, in this case the *line-end pullback* is less aggressive than the *undulating-line* effect and lithography is still verified. Finally, observe that SD contacts must be properly enclosed by the active region in order to avoid them to fall outside the oxide strap. Thereby, the active region must be sufficiently extended all along the SD contact, except one edge thereof that can be minimally extended (5nm), as depicted in fig. 1(b) (region 4).

C. Poly contacts: Channel narrowing

The poly contacts are the only 2-D feature permitted in the design. This irregularity is mandatory because the poly channel is narrower than the poly extension needed to create

a contact. Note that this 2-D shape may cause a narrowing in the channel region whether the poly contact is not properly designed and placed. The channel narrowing effect increases the transistor threshold voltage and reduces its current driving capability. To maintain the desired channel length along the channel region the following guidelines must be considered.

Firstly, the shape of the poly contact enclosure should be rectangular, aligned with the poly shape and avoiding an abrupt change in poly width which causes *bottlenecking*. Figure 2 illustrates different poly shapes and different spacing between poly lines. The shape that achieves a lower gate narrowing is the enlarged poly enclosure with the extra small poly squares and 165 nm of poly spacing (shape *E*, *bottom*). In addition, you can see that the same shape but spaced 160 nm achieves similar and valid results. Eventually, note that it is up to the designer to decide where is the limit between area penalty and lithography accuracy.

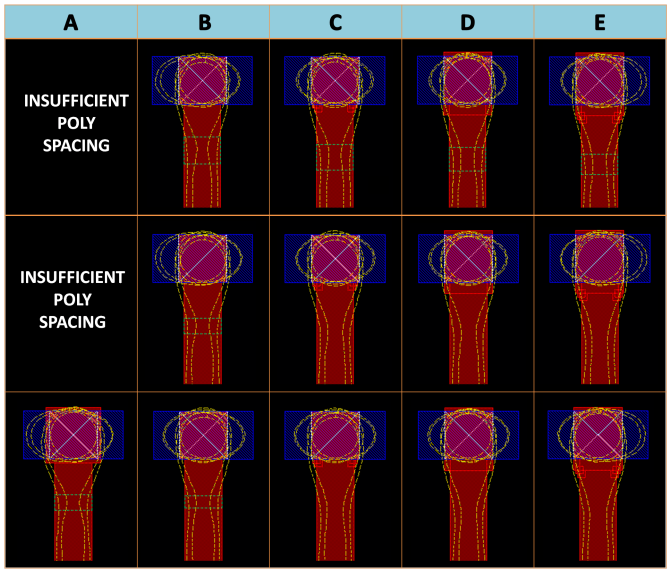
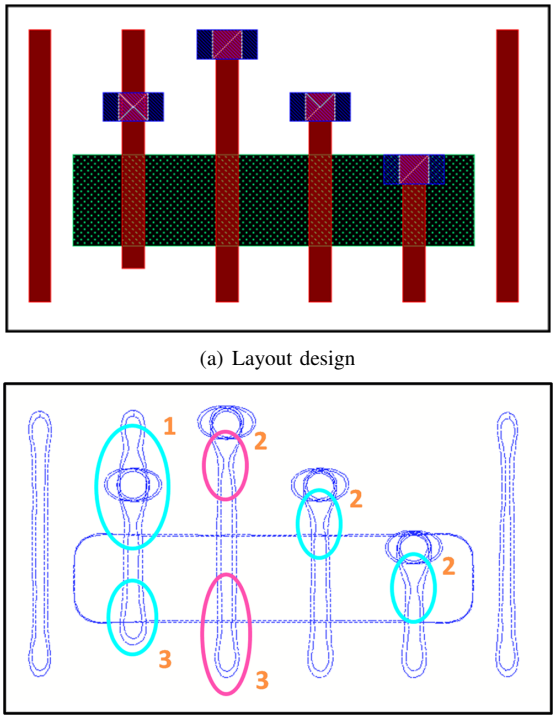


Fig. 2. Different types of poly enclosure. (Top) Spacing between contiguous poly lines: 155nm; (Middle) Spacing: 160nm; (Bottom) Spacing: 165nm. Rows are sorted from worse to best poly enclosure. Green squares indicate regions where the minimum lithography expected pattern is not verified.

Secondly, the number of poly contacts in the cell design must be minimized to diminish the number of poly irregularities. For instance, in case of dual-network topologies, the Euler-path method (or sub-Euler-paths) finds the optimum gate ordering to which the pull-up and the dual pull-down network have an identical ordering of input labels. Besides the advantage of simple routing of signals, and correspondingly, more compact layout area and smaller parasitic capacitance, both networks can share the same poly gate and hence only one poly contact will be necessary.

Thirdly, poly contacts are preferably placed on the ends of the poly gate to avoid the double narrowing effect; in that case, the narrowing would only affect toward one direction, as shown in figure 3 (region 1). Note that the priority on our design is to reduce the double narrowing effect, although this constraint can be omitted whether the routability is prohibitively difficult (excessive wire length or oversized cell area).



(a) Layout design

(b) Lithography

Fig. 3. (1) Double narrowing effect; (2) Channel narrowing perturbation; (3) Poly line-end rounding causing channel width variations.

Fourthly, though the previous irregularities are alleviated, they are not completely wiped out and therefore the poly contacts may still affect the channel region if they are not properly located. Therein lies the next constraint: the poly contact must be placed sufficiently far away from the active region so we can avoid the channel narrowing; a narrowing in the poly line is undesirable, but it is highly more harmful to have this irregularity inside the active region than outside. Thereby, moving the poly contacts further away from the diffusion strap we achieve a regular channel length (apart from random perturbations), as highlighted in fig. 3 (region 2). Finally, the poly gate end without a poly contact suffers from line-end rounding, as all the other layers does. Hence, the poly extension on the active area must be larger than the minimum specified by design rules, as shown in fig. 3 (region 3). Thereby, the channel length can be completely regular and voltage threshold variations can be minimized.

Take into account that some of these constraints are subjected to the technology employed herein and the lithography estimation tool used. Hence, the important idea to remark is that lithography determines the poly contact configuration. Thereby each designer must adjust these constraints (such as poly enclosure) to minimize litho-perturbations and maximize circuit yield.

D. Substrate contacts

Substrate contacts or polarization contacts are used to connect the bulk of transistors to the power supply. They are usually placed either on the power supply line or aligned to the active region. If the power supply is wide enough and the poly lines can be sufficiently spaced, placing them on the power supply line gives a more compact cell. Otherwise they can be placed in line with the active region, but this represents an increase in area. For instance, the minimum spacing needed to place a substrate contact between two poly lines is 190 nm in this technology. In case that spacing between poly lines would be less than 190 nm, which is actually our scenario, substrate contacts must be placed on the power supply lines. In this case, they should be located on places where poly lines do not overlap the power supply, otherwise poly lines should be shortened to allow more room for substrate contacts and consequently might cause a gate narrowing problem.

Note that to optimize the number of substrate contacts, they should be placed during the Place and Route (P&R) stage instead of during the cell design stage. Then, each time a cell is placed in the block field, the necessary polarization contacts will be added into each cell, considering those previously placed. Hence, the number of substrate contacts can be minimized, but the complexity of the P&R algorithm may increase.

III. Regular Cell design

Up to this point, we have seen different lithography constraints that must be considered jointly to minimize lithography perturbations. Furthermore, regular designs are characterized for having only unidimensional shapes. Therefore, an adaptive lithography-aware regular cell design structure (ALARC) that takes into account all the lithography features previously outlined is presented in this paper. Note that this design is still a prototype, probably more enhancements should be done to improve its yield, e.g., routability might require slight modifications on this design.

A. ALARC structure

In this section, the proper placement of each layer to minimize litho-complexity is described. Figure 4(a) illustrates an example of how the structure might look like. Note that depending on the function implemented, the number of lines of each layer and its sizing might vary, but the structure might look similar. In tables I and II the corresponding placement of each layer and its function is listed. The regular structure proposed in this paper has the following characteristics:

- All PMOS transistors lie in a single row near the top of the cell and all NMOS transistors lie in a single row near the bottom of the cell (this is akin to the single-row layout style of standard cells) or vice versa. According to the distribution selected, that distribution will be utilized for cells placed in an odd block row and for even block rows PMOS and NMOS transistors will be swapped. Thereby, a power supply line can be shared by two cells and the block area can be reduced.

TABLE I
Horizontal Layers

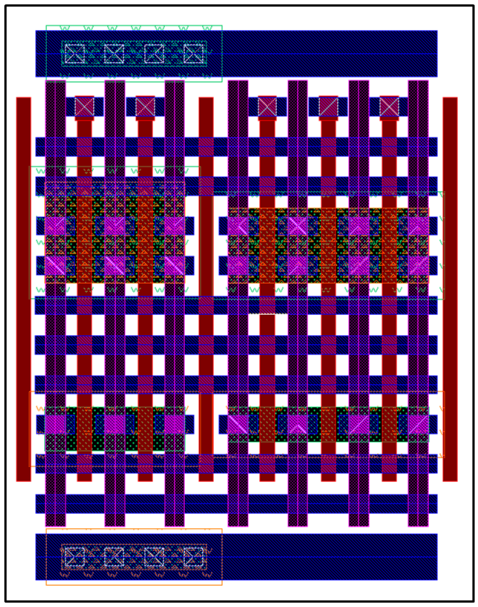
Type	Color	Acronym	Function
metal1	Blue	PST	Power supply layer (wider)
metal1	Blue	MT_1-MT_{NT}	Intra/inter-cell connections
oxide	Green	ODP	PMOS transistors
metal1	Blue	MM_1-MM_{NM}	S/D contacts & cell connections
oxide	Green	ODN	NMOS transistors
metal1	Blue	MB_1-MB_{NB}	Intra/inter-cell connections
metal1	Blue	PSB	Power supply layer (wider)

TABLE II
Vertical Layers

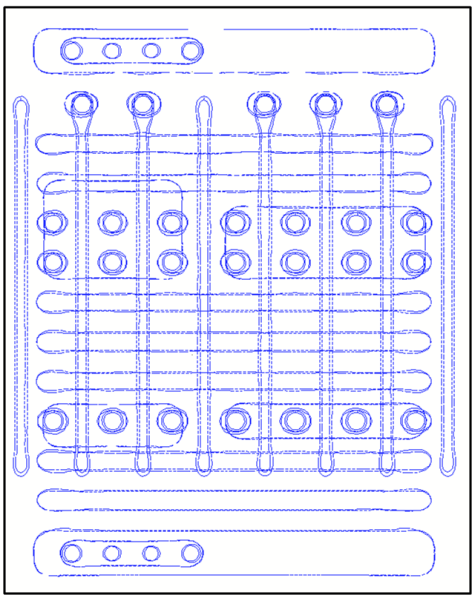
Type	Color	Acronym	Function
poly	Red	DL_1-DL_{ND}	For each OD, 2 dummies (2 OD can share 1 DL)
metal2	Purple	MV_1-MV_{NV}	Cell connections (aligned to S/D contacts)
poly	Red	G_1-G_{NP}	Poly gate per transistor

- Poly lines can be extended outside the cell to perform inter-cell connections in case routability is prohibitive. This choice might produce two side effects: 1) double narrowing or 2) poly narrowing if neighboring poly lines are not extended.
- Dummy lines can also be employed for connections, though the lithography is better with a metal connection.
- Active regions have a variable length, i.e., a different number of transistors. Other regular designs [3], utilize a fixed regular length, but herein it depends on the logic function aiming to increase the area utilization and avoid unwanted unused transistors.
- Variable number of horizontal metal1 lines in order to give more flexibility to the cell design and furthermore to decrease the overall area of the block design. Therefore, each cell will be designed reducing as much as possible the number of metal1 lines and thus the cell area can be minimized.
- Metal1 and metal2 line-width is minimized in this structure, but there is still room for wider connections without area penalization.
- Inputs can be placed either on the top of the cell or on the bottom as needed. However, inputs should never be placed on the closest metal1 lines from the active region to avoid channel narrowing as detailed in section II-C.

Note that the design is via-configurable, in other words, any function can be created selecting the proper vias (any via1 can be placed in the intersection of metal1 and metal2 layers) and cutting the metal lines as necessary. Finally, observe that lithography simulations clearly reveal that implementing functions following the ALARC structure, the channel narrowing has been corrected and the channel specifications are verified, as can be seen from figure 4(b).



(a) Layout design



(b) Lithography

Fig. 4. Adaptive lithography-aware regular cell design structure (ALARC).

B. Cell size

Cell size is determined by both horizontal and vertical pitch of the most restrictive layers. To minimize the across-chip line-width variation (ACLV) of the most critical line-width, the physical gate length, horizontal pitch is ascertained by the minimum poly spacing that verifies gate line-width specifications. More specifically, the lithography constraint that defines the poly pitch (PO_{pitch} = 215 nm) is the trade-off between proximity and isolation between poly lines described in sections II-A and II-C. Hence, the cell width (W_{cell}) is determined by the following expression

$$W_{cell} = \sum_{i}^{N_{OD}} (PO_{pitch}) * (N_i + 1) + PO_{width}$$

$$PO_{pitch} = PO_{spacing} + PO_{width}$$

where N_{OD} is the number of PMOS or NMOS active regions in the cell (both are equal), N_i the number of transistors per region, $PO_{spacing}$ is established to 165 nm in order to consider all lithography constraints previously explained and PO_{width} is the poly width which is fixed to 50nm in the layout design stage (design rule deck) to finally obtain the 45nm required for the technology employed herein.

On the other hand, the vertical pitch is determined by the number of metal1 lines employed to create the intra-cell connections. Furthermore, the spacing between metal1 lines is determined by the minimum distance to place two VIA1s or two contacts in consecutive rows or columns ($VIA1_{pitch}$). Thus, the cell height (H_{cell}) can be derived from the expression stated next

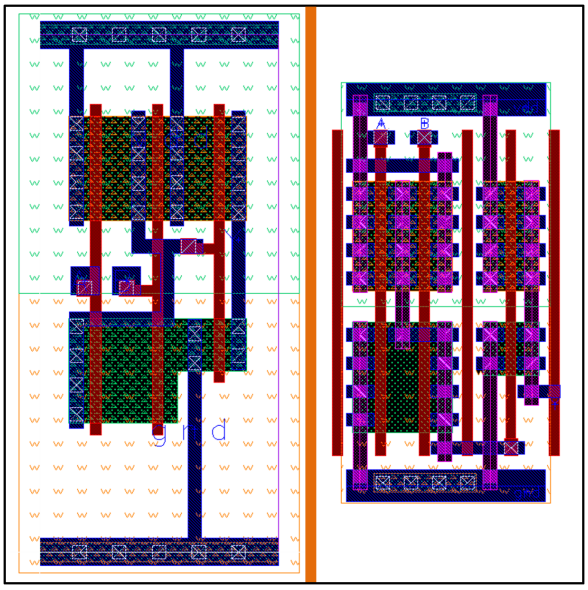
$$H_{cell} = N_{M1} * via1_{width} + (N_{M1} + 1) * via1_{spacing} + 2 * W_{PS}$$

where N_{M1} is the number of metal1 lines in the cell (NT, NM and NB metal1 lines as detailed in table I), W_{PS} is the metal1 power supply width, $via1_{width}$ (65 nm) and $via1_{spacing}$ (75 nm) are the width and spacing of via1 respectively. Thereby, each metal1 line (except for power supply) added to the layout implies a cell height increase of 140 nm.

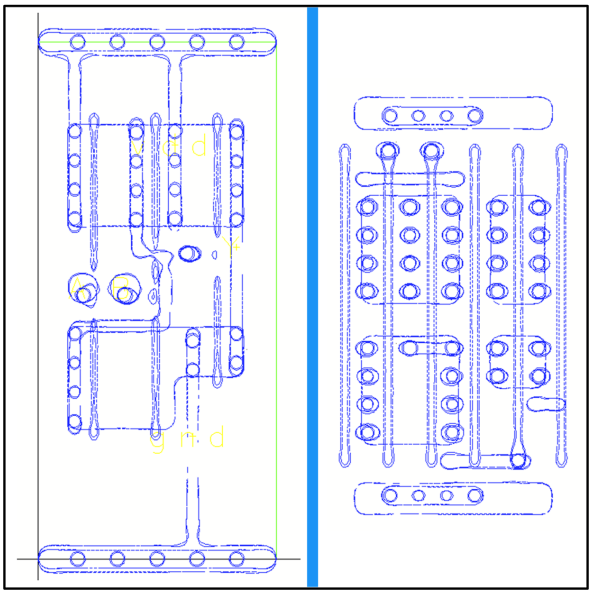
IV. AND2 EXAMPLE

In this section, we analyze the impacts of mapping a typical logic function (AND2) in our proposed regular structure comparing it with an AND2 standard cell provided by [9]. Lithography simulations clearly reveal that the AND2 standard cell is infeasible in terms of lithography; besides the undulating-line effect suffered by metal1 connections, the poly gate lines are not only narrowed, but they are split.

Observe that a regular design does not directly imply an area penalty compared to an standard cell configuration as stated by [6]. However, restricting the layout design with all lithography constraints can lead to an infeasible signal routing or to a prohibitive cell area. Hence, the designer must decide up to which point lithography limits layout design and thereby which and where lithography constraints can be omitted. Obviously, the across-chip line-width variation (ACLV) is enhanced as more restrictions are considered, but there should always be a trade-off between routability, lithography and performance parameters such as timing response or power. For instance, we can allow irregularities on the back-end of line layers, permitting a bended oxide strap and thus the cell width could be diminished. Particularly, allowing a jogged diffusion strap in our AND2 design, the cell width would be decreased. Furthermore, taking profit of the versatility of the structure proposed herein, P&R algorithms can benefit from having different implementations of the same logic function



(a) Layout design: (Left) AND2 Standard Cell; (Right) AND2 ALARC Cell



(b) Lithography: (Left) AND2 Standard Cell; (Right) AND2 ALARC Cell

Fig. 5. AND2 Logic Gate.

with different metal connections, different input placement or different logic synthesis. Thereby, the P&R algorithm would decide which implementation outperforms routability.

Finally, observe that cells might have extra white-space (extra metal1 rows unused) because of different transistor size or different number of metal1 lines required. The extra spacing should not be placed randomly, because it can help to reduce capacitance between contiguous metal lines, therefore the extra spacing may be placed where the parasitic capacitance is much considerable. Another option is to utilize the extra white-space to create double interconnections which increases the reliability of the circuit in case that a VIA fails (i.e. is like having a multi-VIA configuration) or to increase metal width and so the resistance between two points in the circuit can be reduced.

V. Conclusions and Future Avenues of Research

In this paper it is illustrated how lithography perturbations determine layout design even for regular litho-friendly design styles. For instance, we have seen how the trade-off between proximity and isolation between poly lines fixes the cell width. Hence, we have proposed a regular structure (ALARC) that tackles lithography difficulties, i.e., channel narrowing or line-end rounding. Finally, a common logic gate, AND2, is implemented to show how the ALARC structure can be mapped into a function and it is proved that our design outperforms line-pattern resolution compared to an AND2 standard cell.

Note that the proposed structure is just a prototype and further enhancements are predicted in the near future. More specifically, we aim to adjust our structure considering trade-offs between timing, power, area, routability congestion and lithography. Another future avenue of research is to analyze the P&R which implies the employment of other metal layers and thus these layers should be allocated properly in order to maintain regularity on the circuit block.

In conclusion, take into account that the results provided here are particular to the technology employed herein and also they may differ for a real technology, hence for each technology, parameters such as spacing or poly enclosure should be adjusted properly.

Acknowledgment

The research leading to these results has received funding from the European Community's Seventh Framework Programme (FP7/2007-2013) under grant agreement n 248538 (Synaptic project).

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