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Phase noise degradation of LC-tank VCOs due to substrate noise and package coupling

Miguel A. Méndez, Diego Mateo, Xavier Aragonès, Jose Luis González

Electronic Engineering Department, UPC, Jordi Girona, 1-3 Campus Nord – C4, 08034 Barcelona, Spain
mamendez,mateo,aragones,jlgonzalez@eel.upc.edu

Abstract:

The present work addresses the investigation of phase noise degradation of LC-tank VCOs due to realistic digitally originated substrate noise. The dominant mechanisms by which this noise is coupled to the output of the oscillator due to the substrate and the package are analyzed, indicating that both noise at low frequencies and at high frequencies around the oscillation fundamental significantly degrade phase noise.

1. Introduction

During the last years, the impact of substrate noise on radio frequency (RF) mixed-signal ICs has received much attention. The market trend towards low-cost and high-performance communication systems has motivated the appearance of baseband+radio single chip integration solutions for various wireless communication standards. One important challenge in this type of circuits is the minimization of noise coupling from the digital section to the analog/RF circuits. Several works have addressed substrate noise coupling to various types of RF blocks, being the low noise amplifiers (LNA) [1,2,5] and the voltage controlled oscillators (VCO) [3] the most studied due to their higher noise sensitivity and their relevance in the receiver chain. In this paper the impact of digitally originated substrate noise on an LC-tank oscillator is investigated. Since we use a real digital circuit, the whole spectrum of substrate noise is affecting the VCO, providing original results compared to previous work that considered only pure sinusoidal tones. Furthermore, the chip where the oscillator and the digital aggressor are integrated is packaged in a 64 pins CQFP package, which allows including in the investigation the package effects on noise coupling.

The test chip and the substrate noise generated by the digital circuit are presented in section 2. In section 3 experimental results about noise impact on the VCO phase noise are presented, and the digital circuit to VCO noise coupling is analyzed with the help of SubstrateStorm [4] and SpectreRF. In section 3 it is shown also how the local substrate nodes and the analog ground of the VCO receive the same substrate noise even though the substrate is of high resistivity type. Section 4 contains a study of the various mechanisms that couple the noise from the VCO substrate and to its output. Finally, the conclusions are contained in section 5.

2. Test chip and digital noise description

The test chip, shown in Figure 1, contains a 2.65 GHz differential LC-tank VCO and a digital circuit with independent power supplies. It has been fabricated in a conventional four metals two poly 0.35 μm CMOS process on a high-ohmic substrate. The power supply voltage of both digital and RF sections is 3.3 V. The test chip also contains a pair of sensors to measure noise at the digital power supply nodes and at a substrate access point indicated with a circle in Figure 1. The sensor is described in [7]. Its transfer function has been previously characterized and it is used to calibrate the measurements.

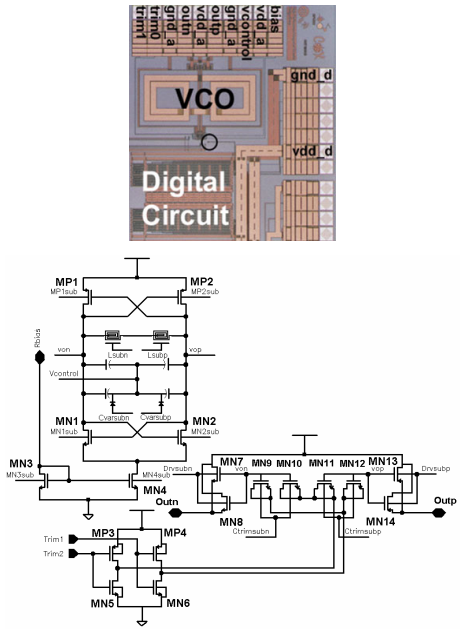

Figure 1: Test chip photograph and VCO schematic.

2.1 Voltage controlled oscillator

The VCO is based on a differential complementary LC oscillator. Fine tuning is achieved through a pair of varactors. Two switchable capacitors implemented with MOS transistors are added to each output to digitally coarse-tune the oscillation frequency. The tuning curves are shown in Figure 2. Biasing is provided through a current mirror that is adjusted with an off-chip resistor. A pair of open drain stages output the signal off-chip,

where a pair of bias-tees are used to bias and terminate the oscillator outputs.

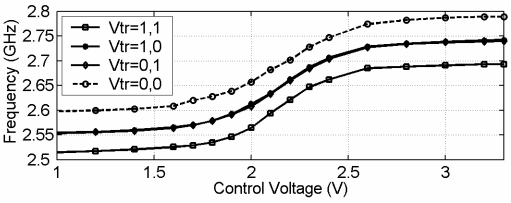

Figure 2: VCO tuning curves.

2.2 Digital circuit

The digital circuit is composed of 48 chains of tapered buffers terminated on a 1pF capacitor all driven by the same external input clock with period T_{clk}. The number of simultaneously switching chains can be varied. In this way the amount of generated digital noise can be controlled. The digital circuit generates a periodically varying substrate noise signal, which spectrum is [5,6]:

$$S_{sub}(f) = \left|H(f)\right|^2 \cdot \frac{1}{T_{clk}^2} \sum_{i=-\infty}^{+\infty} \left| \overline{I_{dd}}\left(\frac{m}{T_{clk}}\right) \right|^2 \delta(f - \frac{m}{T_{clk}}), \quad (1)$$

This discrete spectrum has harmonics separated by the digital clock frequency (f_{clk}). Its envelope depends upon the cyclic digital switching current waveform in the frequency domain $\overline{I_{dd}}(f)$ and the transfer function from the digital power supply nodes to the substrate node of interest *H(f)* [6]. Figure 3 shows an example of the substrate spectrum when all the tapered buffers blocks are active for a f_{clk} = 10 MHz (left axis) and the simulated *H(f)* (dashed line, right axis). The substrate noise transfer function depends on the substrate+chip+package parasitics. In the test chip this results in several resonance peaks. The first one, due to the chip+substrate+package RLC resonance, is located at 104 MHz. There are two more resonances due only to package parasitics at 1 and 4 GHz, which are relevant since they raise the level of substrate noise at high frequencies around the VCO fundamental frequency. Substrate noise will otherwise fall beyond the circuit resonance with -40dB/decade of slope. The high frequency resonances are due to a parasitic coupling path of digital noise to the analog ground through the package.

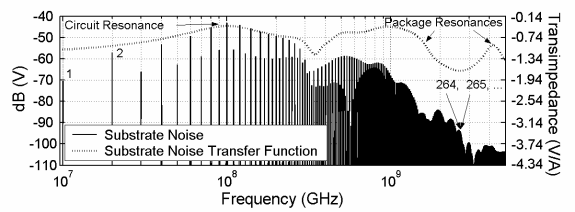

Figure 3: Substrate noise spectrum and substrate noise transfer function.

3. Substrate noise coupling and phase noise

When the digital circuit is activated, the phase noise of the VCO degrades significantly. Figure 4 shows an example of this effect for a f_{clk} = 10 MHz. Many spurs appear at the sidebands of the oscillator fundamental frequency (f_0). These spurs are originated in the substrate noise coupled to the analog ground and to each of the VCO active devices and passives local substrate nodes. The various spurs appearing in Figure 4 are labeled according to its origin. Group B come from low frequency substrate noise harmonics up-converted from close to DC to close to f_0 due to indirect AM to FM modulation. Group A and group C come from high frequency substrate noise harmonics converted from around f_0 to phase noise sidebands. The detailed investigation of the origin of these spurs is addressed in section 4. The spacing between the spurs of each group is exactly equal to the digital clock frequency f_{clk}. The subindexes correspond to the original harmonic index of the substrate noise spectrum, as shown in Figure 3 (i.e. B_1 is an spur due to the first harmonic of the substrate noise at f_{clk} and C_{265} is an spur due to the substrate noise harmonic located at $265 \cdot f_{clk}$). It has been determined experimentally that group A spurs frequency is unaffected by changes in the oscillator frequency. Group B spurs are displaced the same amount of frequency that f_0 when it is varied, and group C spurs are displaced twice this quantity. Indeed, spurs A_i and C_i form a pair of correlated sidebands symmetrically place around f_0, and each B_i has a symmetrical sideband due to the same substrate noise harmonic.

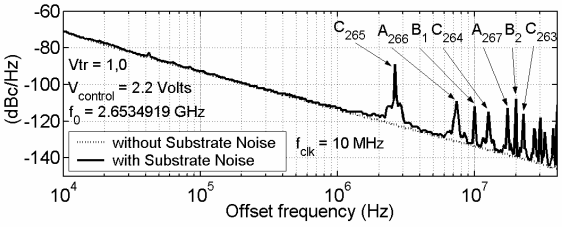

Figure 4: Differential output VCO phase noise degradation due to substrate noise.

The investigation on how substrate noise arrives to the VCO circuit is made by means of simulation. The digital circuit is substituted by a macromodel that efficiently captures the relevant characteristics of the digital circuit from the noise generation point of view [8] whereas the VCO is described at transistor level in a netlist extracted from the layout, including a substrate model obtained with SubstrateStorm. This model includes the VCO and the digital circuit, taking into account any connection between the substrate of the chip and the board ground through the package. A detailed model of the package obtained from an electromagnetic analysis of its 3D structure is used. SpectreRF autonomous Periodic Steady State (PSS) analysis is used to find the time-varying solution of the VCO plus digital aggressor circuit, where the digital switching current and the substrate noise it generates are considered small signals. Subsequently PAC and PXF analysis are used to calculate the noise coupling from the digital circuit to various substrate nodes and the analog ground of the VCO. The results indicate that substrate noise at the bulk node of each of the NMOS (MN*i*) is very similar to noise coupled to the analog ground. The substrate noise coupled to the bulk

nodes of the PMOS transistors (MP*i*) and the varactor substrate node resort much smaller due to the filtering effect of the n-well to substrate capacitance. This is illustrated in the transient simulation for a single clock cycle shown in Figure 5. From this figure it is clear that the substrate underneath the VCO circuit can be approximated by a single node connected to the analog ground, even though the high-ohmic substrate used. Substrate noise arrives almost with the same amplitude and phase to all the VCO substrate nodes and the analog ground. This is partially due to the guard ring connected to the analog ground that surrounds the VCO layout, which effectively shorts the VCO substrate connections with a very low impedance to ground.

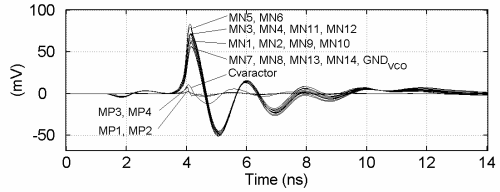

Figure 5: Substrate noise waveforms at different VCO substrate nodes and at analog ground.

4. Spur generation mechanisms.

There exists an extensive literature about phase noise due to physical noise sources in LC oscillators. A recent review can be found in [9]. In the case of substrate noise, instead of many un-correlated noise sources at every device or lossy component of the oscillator, there is a single noise source. This noise source is originally located in the digital circuit and has the form of a current source[1] (the digital switching current), but it can be moved to the VCO analog ground (or any other substrate node in the VCO) by using a linear transformation (the substrate noise transfer function). In the remaining of this section we investigate how noise components originally around DC and f_0 produce phase noise. We don't consider noise around $2f_0$ since at this high frequency for realistic digital circuits used in RF System-on-Chips the substrate noise content is negligible.

4.1.1 Mechanisms of phase noise degradation

Phase noise at the output of the LC-tank VCO can be due to noise sources in the resonator, noise sources in the differential pair and noise sources in the biasing transistor. Substrate noise can be coupled to the varactor and inductors of the resonator tank through the parasitics capacitances. However, due to the symmetry of the circuit, all this noise appears mostly in the common mode and is suppressed by the differential operation of the circuit. Similarly, any fluctuation of the threshold voltage in the differential pair due to substrate noise will appear in the common mode. The dominant impact mechanism of substrate noise is the AM modulation of the bias transistor current due to substrate noise coupled to its ground terminal. This is confirmed by the SpectreRF PSS+PXF analysis and from the experimental results shown in Figures 6 and 7. In this way, substrate noise can be treated as a noise current source in parallel with the bias transistor, with a power spectral density given by (1) scaled by the squared small signal bias transistor transconductance g_m^{bias}.

4.1.2 Bias noise induced by substrate noise

Since substrate noise modulates the gate-to-source voltage of the bias transistor, its effects on the output can be analyzed considering the VCO as a single balanced mixer that multiplies the bias current by the switching function of the differential pair (set by the differential current) [9]. PSS simulation allows determining that the first terms of the mixing function in our VCO are:

$$m(t) \simeq \left(\frac{2}{\pi}\right)\left(\sin(w_0 t) - \frac{1}{6}\sin(2w_o t) + \frac{1}{3}\sin(3w_o t)...\right). \quad (2)$$

The first term will bring low frequency substrate noise harmonics to close to the fundamental as two correlated AM sidebands at an offset equal to its original location. However, spurs of group B can not be explained by this mechanism alone, since these AM sidebands will be suppressed by the limiting mechanism of the oscillator. There are, however, other indirect AM to FM conversion mechanisms that explain the origin of spurs of group that are investigated in the next sub-section.

The second term of (2) moves high frequency substrate noise harmonics originally at $w_0 - w_m$ to a single sideband in the VCO output at $w_0 + w_m$ (the corresponding correlated sideband goes to $3w_0 - w_m$ and is filtered by the tank). This single sideband can be decomposed into two AM and two PM sidebands symmetrically placed around f_0, each containing half the power of the original single sideband. The upper PM sideband at $w_0 + w_m$ is the origin of spurs of group C, and the lower PM sideband at $w_0 - w_m$ is the origin of spurs of group A. Since there are also substrate noise harmonics at $w_0 + w_m$, C spurs appear too in the lower sideband of the oscillator and their paired A spurs appear too in the upper sideband of the oscillator fundamental. Using the same analysis for bias transistor noise impact on phase noise detailed in [10], the single sided phase noise due to spurs of group C (or A) is found to be:

$$\mathcal{L}^{C,A}\{w_m\} = S_{sub}(w_0 \pm w_m)\left(\frac{g_m^{bias}}{12\sqrt{2}I_B}\right)^2\left(\frac{w_0}{2Qw_m}\right)^2, \quad (3)$$

where I_B is the bias current and Q the tank quality factor . Since the phase noise is a single sided measurement, we need to take into account A and C spurs that appear in only one sideband. The sign + in S_{sub} corresponds to group A spurs and the sign – corresponds to group C spurs. This expression is verified experimentally by measuring the phase noise of one spur of group C for increasing bias current and for two control voltages. These measurements are compared with the expression $\left(g_m^{bias}/I_B\right)\left(w_0/2Qw_m\right)$ normalized to its minimum value,

[1] Note that we are considering the usual case where digital switching noise is the dominant source of substrate noise.

and the results are plotted in Figure 6, where a good agreement between (3) and the measurements is shown.

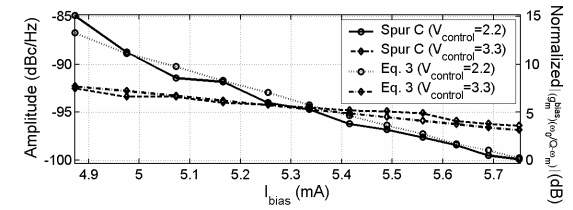

Figure 6: Spurs of group C dependence on bias current.

4.1.3 AM to FM conversion of substrate noise

Tuning voltage supply sensitivity and capacitance modulation due to bias noise resort in FM modulation of the VCO output and have been reported to be the responsible of bias transistor flicker noise upconversion [10, 11, 12]. Both effects are due to fluctuations of the biasing current, and therefore, may also be produced by substrate noise coupled to the analog ground of the VCO. From basic FM theory the phase noise around the first harmonic of the VCO output due to a substrate noise harmonic at w_m, which will produce a group B spur, is:

$$\mathcal{L}^{B}\{w_m\} = S_{sub}(w_m)\left(\frac{d\omega_0}{dI_B}\right)^2 \left(g_m^{bias}\right)^2 \left(\frac{1}{2w_m^2}\right), \qquad (4)$$

where $\left(d\omega_0/dI_B\right)\cdot g_m^{bias} = -K_{GND}$ can be understood as a frequency deviation index equal to the negative of the VCO oscillation frequency sensitivity to changes in ground voltage. This equation is verified experimentally by measuring K_{GND} as explained in [3] for various tuning voltages. Results are plotted in Figure 7 where it is shown that group B spurs amplitude closely follows $|K_{GND}|$, validating the analytical model of (4).

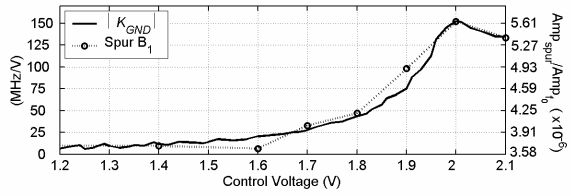

Figure 7: Spurs of group B dependence tuning voltage.

5. Conclusions

Previous works [3] reported that low frequency substrate noise produces phase noise spurs at the output of LC-tank VCOs due to resistive coupling between the injection point and the VCO ground followed by FM modulation. In this paper we have shown that for realistic substrate noise spectrum, there appear additional spurs close to the VCO fundamental due to high frequency substrate noise harmonics. The substrate noise harmonics around f_0 are transformed into phase noise at the VCO output due to mixing with the second harmonic of the differential pair output current. In our case the problem is aggravated because resonances due to the package in the substrate noise transfer function from the digital circuit to the VCO local substrate nodes and ground raises the level of the substrate noise around f_0. This underlines the importance of package coupling in substrate noise impact on RF circuits. Two analytical expressions have been derived that explain the mechanisms of phase noise degradation due to substrate noise harmonics close to DC and around f_0, respectively. Both expressions have been verified experimentally. From these expressions it is possible to derive strategies to minimize substrate noise impact on VCO phase noise. Concerning high-frequency substrate noise that originates spurs A and C, besides engineering the package and pin assignment to move package resonances to other frequencies that would reduce the substrate noise level around f_0, the minimization of the second order harmonic of the mixing function will reduce its conversion to phase noise sidebands. This can be achieved by optimizing the VCO differential current waveform symmetry. Concerning the up-conversion of low frequency substrate noise due to indirect FM modulation, the same techniques used to minimize bias transistor flicker noise up-conversion may be used [12].

6. Acknowledgements

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