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Novel UHF passive rectifier with Tunnel FET devices

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Abstract—The increase of the losses in UHF passive rectifiers with Tunnel FET devices at large RF AC amplitudes are mainly due to the high reverse current inherent in this technology when subjected to high reverse bias conditions. In this work, a new UHF passive rectifier circuit is proposed, with the purpose of reducing the reverse current suffered by Tunnel FET devices at large RF AC amplitudes. Compared to the differential-drive rectifier, the proposed topology is shown to improve the output voltage and power conversion efficiency at similar RF voltage/power conditions as well as the transmission distance for RFID applications.

Keywords—Energy Harvesting; Passive Rectifier; RFID; Tunnel FET; UHF; Ultra-low Power.

I. INTRODUCTION

Several low-power applications benefit from the surrounding radiated energy in order to power their circuits. RFID tags and biomedical implants are examples of radio-frequency (RF) powered circuits that can be placed in areas of difficult access, and therefore, the constant replacement of their batteries is undesired. However, the low power conversion efficiency (PCE) demonstrated by UHF passive rectifiers at low RF input power levels (below -30 dBm) along with the limited available RF power from the surrounding environment constrains the operation range of these circuits in both distance of operation and computational capability [1-7].

At such low power levels, the losses in the front-end rectifiers are mainly due to the high forward losses at each diode/transistor present in the rectification process. Schottky diodes present low threshold voltage values (0.2-0.3 V) and for this reason they are often found in Dickson multiplier structures [1]. However, the incompatibility with CMOS processes has resulted in the use of diode-connected MOSFET configurations for IC applications [2].

In order to increase the range of available power operation in conventional passive rectifiers, higher power efficiencies are required, especially at sub-mW levels of the available RF power, where the use of current MOSFET technology is shown to be inefficient [3-6]. Conventional transistors applied in the front-end rectifiers of RF powered circuits are characterized by a minimum subthreshold-slope swing (SS) of 60 mV/dec (at room temperature). This characteristic limits the current at low voltage values in the front-end rectifier.

The steep-slope Tunnel FET (TFET) device has been shown to increase the efficiency of passive rectifiers at lower RF power levels compared to the use of FinFET technologies [6-7]. For example, an RF passive rectifier circuit with TFETs can improve the PCE up to 70 % at -39 dBm, compared to the 7 % achieved with the FinFET technology at similar load conditions [6]. However, when the p-i-n structure of the TFET device (Fig. 1) is largely reverse biased (both $V_{GS}$ and $V_{DS}$ negative for n-type TFET, and $V_{GS}$, $V_{DS}$ positive for p-type TFET), the reverse current can be increased by several orders of magnitude, thus limiting the PCE of the rectifier circuit due to the resultant reverse losses. In order to alleviate these losses, a different passive rectifier topology is proposed in this work.

The structure of the work is as follows. Section II introduces the TFET carrier injection mechanism. Section III discusses the problems of applying TFET devices in passive rectifiers. Section IV proposes a novel UHF passive rectifier topology for the specific characteristics of TFET devices. Section V compares the performance between a TFET differential-drive rectifier and the proposed TFET rectifier. The last section presents the conclusions.

II. THE TUNNEL FET DEVICE

A. Physical Characteristics

Unlike the conventional MOSFET, the TFET device is designed as a reverse-biased gated p-i-n diode. For an n-type TFET (n-TFET) the source (drain) region presents a highly doped p-type (n-type) semiconductor as shown in Fig. 1. For this configuration, the tunneling current is generated at the source-channel interface (Fig. 2 b). In the p-TFET the drain (source) presents a p-type (n-type) doped semiconductor.
B. Band-to-Band Tunneling and Drift Diffusion

In TFET devices, the carrier injection mechanism does not follow the laws of thermionic injection as in conventional MOSFET devices. In Fig. 2, the band-to-band tunneling (BTBT) injection mechanism and drift diffusion of a 20 nm Si n-TFET device with the same source/drain doping concentration \( N_{A,D} = 1 \cdot 10^{20} \text{cm}^{-3} \) is presented:

![Fig. 2 Energy band diagram of a Si n-TFET](image)

In the equilibrium state \( (V_{GS} = V_{DS} = 0V) \), both regions in the n-TFET are doped such that the valence band in the p+ type region is located above the Fermi level and the conduction band in the n+ type region is located below the Fermi level. When no voltage is applied to the gate, the tunneling barrier between the source and the channel region is high (Fig 2 a). This will result in a low BTBT probability as expressed in (1), and a consequent low tunneling generation rate (TGR) between the regions (2).

\[
T_{b2b} = \exp \left( -\frac{4}{3} \frac{\sqrt{2} \cdot m \cdot m_o \cdot E_g^{3/2}}{q \cdot h_{eff} \cdot E_{(xy)}} \right) \tag{1}
\]

\[
TGR = T_{b2b} \cdot (f_c - f_v) \cdot E_{(xy)} \tag{2}
\]

\[
I_{on} = \frac{\mu_{sat} \cdot N_c \cdot q^2}{k \cdot T} \int TGR \cdot E_{(xy)} \, dx \, dy \tag{3}
\]

In passive rectifiers, it is assumed that the n-type transistors present a similar voltage polarity on both the gate and drain regions while the p-type transistors present a similar voltage polarity on both the gate and source regions. For the case of forward biased n-TFET devices, the increase of both gate and drain voltage values decrease the tunneling barrier in the source-channel interface as shown in Fig 2 b). Both the conduction and valence band in the channel region bend down, thus increasing the tunneling probability of carriers under the valence band of the p+ region to tunnel through the channel to the empty states of the conduction band in the n+ region. For p-type devices, the decrease of both gate and source voltage values increases the BTBT probability of carriers to tunnel through the channel from the n+ to the p+ region (not shown).

In TFET devices, the reverse bias characteristic leads to two different carrier injection mechanisms. At low reverse bias, the increase of both energy band diagrams on both channel and drain regions can produce both reverse BTBT and drift injection. The latter is shown in Fig. 2 c). At large reverse bias, only the drift diffusion mechanism is produced, as shown in Fig. 2 d). The reverse current produced either by the reverse BTBT and drift diffusion mechanism under reverse bias conditions degrade the TFET transistor performance when applied in rectifiers. The following sections discuss the limitations of using TFET devices in passive rectifiers and how these limitations can be attenuated by the rectifier proposed in this work.
This section discusses the limitation of using Tunnel FET devices in UHF passive rectifiers. For reference, the differential-drive passive rectifier (DDPR) circuit presented in Fig. 3 a) has been presented as a viable solution for RF energy harvesting at low power levels (~mW range) with conventional transistors [3-5]. The application of TFET devices in the DDPR topology was also investigated in [6-7]. The authors have shown by simulations higher power conversion efficiency at low RF voltage amplitudes (sub-0.35 V_{AC}) compared to the use of the FinFET technology. However, and as expected, at higher RF amplitudes (and consequent high reverse bias) the power conversion efficiency of the circuit is degraded. This degradation, although not explicitly stated by the cited references, is not only due to the TFET forward losses but also due to the increase of the reverse current suffered by the TFET transistors during the “reverse” state on both regions of operation (Fig. 3 b).

Considering the state-of-the-art DDPR of Fig. 3 a) and during the first region of operation of Fig. 3 b), the node RF' always presents a voltage higher than that of the node RF. This behavior results in the transistor conditions presented in Fig. 4 a): both transistors M2 and M3 are in the “on state” while M1 and M4 are in the “off state”. According to Table I and II at steady-state conditions, the transistors in the “on state” are characterized by a V_{GS}=2 V_{DS}. The same biasing conditions are presented in the transistors during the “off state”.

<table>
<thead>
<tr>
<th>Region I</th>
<th>State</th>
<th>V_{GS}</th>
<th>V_{DS}</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1 (n)</td>
<td>Off</td>
<td>RF' - RF &gt; 0</td>
<td>RF' &lt; 0</td>
</tr>
<tr>
<td>M2 (p)</td>
<td>On</td>
<td>RF' - RF &gt; 0</td>
<td>V_{out} - RF' &lt; 0</td>
</tr>
<tr>
<td>M3 (n)</td>
<td>On</td>
<td>RF' - RF &gt; 0</td>
<td>RF' &gt; 0</td>
</tr>
<tr>
<td>M4 (p)</td>
<td>Off</td>
<td>RF' - RF &gt; 0</td>
<td>V_{out} - RF' &gt; 0</td>
</tr>
</tbody>
</table>

In the first region of operation and according to Table I, the increase of the RF magnitude (RF’-RF') will result in the increase of the reverse bias V_{DS} of the transistors in the “off state” M1 and M4. With a similar polarity than that of V_{GS} these two transistors are conducting reverse current as explained in section II B. Higher RF AC magnitudes will result in higher reverse losses of the rectifier and PCE degradation.

In the second region of operation and according to Table II, the reverse losses of the rectifier at high RF AC magnitudes will result due to the increase of the reverse bias V_{DS} of transistors M2 and M3.

<table>
<thead>
<tr>
<th>Region II</th>
<th>State</th>
<th>V_{GS}</th>
<th>V_{DS}</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1 (n)</td>
<td>On</td>
<td>RF' - RF &gt; 0</td>
<td>- RF' &gt; 0</td>
</tr>
<tr>
<td>M2 (p)</td>
<td>Off</td>
<td>RF' - RF &gt; 0</td>
<td>V_{out} - RF' &gt; 0</td>
</tr>
</tbody>
</table>
In order to understand the degree of reverse losses in the DDPR due to the reverse current conducted by the transistors under reverse bias conditions, a comparison between the internal resistance of a Tunnel FET and FinFET device is presented in Fig. 5 for the biasing condition $V_{GS}=2V_{DS}$. The simulation results of the TFET device are based on heterojunction structure with III-V materials [9-10]. As expressed in (1) the use of materials with low energy band gap materials can increase the BTBT probability of the TFET device, thus increasing the tunneling current at similar voltage values compared to the use of higher energy band gap materials as silicon.

According to Fig. 5, there is a $V_{DS}$ bias region (in between the dotted lines) where the TFET device is expected to improve the power conversion efficiency of UHF passive rectifiers due to its lower internal resistance in the forward region and higher internal resistance in the reverse region compared to the FinFET device. However, when largely reverse biased ($V_{DS}$ below -0.2 V), the drift diffusion current explained in section II B dominates the reverse current, and degrades the PCE of the rectifier. In Fig. 5, it is shown that under reverse $V_{DS}$ bias, a $V_{GS}$ forced to 0 V can increase the internal resistance, thus attenuating the reverse current (dotted curve). This way, a viable solution to apply TFET devices in rectifiers passes through forcing the $V_{GS}$ of the devices in the “off state” to values close to 0 V.

### IV. PROPOSED UHF PASSIVE RECTIFIER CIRCUIT

In Fig. 6, an UHF passive rectifier circuit designed for the special characteristics of Tunnel FET devices is proposed. The rectifier maintains the forward characteristics of the previous differential-drive circuit, attenuating the reverse losses suffered from the transistors during the “off state”. Compared to the previous rectifier, it maintains four main transistors M1-M4 and requires two auxiliary transistors $M_{1aux}$, $M_{2aux}$ (p and n-type) and two auxiliary capacitors.

---

**Table:**

<table>
<thead>
<tr>
<th>M3 (n)</th>
<th>Off</th>
<th>$RF^+ - RF^- &lt; 0$</th>
<th>$-RF^+ &gt; 0$</th>
</tr>
</thead>
<tbody>
<tr>
<td>M4 (p)</td>
<td>On</td>
<td>$RF^+ - RF^- &lt; 0$</td>
<td>$V_{out} - RF^- &lt; 0$</td>
</tr>
</tbody>
</table>

---

The TFET presents the following characteristics: $L_g=40\,\text{nm}$, P' GaSb, $N_c=4\times10^{19}\,\text{cm}^{-3}$, N' InAs, $N_d=2\times10^{17}\,\text{cm}^{-3}$, $T_{CSL}=5\,\text{nm}$, $T_{OX}=2.5\,\text{nm}$ (HfO$_2$), EOT=1 nm, $\Phi_M=4$ eV. FinFET device is presented as a triple-gate configuration, bulk material, EOT=0.84 nm, fin height=28 nm, fin width=15 nm and gate length of 22 nm.

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![Fig. 5 Internal resistance comparison between TFET and FinFET.](image)

![Fig. 6 Proposed UHF passive rectifier circuit and voltage signals](image)
A. First Region of Operation ($RF^+ > RF^-$)

Considering steady-state conditions, during the first region of operation the two auxiliary transistors are in the “on state” allowing the auxiliary capacitors to charge the nodes $AC^+$ and $AC^-$ to the maximum and minimum voltage values of the nodes $RF^+$ and $RF^-$ respectively. This behavior is observed in Fig. 6, for an ideal case (no output load, no losses in the transistors). In this region, and similarly to the previous DDPR, the main transistors M2 and M3 are forward biased “on state” while transistors M3 and M4 are reverse biased “off state”. With the proposed rectifier, the DC voltage at the gate of the four main transistors will allow a lower average value of $V_{GS}$ (in magnitude) for the reverse biased transistors (less reverse losses) and a higher average value of $V_{GS}$ for the forward biased transistors (less forward losses).

![Fig. 7 First region of operation in the proposed rectifier. Transistors in green are in the “on” state and red in the “off” state](image)

With this configuration, the $V_{DS}$ values of the main four transistors remain the same as the counterpart DDPR. As seen in Table 3, there are possible conditions for reverse current to occur in the reverse biased transistors M1 and M4. However, as $AC^+$ and $AC^-$ present DC values, the period of time that the reverse current is verified is lower compared to the previous rectifier. In this region of operation, there is also a specific region where the auxiliary transistors enter into a reverse bias condition, conducting reverse current.

<table>
<thead>
<tr>
<th>Region I</th>
<th>State</th>
<th>$V_{GS}$</th>
<th>$V_{DS}$</th>
<th>Rev. Current</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1 (n)</td>
<td>Off</td>
<td>$AC^+ &gt; RF^+$</td>
<td>$- RF^+ &lt; 0$</td>
<td>$AC^+ &gt; RF^+$</td>
</tr>
<tr>
<td>M2 (p)</td>
<td>On</td>
<td>$AC^- &lt; RF^- &lt; 0$</td>
<td>$V_{out} - RF^- &lt; 0$</td>
<td>-</td>
</tr>
<tr>
<td>M3 (n)</td>
<td>On</td>
<td>$AC^- &gt; RF^- &gt; 0$</td>
<td>$- RF^- &gt; 0$</td>
<td>-</td>
</tr>
<tr>
<td>M4 (p)</td>
<td>Off</td>
<td>$AC^- &gt; RF^- &gt; 0$</td>
<td>$V_{out} - RF^- &gt; 0$</td>
<td>$AC^- &lt; RF^- &gt; 0$</td>
</tr>
<tr>
<td>M1a (p)</td>
<td>On</td>
<td>$RF^- &gt; RF^- &gt; 0$</td>
<td>$AC^- &gt; RF^- &gt; 0$</td>
<td>$RF^- &lt; AC^- &gt; 0$</td>
</tr>
<tr>
<td>M2a (n)</td>
<td>On</td>
<td>$RF^- &gt; RF^- &gt; 0$</td>
<td>$AC^- &gt; RF^- &gt; 0$</td>
<td>$RF^- &lt; RF^- &gt; 0$</td>
</tr>
</tbody>
</table>

B. Second Region of Operation ($RF^- > RF^+$)

During the second region of operation, the two auxiliary transistors are reverse biased “off state” and therefore, with a sufficient auxiliary capacitance value, the previous voltage at nodes $AC^+$ and $AC^-$ is retained during the entire region. As seen in Table 4, the $V_{DS}$ of the four main transistors remains the same than those of the previous rectifier. In this region, the average value of $V_{GS}$ in the reverse biased transistors M2 and M3 is lower (in magnitude) than the values presented by the previous rectifier.

![Fig. 8 Second region of operation in the proposed rectifier. Transistors in green are in the “on” state and red in the “off” state](image)

<table>
<thead>
<tr>
<th>Region II</th>
<th>State</th>
<th>$V_{GS}$</th>
<th>$V_{DS}$</th>
<th>Rev. Current</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1a (p)</td>
<td>On</td>
<td>$RF^- &gt; RF^- &gt; 0$</td>
<td>$AC^- &gt; RF^- &gt; 0$</td>
<td>$RF^- &lt; AC^- &gt; 0$</td>
</tr>
<tr>
<td>M2a (n)</td>
<td>On</td>
<td>$RF^- &gt; RF^- &gt; 0$</td>
<td>$AC^- &gt; RF^- &gt; 0$</td>
<td>$RF^- &lt; RF^- &gt; 0$</td>
</tr>
</tbody>
</table>
In this section, the performance comparison between the state-of-the-art differential-drive passive rectifier DDPR of Fig. 3 and the proposed rectifier of Fig. 6 is presented. Both rectifiers are simulated with GaSb-InAs Tunnel FET devices [9-10] (characteristics presented in Fig. 5). For both rectifiers, transistors M1-M4 are simulated with channel widths of 1 µm. The auxiliary transistor widths of the proposed rectifier are 400 nm. In both rectifiers, the coupling and load capacitors present a capacitance of 1 pF. The auxiliary capacitors of the proposed circuit are simulated with capacitances of 0.1 pF. The frequency of the AC source is 900 MHz.

Fig. 9 and Fig. 10 present respectively the output voltage and power conversion efficiency of the two rectifiers in study, in function of the RF input voltage. For the simulations, two loads were chosen at the output: 100 kΩ and 10 kΩ.

V. SIMULATION RESULTS

In Fig. 9, it is observed that the proposed rectifier allows for higher DC output voltage at large RF input magnitudes, considering both loads. The reduction of both BTBT and drift diffusion current of the reverse biased transistors allows for higher current in the output load of the circuit, and therefore a higher voltage between the load terminals. At low RF voltage magnitudes, the output voltage of the rectifiers at both load conditions is similar.

As presented in Fig. 10, the reduction of the reverse losses of the proposed rectifier allows for a higher PCE at larger RF input voltage values compared to the DDPR. However, when considering low RF voltage values, the PCE performance of both rectifiers differs according to the load. Under the highest output impedance the losses of the auxiliary circuitry (charging losses and transistor losses) degrade the PCE of the proposed rectifier. As indicated in Table 3 and 4, when the auxiliary transistors are reversed biased, their VGS values are directly dependent on the RF+ and RF− voltage values. For the considered load of 100 kΩ, the
PCE of the proposed converter is shown lower at the input voltage range of 0.1 V and 0.45 V. At higher input voltage, the increase of the output current outperforms the current losses resultant by the auxiliary circuitry, thus increasing the PCE.

The “M” shape of the PCE for a load of 100 kΩ is explained due to the specific characteristics of TFET devices. When reverse biased, the reverse BTBT current is highly dependent on $V_{GS}$, increasing first at low $V_{GS}$ and then decreasing at high $V_{GS}$. Consequently, at low input voltage values the reverse current of the auxiliary transistors is higher than that observed at higher voltage values. When considering the load of 10 kΩ, the higher output current required at the output surpasses the reverse current during all the RF input voltage range considered, and therefore no “M” shape is observed.

In Fig. 11, the PCE of both rectifiers in function of the output current is presented. For both cases, the increase of the output current degrades the efficiency of the rectifiers due to the transistor forward losses. Considering the load of 10 kΩ, the proposed rectifier presents a wider range of output current in terms of efficiency compared to the DDPR.

Under the load condition of 100 kΩ, the “M” shape presented in Fig. 10 is reflected in the PCE of the proposed rectifier. In between the range of 700nA-3μA, the proposed converter is shown less efficient.

In Fig. 12, it is shown that at similar load conditions, and at higher RF input power values, the proposed rectifier allows for higher output voltage values compared to the DDPR. For an output load of 100 kΩ and 10 kΩ, this behavior is respectively observed at -22 dBm and -18 dBm.

Considering the proposed rectifier topology, the consequent increase of the output voltage and output current allows for a higher PCE at large RF input power levels as shown in Fig. 13. As explained in Fig. 10, when considering a load of 100 kΩ the auxiliary circuitry degrades the PCE at low RF input voltage. This degradation is observed for the RF input power range of -42 to -25 dBm.
In Fig. 14, the RF input power distribution of both rectifiers is presented, considering an output load of 10 kΩ and an input RF power level of -13 dBm. At this RF power level, it is observed that the differential-drive rectifier suffers from higher reverse losses (24 %) compared to the proposed rectifier (6 %). It is also observed that the auxiliary circuit of the proposed rectifier is consuming 12 % of the total RF input power. Despite these losses, an increase from 31 % to 46 % in power efficiency is observed with the proposed rectifier.

For reference, the performance of a differential-drive rectifier with FinFET devices (characteristics presented in Fig. 5) is compared with the above mentioned two rectifiers with Tunnel FET devices. The results are presented in Fig. 15.

At low RF input power levels (below -30 dBm), the application of FinFET devices in the differential-drive rectifier is shown to be less efficient than the application of TFET devices due to the difficulty of conventional transistors in conducting the same levels of current as TFETs at low voltage values (sub-0.25 V).

For RFID applications, the use of Tunnel FET devices in passive rectifiers can improve the transmission distances as shown in Fig. 16. According to the Friis transmission equation [3] and compared to the differential-drive rectifier, the proposed solution can increase the range of transmission distances at RF input power levels below -45 dBm.
VI. CONCLUSIONS

In this work, a novel UHF passive rectifier topology for the application of Tunnel FET devices is proposed. It was shown by simulations that compared to the differential-drive rectifier topology, the proposed rectifier allows for higher output voltage and power conversion efficiency at higher RF input power levels. This is possible due to the reduction of the drift diffusion and BTBT current of the TFET devices during their reverse biasing state and a consequent decrease of the reverse losses of the rectifier.

Considering low RF voltage amplitudes, the increase of the output load in the proposed rectifier is expected to degrade the PCE compared to the differential-drive rectifier topology due to the losses suffered by the auxiliary circuitry.

In summary, the proposed rectifier for Tunnel FET devices can improve the RF energy harvesting field due to the possibility of delivering more power to a load for a wider RF input power range compared to the differential-drive rectifier. For RFID applications, the proposed rectifier can increase the transmission distance at a wider range of RF power level.

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