Advances in a baseline process towards high efficiency c-Si solar cell fabrication

P. Ortega, G. Lopez, I. Martín, S. Bermejo, S. Blanqué, M. García, A. Orpella, C. Voz, and R. Alcubilla

Universidad Politécnica de Cataluña, Grupo de Micro y Nanotecnologías MNT, C/ Jordi Girona 1-3, Barcelona, 08034 Spain, e-mail: ortega@eel.upc.edu

Abstract—This paper shows a baseline process to fabricate high efficiency solar cells that are based on the Passivated Emitter and Rear Cell solar cell concept. The idea is to define a very flexible process in order to see, for comparison, the benefits of introducing alternative fabrication steps. For instance, new structures based on laser firing contacts and rear passivation with deposited PECVD a-SiC_x:H layers are planned to be fabricated following the baseline process outlined hereby. In its design, special attention is paid to the front metallization grid and rear point contact design. Preliminary results using Cz p-type 2.8 $\Omega\cdot\text{cm}$ substrates yields photovoltaic efficiencies up to 18.6% in a 1 cm^2 cell with open circuit voltage of 628 mV and an outstanding photocurrent density of 39 mA/cm^2 . Efficiencies of about 21.5% are predicted for the improved devices.

I. INTRODUCTION

A baseline fabrication process is necessary as a reference to demonstrate the benefit of innovative steps introduced into conventional fabrication of crystalline silicon (c-Si) solar cells. This paper describes in detail the design of a baseline fabrication process to obtain high efficiency c-Si cells (> 20%). Additionally, it can be adapted to fabricate other special photovoltaic devices [1-2]. As can be seen in Fig. 1(a), the basic solar cell structure is based on the Passivated Emitter Rear Cell (PERC) concept [3]. In this case rear contacts are done by means of photolithography and rear passivation is achieved by *annealed* thermal SiO₂. This structure can be easily adapted to other recent high efficiency approaches like laser firing contacts (see Fig. 1(b)) [4], or a new promising solution, combining laser firing contacts with a PECVD a-SiC_x:H rear passivation layer (see Fig. 1(c)) [5]. Assuming high quality c-Si material, emitter diffusion and surface passivation, the design of this process is focused on the definition of front and rear metallization. For the front grid, a minimum metallized area is desired keeping series resistance sufficiently low. We study the benefits of a combination between lift-off process and silver electroplating to increase the silver film thickness. On the other hand, we theoretically study the optimum pitch of the rear point contact.

Fig. 1. (a) Basic solar cell structure. (b) Alternative structure using laser firing contacts Front grid metallization (b). (c) Modified solar cells combining laser firing contacts and rear passivation with a-SiC_x:H layers.

II. BASELINE FABRICATION PROCESS

Solar cells are fabricated in p-type FZ or CZ c-Si 4" single side polished wafers with resistivities ranging from 0.5 to 3 $\Omega\cdot\text{cm}$. The main stages in the fabrication process are sketched in Fig. 2: *a*) the process starts with a thermal SiO₂ growth (240 nm thick) to mask texturization and phosphorous diffusion. *b*) Inverted pyramids are created using anisotropic etching with Tetramethylammonium hydroxide TMAH except below metallization paths (busbar and fingers), *c*) once SiO₂ is etched at the active zone, *d*) a phosphorous diffusion is performed using planar diffusion sources to create a homogeneous emitter. *e*) After remove mask SiO₂, *f*) a new thermal dry 110 nm thick SiO₂ film is grown for passivation and antireflection coating purposes. Simultaneously phosphorous emitter is driven-in to the final doping profile ($\sim 70 \text{ } \Omega/\text{sq}$). *g*) Back contacts are patterned using standard photolithography, and *h*) aluminium is evaporated by e-beam at the rear side and sintered with forming gas (*annealing*) at 400°C for 20 min. *i*) Finally front contacts are opened by photolithography and e-beam metallization of Ti/Pd/Ag (40 nm /40 nm/1000-2000 nm) is deposited. Front grid metallization is defined by lift-off and a forming gas annealing at $T=370^\circ\text{C}$ $t=20$ min is carried out to improve passivation and ensure good ohmic contacts.

Fig. 2. Main stages in the baseline fabrication process. Below (right) the front metallization pattern for a $2 \times 2 \text{ cm}^2$ solar cell is shown.

III. SOLAR CELL DESIGN

Device design has two important phases, rear contact grid design and front metallization grid design. In Fig. 3 the different distributed contributions to the specific series resistance r_s in $\Omega\cdot\text{cm}^2$ are shown. Where r_{bus} , r_f , r_{ce} , r_e , r_b , and r_{cb} are the specific lumped series resistances related to busbar, fingers, emitter contacts, emitter, base, and base contact respectively. It is important to minimize r_s without jeopardizing photovoltaic conversion efficiency, η , i.e. maintaining high values of short circuit current density (J_{sc}) and open circuit voltage (V_{oc}).

Fig. 3. Distributed resistance components in the compute of the specific series resistance (a). Point contact geometry (b).

A. Front metallization design

Front metallization must allow extracting current from the device minimizing the blocking of light, and maintaining low front series resistances to obtain acceptable fill factor FF values. Besides, front metallization grid design has technological limitations as it can be the minimum photolithography resolution ($\sim 5 \mu\text{m}$ or $\sim 35 \mu\text{m}$ using glass or acetate masks respectively), and the maximum metal thickness ($\sim 2 \mu\text{m}$ Ag thickness using lift-off technique). As it can be sketched in Fig. 2 metallization grid has a central triangular busbar and rectangular fingers. To simplify the fabrication process, the contacted fraction area in the emitter is the same that the metal fraction area, f_m . Front specific series resistance r_{sFront} can be determined from its components using (1), being r_{ce} negligible.

$$r_{sFront} = \frac{r_{Bus}}{4f_{Bus}W_m}A_{cel} + \frac{r_f}{12f_fW_m}A_{cel} + \frac{r_e}{12n^2}A_{cel} \quad (1)$$

Where ρ_m , W_m , f_{Bus} , f_f , R_{she} , n , and A_{cel} are the metal resistivity ($1.8 \times 10^{-6} \Omega\cdot\text{cm}$ for Ag), the metal thickness, the busbar metallization fraction area, the finger metallization fraction area, the emitter sheet resistance, and the active solar cell area respectively. If we use a high resolution photolithography process f_f and f_{Bus} can be as low as 0.65% and 0.77% respectively ($f_m=1.37\%$ in total). Considering $R_{she}=120 \Omega/\text{sq}$ (measured in the texturized emitter regions) and $W_m=2 \mu\text{m}$, r_{sFront} yields $1.8 \Omega\cdot\text{cm}^2$ for a 4 cm^2 solar cell with $n=25$ fingers. In the same case with a 1 cm^2 cell and $n=10$, r_{sfront} yields $0.86 \Omega\cdot\text{cm}^2$. In a very high efficiency lab cell, total specific series resistance should be lower than $0.5 \Omega\cdot\text{cm}^2$ [7]. Therefore, it is mandatory to grow a thicker metal film. Electroplating is generally used in laboratory c-Si solar cells to overcome this problem. If we assume an electroplating Ag thickness of $7 \mu\text{m}$, r_{sFront} can be about $0.35 \Omega\cdot\text{cm}^2$ for a $2 \times 2 \text{ cm}^2$ lab cell. Nevertheless f_m will be increased to 3.25% due a lateral metal growth during plating process assuming a height-to-width aspect ratio of 1:2.

B. Rear contact grid design

Rear contact grid design not only affects specific rear series resistance $r_{sRear}=r_b + r_{cb}$, but V_{oc} , and J_{sc} as well in opposite manner. A low pitch p value between contacts decrease r_b and r_{cb} but increases rear effective surface recombination velocity, SRV, lowering J_{sc} and V_{oc} . Therefore an optimization of rear contact grid is necessary to obtain high efficiency solar cells.

From [9], r_b can be calculated, neglecting high injection level effects, as

$$r_b = \frac{p^2 \rho_b}{2\pi r} \text{tg}^{-1} \left(\frac{2W}{r} \right) + \rho_b W \left(1 - \exp \left(-\frac{W}{p} \right) \right), \quad (2)$$

and r_{cb} as follows

$$r_{cb} = \frac{\rho_{cb}}{f_{cb}} = \rho_{cb} \frac{p^2}{\pi r^2} \quad (3)$$

Where ρ_b , W , p , r , f_{cb} , and ρ_{cb} are the base resistivity, the wafer thickness, the pitch and point contact radius (see Fig.3), the base contacted fraction area, and the contact specific resistance at the base contacts respectively.

Rear passivation can be studied trough an effective 1D rear passivation S_{Ref} taking into account point contacts grid, and SRV at the passivated regions S_{Rpas} and at the contacts S_c [8]. S_{Ref} is given using (4) and (5), being D_n the minority carrier diffusion coefficient.

$$S_{Ref} = \frac{D_n}{\left[\left(\frac{r_b}{\rho_b} + \frac{D_n}{f_{Cb} S_C} \right)^{-1} + \left(H + \frac{D_n}{(1-f_{Cb}) S_{pas}} \right)^{-1} \right]^{-1} - W} \quad (4)$$

with

$$H = \frac{1}{W} - \frac{2\pi r}{p^2 \tan^{-1} \left(\frac{2W}{r} \right) \cdot \exp \left(\frac{W}{p} \right)} \quad (5)$$

Therefore, rear contact grid can be optimized using a one-dimensional semiconductor device simulator (e.g. PC-1D program). Optimization is performed simulating the structure in the inset of fig. 4. Where R_{tex} is the reflectance of the front texturized surface (square of polished SiO_2 reflectance), $R_{inFront}$ and R_{inRear} is the internal front and rear reflectance respectively (85% and 95% each). In ref. [9] experimental work reported by our group shows the dependence of emitter saturation current density J_{oe} vs. emitter sheet resistance at the end of our baseline process. From this work, it can envisage a J_{oe} value about 50 fA/cm^2 for an emitter of $120 \text{ } \Omega/\text{sq}$ and 1.37% of contacted area. In this case, a front surface recombination velocity SRV about 300 cm/s is estimated at the front passivated surface (introduced into the simulated structure), whereas the contribution of the contacted areas (J_{oec}), is estimated to be 15 fA/cm^2 . This is modelled by introducing a shunt diode with the corresponding saturation current density.

Fig. 4. Reflectance of texturized SiO_2 front surface (dashed line) and total reflectance taking into account internal reflectance (continuous line). The simulated structure to optimize rear contact grid is sketched in the inset of the graph.

In Figure 5 we can see the V_{oc} and FF behaviour related to the pitch distance between contacts with constant radius of $250 \text{ } \mu\text{m}$ for two representative substrate resistivities. It is clear that high FF values require small pitch but it degrades rear passivation lowering V_{oc} . However, highly doped substrates are less sensitive to FF degradation as the additional series resistance is lower. In Fig. 6 efficiency vs. pitch is shown. As it can be seen an optimum pitch about 2 and 1.4 mm is necessary for 0.5 and $3 \text{ } \Omega\cdot\text{cm}$ substrates respectively. As it was

expected, the optimum rear pitch is strongly dependent on substrate resistivity and an *ad-hoc* optimization for the substrate resistivity in use becomes mandatory.

Fig. 5. V_{oc} and FF vs. pitch p for two substrate resistivities (0.5 and $3 \text{ } \Omega\cdot\text{cm}$). Next parameters are been considered in the simulations: $r_{sFront}=0.35 \text{ } \Omega\cdot\text{cm}^2$, $S_{ppas}=300 \text{ cm/s}$, $S_{Rpas}=200 \text{ cm/s}$, $S_C=5 \cdot 10^6 \text{ cm/s}$, $r=250 \text{ } \mu\text{m}$, $J_{oe}=15 \text{ fA/cm}^2$, $\rho_{cB}=0.01 \text{ } \Omega\cdot\text{cm}^2$.

Fig. 6. Photovoltaic efficiency vs. pitch between contacts.

IV. RESULTS AND FURTHER IMPROVEMENTS

Fabrication process have been evaluated using Cz c-Si p-type ($2.8 \text{ } \Omega\cdot\text{cm}$ resistivity) material. Electrical measurements, current voltage I-V and power voltage P-V characteristics, have been obtained using standard test conditions (AM1.5G @ 1 kW/m^2 , $T=25^\circ\text{C}$) as it can be seen in figure 7. Photovoltaic efficiency yields 18.6% in a 1 cm^2 cell with an outstanding photocurrent density of 39 mA/cm^2 . QSS-PC lifetime measurements before metallization and the final measured open circuit voltage V_{oc} value indicates a well-passivated front and rear surface with an estimated rear SRV of 200 cm/s for our SiO_2 layers. The low fill factor FF is mainly due to the use of a high resistivity substrate leading to a high rear contact resistance ($\sim 10 \text{ m}\Omega\cdot\text{cm}^2$), and a non-optimized distance between rear point contacts ($p=2 \text{ mm}$). Additionally a too thin Ag front metallization introduces a significant series resistance to the final device.

Fig. 7. I-V and P-V charts of a 1 cm² solar cell measured in standard test conditions (AM1.5G 1kW/m² T=25°C). A view of the textured surface is shown in the inset of the graph. Table summarizes the main photovoltaic parameter values.

To improve electrical performance of our devices we can introduce some changes: a) a silver Light Induced Plating process (LIP process) to reduce the impact of front metallization in the series resistance. b) Laser firing contacts can create a local p+ region decreasing resistance and SRV at the contacts (see structure *b* in Fig. 1), and lowering rear contact resistance too. Additionally, an empirical optimization of the rear pattern is easily possible. c) The use of a SiC_x:H passivation layer (structure *c* in Fig.1) to minimize SRV at the rear cell side (~50 cm/s).

In order to forecast the maximum achievable efficiency of these improved devices, Fig. 8 shows the calculated efficiency vs. electroplated thickness assuming a rear SRV of 50 cm/s at the passivated surface. A non-selective growth has been considered (height-to-width aspect ratio of 1:2). As it can be seen photovoltaic efficiencies up to 21.5% are possible for electroplated thickness about 7 μm and 0.5 Ω·cm material. Additionally, the upper limit for an ideal Passivated Emitter Rear locally-diffused PERL structure [7] ($p \approx 0$, $J_{0b} \approx 0$ fA/cm², $r_b \approx 0$ Ω·cm²) is also shown in Fig. 8. In this case efficiencies around 23.2% would be possible demonstrating that there is still plenty room for improvement specially for the rear contact design.

V. CONCLUSION

This paper shows a baseline process and the solar cell design to fabricate high efficiency solar cells. The basic cell is based on the PERC solar cell concept. Preliminary results using Cz p-type 2.8 Ω·cm substrates yields photovoltaic efficiencies up to 18.6% in a 1 cm² cell with open circuit voltage of 628 mV and an outstanding photocurrent density of 39 mA/cm². Fabrication process can be easily adapted to recent high efficiency approaches based on laser firing contacts, or a new promising solution, combining laser firing contacts with a PECVD a-SiC_x:H rear passivation layer. Additionally, impact of metallization front grid in the series resistance, especially in large area solar cells, can be reduced by means of a recent silver electroplating method that uses light (Light Induced

Plating LIP process). Simulated studies show that efficiencies up to 21.5% are possible introducing these improvements in our baseline fabrication process.

Fig. 8. Photovoltaic efficiency vs. no selective electroplated Ag thickness for several substrate resistivities. An initial Ag thickness of 1 μm is considered. Rear contacts grid have points with radius $r=250$ μm and pitch $p=2$ mm (in all cases). J_{0a} is fixed to 50 fA/cm². Ideal PERL structure efficiencies with a non-selective (dashed line) and selective growth (dotted line) are also included in the graph.

ACKNOWLEDGMENT

This work was funded by the Spanish government under programs ENE2007-67742-C04-02, ESP2007-299975-E, and TEC2008-02520/TEC.

REFERENCES

- [1] J.M.Quero, C. Aracil, L.G. Franquelo, J. Ricart, P.R. Ortega, M. Dominguez, L. Castañer, and R. Osuna "Tracking control system using an incident radiation angle microsensor" *IEEE Trans. on Industrial Electronics*, vol. 54, no. 2, 2007, pp. 1207-1215.
- [2] P. Ortega, S. Bermejo, L. Castañer "High voltage photovoltaic mini-modules" *Prog. in photovolt.: Res. Appl.*, vol. 16, 2008, pp. 369-377.
- [3] A.W. Blakers, A. Wang, A. M. Milne, J. Zhao, M. Green "22.8 efficient silicon solar cell", *Appl. Phys. Lett.*, 55(13), 1989, pp. 1363-1365.
- [4] W. Brendle, V.X. Nguyen, A. Grohe, E. Schneiderlöchner, U. Rau, G. Palfinger, J.H. Werner "20.5% efficient silicon solar cell with a low temperature rear side process using laser-fired contacts", *Prog. in photovolt.: Res. Appl.*, vol. 14, 2006, pp. 653-662.
- [5] S.W. Glunz, A. Grohe, M. Hermle, M. Hofmann, S. Janz, T. Roth, O. Schultz, M. Vetter, I. Martin, et al. "Comparison of different dielectric passivation layers for application in industrially feasible high-efficiency crystalline silicon solar cells" *Proc. of 20th EPVSEC*, Barcelona, Spain, Jun. 6-10, 2005, pp. 572-577.
- [6] V. Radtke, J. Bartsch, S. Greil, C. Schetter, R. Bergander, and S. W. Glunz "Understanding the electrochemical mechanism of light induced plating by means of voltammetric techniques" *Proc. of 23rd EPVSEC*, Valencia, Spain, Sep. 1-5, 2008.
- [7] J. Zhao, A. Wang, P.P. Altermatt, S.R. Wenham, M. Green "24% efficient silicon solar cells" *Proc. 1st WCPEC*, Hawaii, Dec. 5-9, 1994, pp. 1477-1480.
- [8] H. Plagwitz, R. Brendel "Analytical model for the diode saturation current of point-contacted solar cells" *Prog. Photovolt.: Res. Appl.*, vol. 14, 2006, pp. 1-12.
- [9] P. Ortega, M. Vetter, S. Bermejo, R. Alcubilla "Very low recombination phosphorus emitters for high efficiency crystalline silicon solar cells" *Semicond. Sci. Technol.*, vol. 23, 2008.