I. Introduction

Efficient and optimization power delivery for next generation of multi-core high performance processors and multichannel memory systems, are the challenges required to achieve the high restrictions to design a Voltage Regulator Module (VRM). The challenges imposed for a VRM are a high current capability, low output voltage variation in both steady-state and transient conditions, and high efficiency and optimal power delivery [1]. Multiphase interleaving techniques with voltage-mode and current-mode hysteretic control techniques can to match that challenges [2].

Different control approaches have been considered in the literature for VRM design. Classical solutions such as voltage-mode and current-mode control based in PWM (Pulse Width Modulation) techniques require PI (Proportional Integral) feedback loop compensation circuitry [3]. The dynamic characteristics of these controllers are relatively slow, due to actual limitations to the unity-gain bandwidth imposed by the switching frequency.

The voltage-mode hysteretic control is one of the most appropriate solutions for powering microprocessor loads with high slew-rate current transients. Advantages of this control approach include simplicity and excellent dynamic characteristics. The controller does not have feedback loop compensation circuitry, thus it reacts in the switching cycle where the transient occurs. The hysteretic controller no has the restrictions on the conduction interval of the power switches, this is very important to decrease the recovery time of the output voltage after a current transient [4].

The classical hysteretic controller also has some drawbacks. The output voltage ripple is always higher than the fixed window of the hysteretic comparator, because of delays the switching frequency depends significantly on the power stage components, including output filter parasitic elements. The advanced voltage-mode hysteretic controller includes two sensing networks [5-6]. The switching frequency of this modified controller becomes invariable from optimal parameters controller and the output filter of the regulator.

Multiphase interleaving techniques has several advantages: lower output voltage ripple, harmonics current cancellation, current sharing with high current capability, and fast transient response. Combining the advantages of both techniques, voltage-mode hysteretic control and multiphase interleaving, will result in a efficient and high performance VRM [7].

II. Design of the multi-phase hysteretic regulator

Fig. 1 shows the general diagram of the proposed multi-phase hysteretic regulator, where each phase of the buck converter has its own advanced voltage-mode hysteretic controller. The power stage, include the power components and their respective parasitic elements. The large signal model of this multiphase regulator and the control model are explained in [7]. The controller senses the \( V_{in}(t) \) of each phase and the output voltage \( V_{out}(t) \) and the inductor current of each phase \( i_d(t) \).

II.A. Hysteric controller design

The implementation of the model of control surface for the advanced voltage-mode hysteretic controller is detailed in [7]. The optimal control parameters for the stability and optimal transient response of the output regulator can be determined using the design procedure explained in [7]. The parameters of each hysteretic controller also must satisfy the requirement of resistive output impedance.

II.B. Design example

The multi-phase hysteretic regulator shown in Fig. 1 has been designed according to the requirements given in [7]. A four phase power topology is chosen as good design trade-off between efficiency and cost. The solution to the example is listed in Table 1. The control parameters are calculated according to [7]. The parameters of the current equalization loop are selected by simulation.

![Figure 1. General diagram of the multi-phase buck regulator and i-phase hysteretic controllers.](image-url)
III. Simulation results

Fig. 2 shows the output voltage during a load step change from 0 A to 40 A. Note that output impedance is perfectly resistive given that no over or under shoots are noticeable in the output voltage waveform. Fig. 3 shows the four phase currents. Note that both the current equalization and the interleaving are preserved even during load transient.

![Figure 2: Transient response of v(t) and tolerance limits.](image)

![Figure 3: Interleaving and equalization of the inductor currents.](image)

IV. Experimental results

This section verifies the proposed control design procedure with selected experimental results. A prototype with a selectable number of active phases has been build. Fig. 4 shows the experimental load transient response for four-phase prototype. As it can be seen, the closed-loop output impedance is resistive given that no over-voltage or under-voltage is noticeable.

V. Conclusions

A multi-phase advanced voltage-mode hysteretic regulator has been proposed in this work. The advanced voltage-mode hysteretic controller has been designed and prototyped. The selected simulations and the experimental results demonstrate the validity of the proposed controller. With this laboratory prototype has been achieved the objectives of the proposed multi-phase hysteretic controller.

VI. References


2009 Barcelona Forum on Ph.D. Research in Electronic Engineering 42