Verifying Analog Circuits Based on a Digital Signature

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Abstract—Verification of analog circuit specifications is a challenging task requiring expensive test equipment and time consuming procedures. This paper presents a method for low cost parameter verification based on statistical analysis of a digital signature. A CMOS on-chip monitor and sampler circuit generates the digital signature of the CUT. The monitor composes two signals \( (x(t), y(t)) \) and divides the X-Y plane with nonlinear boundaries in order to generate a digital code for every analog \((x, y)\) location. A metric to be used to discriminate the golden and defective signatures is also proposed. The metric is based on the definition of a discrepancy factor performing circuit parameter identification via statistical and pre-training procedures. The proposed method is applied to verify possible deviations on the natural frequency of a Biquad filter. Simulation results show the possibilities of the proposal.

Index Terms—Mixed-Signal Test, Specification Verification, Monitoring, Nonlinear Zone Boundary.

I. INTRODUCTION

A s circuits increase in complexity, internal signals become deeper embedded into the structure what makes difficult their tracking from IC’s primary inputs/outputs.

Analog and mixed-signal test, in parameter validation procedures, highlights the divorce between new technologies and available test methods. Manual test procedures and the high costs of analog automatic test equipments (AATEs) used for traditional specification based test require increasing resources. In order to assure quality, different methods have been proposed.

Oscillation based test (OBT) has been highly accepted and lately expanded by many authors [1]–[3]. The method consists on making some changes in the CUT which drive the system into a characteristic oscillation. Studying the resulting waveform many defects are detected. Yet, changes should be of minimum impact in the CUT’s normal operation what may be a drawback of the method.

Otherwise, transient testing compares fault-free patterns with some characteristics of the CUT response to simple stimulus (step response or similar). Comparing responses, it is possible to discriminate between defective and non-defective circuits [4]–[6]. On the other hand, structural fault based tests look for the best stimuli to excite the fault. However, in many situations, fault-free does not mean specifications compliant [7], [8].

Alternate test methods [9], [10] try to overcome this analog test scenario using regression models as a technique to predict circuit specifications. Monitoring the power supply current has been used to detect faulty behavioural activity in the CUT [11]. Trying to improve the current resolution, some techniques use multiple chip supply paths [12] or study some interesting points of the circuit [13]. The impact of the monitor insertion into the supply lines and the increment of leakage currents in nanotechnologies limit the viability of these strategies.

In this paper we focus on built-in monitoring of analog signals combined with the on-chip digital signature generation in order to overcome AATE costs. Monitoring can be applied in production testing, diagnosis, parameter validation and signal integrity as well as in field and on-line test. Oscillation test method [2], [3], current monitoring [12], [13], and zoning [14], [15], have been used in the past for these purposes with promising results in digital and mixed-signal applications.

For test purposes, X-Y zoning uses straight lines to cut the plane into zones in order to monitor signal compositions (Lissajous curves) [16], [17]. Recently, a generalization of the monitoring method for multiple variables using several hyperplanes has been proposed. The study is based on Lissajous compositions in a CUT with multitone excitation [18].

In this context, we present: (a) A CMOS digital signature generator and (b) a metric to validate the circuit specifications. The latter is based on the definition of a discrepancy factor and its possibility to verify specifications via statistical and circuit pre-training methods.

The paper is organized as follows. Section II is devoted to present the X-Y zoning method, its possibilities and benefits in circuit testing. Section III introduces the new structure of the nonlinear boundary based signature generator. An on-chip implementation in a 65 nm technology is presented. Section IV is devoted to signature comparison through the defined discrepancy factor and its direct application to validate the natural frequency of a Biquad filter. In section V a summary of the work and conclusions are presented.
II. X-Y ZONING METHOD DESCRIPTION

In the X-Y zone testing method, signal monitoring is based on the composition of two signals of the circuit, \( x(t) \) and \( y(t) \), in a similar way an oscilloscope in X-Y mode represents the trace on the screen. If the ratio of the frequencies of the composed periodic signals is rational, the resultant curve is also periodic becoming the well-known Lissajous curves.

Previous work on monitoring signals in the X-Y plane, is based on dividing the plane by straight lines that delimit the zones where the curve is allowed to have points and the zones where the points are not expected. As an example of application, the output of a low pass filter is represented as a function of its multitone input, generating the Lissajous curve of the CUT. The nominal fault-free curve is represented in the left side in Fig. 1. On the right, the figure shows the Lissajous curve with parameters of the filter out of specification tolerance. In this way, a large set of parametric and catastrophic defects can be detected by just checking whether or not the Lissajous curve remains in the specified zones. Using multiple partitions, the digital code of the zones traversed by the Lissajous curve becomes the digital signature of the circuit. Digital signatures are efficiently processed thereby reducing the overall mixed-signal test costs.

III. MONITOR FOR DIGITAL SIGNATURE GENERATION

Current comparison is a straightforward way to implement control lines composing two or more voltage signals. In contrast with voltage comparison, the easy way to add and subtract currents (Kirchhoff’s law) allows very simple structures to be used. Furthermore, in CMOS applications, the quasi-quadratic current-voltage characteristic of MOS transistors in saturation, enables the implementation of nonlinear curves to delimit zones in the X-Y plane. These characteristics make easier the generation of efficient zone boundaries and the reduction of area overhead.

A. Circuit Design

In order to implement the current comparison we propose the differential input stage of Fig. 2 [21], [22]. In the proposal, four input signals are used, even though the structure can be generalized by simply adding transistors in parallel.

This circuit with only two NMOS input transistors is the well-known “Source grounded differential pair” or “Pseudo
differential pair”. For the PMOS, we use equal sized transistors M5 and M8 as active loads while equal sized transistors M6 and M7 perform the required feedback in order to improve the gain of the stage.

As shown in Fig. 2, input signals ($V_1$ to $V_4$) are directly connected to the gate of NMOS transistors (M1 to M4 respectively), which deliver the current to be added at each side of the differential input stage. Every transistor current is selected according to the needed curve parameters by adequately sizing the input transistor dimensions ($W/L$).

The layout of the proposed monitor, implemented in STMicroelectronics 65 nm CMOS technology, is depicted in Fig. 3. It also includes a high gain output stage. In the design, the transistors have been split in four to balance the structure in order to satisfy two-dimension common-centroid strategies [23] and thus minimize mismatch effects.

### B. Commutation Curves

As can be observed in TABLE I, by interchanging positions of the four input voltages, curve shape and location are controlled. Fig. 4 shows the layout simulation results of the curves corresponding to circuits with the sizes and voltages specified in TABLE I.

![Lissajous Curves and Control Lines](image)

Fig. 4. Layout simulated control lines of TABLE I.

Comparing $V_1$ and $V_3$ voltages (one signal at each side of the differential pair) and setting $V_2$ and $V_4$ to a DC level, the resulting curves are segments of hyperbolae (curves 1 and 2 in Fig. 4). If both sides are symmetrical (transistor aspect ratio and constant voltages) we obtain a degenerated hyperbola that becomes a straight line for input voltages below the threshold voltage because input transistors do not deliver current to the addition. Similar effect affects hyperbolae when reaching the axis.

### IV. Digital Signature Processing

#### A. Basic Approach

In [20] a generalized test method using two observable signals was proposed. Test monitors the Lissajous trace across the nonlinearly divided X-Y plane comparing the resulting set of codes against the golden sequence. In the present work, in order to improve the resolution of the method for small parametric deviations, a new methodology and specification verifying process are proposed.

The zones in Fig. 4 are codified in such a way that every monitor delivers a digital “0” for the region that contains the origin, and a digital “1” for the complementary. Outputs from the monitors are processed by an asynchronous sampler which generates the periodic digital signature.

The signature of a CUT is defined as the sequence of pairs of zone code and time interval of permanence of the CUT’s signals in a zone. This way, the signature registers the zone codes and the duration of the Lissajous curve in the same zone.

Formally, if the periodic Lissajous curve crosses $k$ zones, $Z_1, Z_2, \ldots, Z_k$, and the time duration in each zone is denoted as $\Delta_i, \forall i = 1, \ldots, k$, the CUT’s signature is defined as,

$$\text{SIGNATURE} = \{(Z_1, \Delta_1), (Z_2, \Delta_2), \ldots, (Z_k, \Delta_k)\}$$  \quad (1)

where $Z_i$ represents the code of the $i$th zone traversed and $\Delta_i$ represents the time duration in the $i$th zone.

The implementation is schematized in Fig. 5, where an $m$-bit counter holds the time between code samples. Besides, in Fig. 6, the golden and $+10\%$ $f_0$ shift Lissajous curves can be observed when crossing the X-Y plane. The faulty trace
draws on different zones at different instants which generates a different piecewise function.

The upper chronogram in Fig. 7 shows the zone code (in decimal) for any time $t$ within the period of the Lissajous curves. This procedure in turn leads to a more precise and easier signature comparison when using an appropriate difference between function pairs. Due to the zone codification criterion, neighbour zones only vary in one bit. Furthermore, Hamming distance is suitable as can be observed in Fig. 7 lower chronogram, where the Hamming golden-defect distance is plotted during a period. Note the achievement of 2 (in Hamming distance sense) in the interval $[0, T]$. This is because, in Fig. 6, the faulty trace reaches zone $111110_2 (62_{10})$ instead of the sequence $011110_2 (30_{10}), 011100_2 (28_{10}), 111100_2 (60_{10})$ what will define a free-defect Lissajous.

An indicator of signature difference is required. To achieve this goal we define the discrepancy factor as,

$$
DF = \int_0^T \text{dist}(f,g) \, dt \quad (2)
$$

where the functions $f(t)$ and $g(t)$ respectively represent the defective and golden zones defined within the period $T$ of the Lissajous curves. Operator dist() is the Hamming distance of the codes at each time instant. It indicates the discrepancy of the defective and golden instantaneous codes weighted by the duration of interval in which the Lissajous curve remains in the same zone. This discrepancy factor is sensitive to the length of the curve. To avoid this handicap, a normalized version of the discrepancy factor will be used,

$$
NDF = \frac{1}{T} \int_0^T \text{dist}(f,g) \, dt \quad (3)
$$

The previous definition matches with the average value of the Hamming distance chronogram over the interval $[0,T]$. For the example of Fig. 7, a NDF of 0.102102 is obtained.

In order to investigate the reliability of the normalized discrepancy factor, extensive software simulation has been performed. It explores different degrees of deviation in the parameter under validation. Results are as expected: The discrepancy factor increases almost linearly with the amount of deviation and symmetrically with positive and negative defects, as can be seen in Fig. 8. Simulations on a Biquad filter with added white noise have been performed. In it, we use a $3\sigma$ spread of 1.5% of the supply voltage. Simulations show that deviations as low as 1% in the natural frequency of the filter are easily detected.

### B. Parameter Verification Process

First, it is necessary to study if there is a difference between Hamming signatures of positive and negative defective circuits. To achieve this, a set of training defects have been considered: $-10\%, -9\%, \ldots, +9\%, +10\%$. After computation, signatures are entirely equalized in time, as to obtain unique sized vectors. For instance, in our low pass filter, the resulting signatures are entirely equalized in time, as to obtain unique sized vectors.

A simple method to scatter the two groups of defects is to use a $N$ dimensional hyperplane. This data clustering method is performed by the calculation of the centre of gravity of every set and use it to define the hyperplane parameters. Let us respectively define $z^+$ and $z^-$ as the centre of gravity of the positive and negative set of defects. In a $N$-dimensional vector space, a hyperplane takes the form,

$$
\pi \equiv \sum_{i=1}^N n_i(z_i - p_i) = 0 \quad (4)
$$

where $n = (n_1, \ldots, n_N)$ is a vector normal to $\pi$ and $p = (p_1, \ldots, p_N)$ is any point within $\pi$. In this way, the following definitions become natural (see Fig. 10).
With the calculated $\pi$-hyperplane, parameter identification is easy because we only have to evaluate the resulting Hamming signature in the $\pi$ equation. If the evaluation yields a positive number, the defect is positive and if it yields a negative value, the defect is negative. Defect quantity is determined by the use of the graphical data of Fig. 8.

In order to verify analog circuits with two observable signals, we define a metric to compare golden-defective digital signatures. Comparison is performed using the concept of Hamming distance and defines a discrepancy factor which extracts the amount of defect deviation. A normalized discrepancy factor (NDF) has been defined as the average value of the Hamming distance of the digital zone codes weighted by the time duration of each code.

Verification process is divided in two stages. The former is a data clustering method to compute a separation plane using a training set of defects which lay in opposite space regions. The latter verifies the circuit parameter deviation. This is performed using the mapping of the discrepancy factor and the quantity of deviation within the same sign group.

The method targets the verification of analog parameter specifications in analog and mixed-signal circuits.

V. CONCLUSIONS

A low cost X-Y zoning monitor circuit has been proposed based on a four input current comparator and followed by a high gain stage. The monitor divides the X-Y plane with nonlinear boundaries into zones in order to generate a digital output for each analog $(x, y)$ location. Zone boundaries can be adjusted by changing the biasing voltages and/or the aspect ratio of the input transistors.
Simulations in a noisy environment, with an emphasis on the timing precision (counter size) and the signal quality. Simulations in a noisy environment, with a $3\sigma$ spread of 1.5% of the supply voltage, show encouraging results in detecting deviations as low as 1% in the natural frequency of the filter.

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**REFERENCES**


