Analysis of a Voltage Balancing Technique with Reduced Switching Transitions in a Flying Capacitor Multilevel Converter

Amer M. Y. M. Ghias   Josep Pou   Vassilios G. Agelidis   Mihai Ciobotaru

Australian Energy Research Institute & School of Electrical Engineering and Telecommunications,
The University of New South Wales, Sydney, NSW 2052, Australia.
Email: amer.ghias@student.unsw.edu.au.

Abstract—**This paper reports the analysis of a voltage balancing technique based on optimal switching transitions for a flying capacitor (FC) multilevel converter using phase disposition pulse-width modulation. Since multiple switching transitions between two consecutive voltage levels may be available, such a redundancy is used to regulate the FC voltages at their desired levels. For the selection of the transitions, two techniques are studied and compared in terms of capacitor voltage ripples and switching frequencies. In the first technique, called optimum transition voltage balancing technique, the transitions between two consecutive voltage levels that produce high switching frequencies are avoided. On the other hand, all the transitions between consecutive levels are considered in the second technique. It is therefore called unrestricted voltage balancing technique. Study analyses are conducted by simulation considering all the possible modulation indices and load power factors.**

Index Terms—**Multilevel converter; Flying capacitor converter; Voltage control; Switching transition; Pulse-width modulation.**

I. INTRODUCTION

The flying capacitor (FC) multilevel converter [1] has attracted significant interest in the recent years. The main challenge associated with multilevel FC converters is the voltage balancing of the FCs. For the three-level FC converter, the control of the FCs voltages is relatively simple; it can be performed independently per each phase by simply alternating the two available redundant switching states. A similar voltage balancing technique can be applied to FC converters with a higher number of levels ($n > 3$). However, in this case there are more redundant states to deal with, and also more FCs voltages to be controlled. Each redundant state produces different effects on the charging/discharging the capacitor voltages. Subsequently, controlling the voltages across the capacitors becomes a challenge.

There are many voltage balancing techniques found in the literature for FC multilevel converters. They can be classified into two main categories. The first capacitor voltage balancing techniques are based on the natural balancing mechanism of the converter and therefore they operate in open loop [2]–[11]. Those techniques are mostly based on modifying the phases and shapes of the carriers. Although those techniques usually perform well, the balancing dynamic depends on the loading conditions. Furthermore, they may fail to retain the FC voltage levels if there are nonlinearities or asymmetries in the system. The voltage balancing mechanism can be accentuated

by means of external circuits [5], [6], which usually consist of RLC filters. In [5], a comparison between phase disposition pulse-width modulation (PD-PWM) and phase-shifted pulse-width modulation (PS-PWM) is made, where PD-PWM shows better voltage balancing dynamic. However, the addition of extra passive components makes the system unreliable and large. Moreover, some additional power losses are produced in the filter and also in the converter transistors due to additional ripples in the currents.

A second group of solutions makes use of active schemes to achieve voltage balance in the FCs [12]–[18]. The balancing techniques are based on changing the PWM switching patterns for the capacitor voltage balance. In [12], the voltage balancing technique is integrated in a direct torque control strategy for motor drive applications. The solution of voltage balancing discussed in [13] is based on an exact linearization and is attractive for dc-dc conversion applications. In [14], a voltage balancing technique for a five-level multilevel FC converter is introduced using corrected modulation waveforms by means of adding a square-shaped signal. Nonetheless, the output voltage is affected. In [15], the proposed algorithm uses redundant switching states to adjust the time of the switching functions; however, the algorithm is based on PS-PWM, which produces line-to-line voltages of inferior spectrum quality than PD-PWM [5]. In [16], a proportional integral (PI) controller is used to compensate for the voltage errors in the FCs. However, the dynamic of the system in balancing the capacitor voltages using PI controllers is slower compared to the selection of optimal redundant states in the modulation [17]. Furthermore, tuning of the PI parameters is required [20], and it becomes difficult for converters with a high number of levels. For converters with a number of levels higher than three ($n > 3$), the authors in [16] suggest delaying the measured capacitor voltage signals to regulate the FC voltages, yet this technique is based on a trial and error. In [17], the voltage balancing control is based on space-vector modulation (SVM) by selecting the appropriate redundant switching states. This voltage balancing technique is very effective. The authors however do not perform any switching frequency analysis for the proposed voltage balancing technique and neither have they evaluated the spectrum of the output voltages. A similar voltage balancing approach is conducted in [18] using a cost function but in this case under PD-PWM. The average switching frequencies
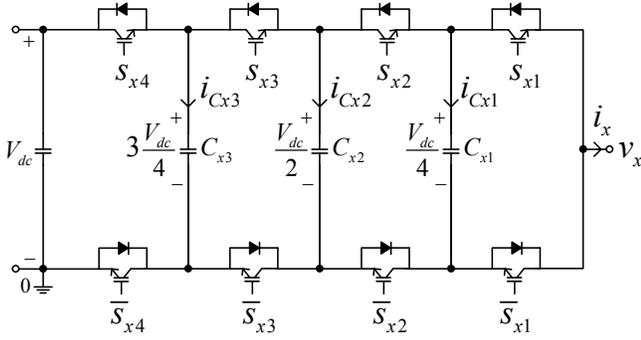
Fig. 1. Scheme of a five-level FC VSC.

TABLE I
FIVE-LEVEL FC CONVERTER: VOLTAGE LEVELS, SWITCHING STATES, FC CURRENTS, AND EFFECTS ON THE FC VOLTAGES

Output Voltage Level (v_{x0})		Switching States					FC Currents			FC voltages		
		s_{x4}	s_{x3}	s_{x2}	s_{x1}	$(State)$	i_{Cx3}	i_{Cx2}	i_{Cx1}	v_{Cx3}	v_{Cx2}	v_{Cx1}
5	V_{dc}	1	1	1	1	{15}	0	0	0	x	x	x
4	$3\frac{V_{dc}}{4}$	1	1	1	0	{14}	0	0	i_x	x	x	↑
		1	1	0	1	{13}	0	i_x	$-i_x$	x	↑	↓
		1	0	1	1	{11}	i_x	$-i_x$	0	↑	↓	x
		0	1	1	1	{7}	$-i_x$	0	0	↓	x	x
3	$\frac{V_{dc}}{2}$	1	1	0	0	{12}	0	i_x	0	x	↑	x
		1	0	1	0	{10}	i_x	$-i_x$	i_x	↑	↓	↑
		0	1	1	0	{6}	$-i_x$	0	i_x	↓	x	↑
		1	0	0	1	{9}	i_x	0	$-i_x$	↑	x	↓
		0	1	0	1	{5}	$-i_x$	i_x	$-i_x$	↓	↑	↓
		0	0	1	1	{3}	0	$-i_x$	0	x	↓	x
2	$\frac{V_{dc}}{4}$	1	0	0	0	{8}	i_x	0	0	↑	x	x
		0	1	0	0	{4}	$-i_x$	i_x	0	↓	↑	x
		0	0	1	0	{2}	0	$-i_x$	i_x	x	↓	↑
		0	0	0	1	{1}	0	0	$-i_x$	x	x	↓
1	0	0	0	0	0	{0}	0	0	0	x	x	x

Note: The charging/discharging effects in the FCs are given
assuming that i_x is positive ($i_x > 0$) with the following
notation:
↑ Capacitor voltage increases
↓ Capacitor voltage decreases
x No change in the capacitor voltage

of the power devices and the output voltage spectra are determined using triangle and sawtooth carriers. A significant amount of switching frequency of the power devices is reduced when using sawtooth carriers. An improved voltage balancing technique is reported in [19], called optimum transition voltage balancing (OTVB) technique, which is based on selecting the best transitions for capacitor voltage balance, besides avoiding those transitions that produce high switching frequencies to the power devices (non-optimal transitions). A significant reduction in the switching frequency of the power devices is achieved when compared with the voltage balancing technique presented in [18].

This paper is a continuation of the previous work reported in [19], where the OTVB technique based on minimum transitions between consecutive states was presented. The main objective of this paper is to evaluate and compare the OTVB technique, that avoids the use of non-optimal transitions, with a similar one where the non-optimal transitions are considered. The second one is called unrestricted transition voltage balancing (UTVB) technique. The analysis is performed by comparing both techniques in terms of average switching frequencies of the power devices and FC voltage ripples. In the analysis, all the possible modulation indices $[0,1]$ and load power factors ranges $[-1,1]$ are considered and some interesting merits and demerits on both techniques are reported.

The rest of the paper is organized as follows. Section II describes the operating principle of a FC converter. In Section III, the OTVB and UTVB voltage balancing techniques are introduced. In Section IV, switching frequencies on the power devices and capacitor voltage ripples are studied and compared. Finally, the conclusions are summarized in Section V.

II. OPERATING PRINCIPLES OF THE FC CONVERTER

Fig. 1 shows a phase-leg of a five-level FC VSC, which integrates three FCs. The subscript x is used for the phase identification $x = \{a, b, c\}$. During normal operation, the mean voltage values of the FCs C_{x1}, C_{x2}, and C_{x3}, should be maintained at $V_{dc}/4$, $V_{dc}/2$, and $3V_{dc}/4$, respectively, where V_{dc} is the voltage of the dc bus. Consequently, the voltage across each switch is only one quarter of the dc-link voltage. The switch control function is defined as s_{xy},

where y defines the particular switch in the phase-leg of the FC converter ($y = \{1, ..., 4\}$). The switch control functions can take two values $s_{xy} = \{0, 1\}$, meaning "0" for switch off and "1" for switch on. The switch pairs in each phase-leg $s_{x1} - \bar{s}_{x1}$, $s_{x2} - \bar{s}_{x2}$, $s_{x3} - \bar{s}_{x3}$, and $s_{x4} - \bar{s}_{x4}$ operate in a complementary manner.

Each phase of the converter can generate five output voltage levels, i.e. 0, $V_{dc}/4$, $V_{dc}/2$, $3V_{dc}/4$, and V_{dc}, with respect to the dc negative rail "0". Using Kirchhoffs voltage and current laws, the line-to-ground voltage v_{x0} and the currents through the FCs (i_{Cx1}, i_{Cx2}, and i_{Cx3}) can be written as:

$$v_{x0} = s_{x4}V_{dc} + (s_{x3} - s_{x4})v_{Cx3} + (s_{x2} - s_{x3})v_{Cx2} + (s_{x1} - s_{x2})v_{Cx1}, \tag{1}$$

$$i_{Cx1} = (s_{x2} - s_{x1})i_x, \tag{2}$$

$$i_{Cx2} = (s_{x3} - s_{x2})i_x, \tag{3}$$

$$i_{Cx3} = (s_{x4} - s_{x3})i_x. \tag{4}$$

Based on (1)-(4), the line-to-ground output voltage and FC currents is determined for all switching states and shown in Table I. The switching states are indicated by binary notation representing the control functions of the upper switches of the phase-leg. It can be seen in this table that the redundant switching states for the voltage levels $V_{dc}/4$, $V_{dc}/2$, and $3V_{dc}/4$ define different current paths through the FCs. Fig. 2 shows the possible transitions between consecutive voltage levels, considering the sixteen switching states of a phase-leg. As in Table I, the binary notation of the switch control
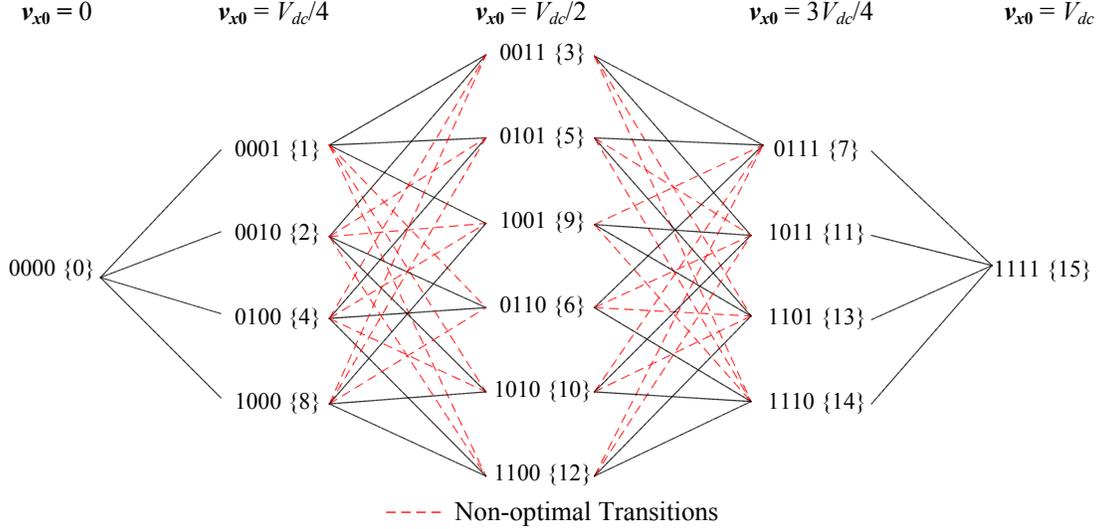
$v_{x0} = 0$ $v_{x0} = V_{dc}/4$ $v_{x0} = V_{dc}/2$ $v_{x0} = 3V_{dc}/4$ $v_{x0} = V_{dc}$

---- Non-optimal Transitions

Fig. 2. Switching transitions between consecutive voltage levels.

functions is also represented by its decimal number within curly brackets.

III. OTVB AND UTVB TECHNIQUES

A. Switching Transitions

Fig. 2 shows the switching transitions between consecutive voltage levels of all the possible combinations of switching states from 0000 {0} to 1111 {15}. The transitions between two consecutive switching states shown by solid lines are called optimum transitions, as those transitions involve changing only one bit. As a result, they produce the minimum number of switching events. On the other hand, the transitions between two consecutive switching states represented by dashed lines are non-optimal, as two or more bits change. For example, an optimal transition is produced when switching between the states 0001 {1} and 0101 {5} (see Fig. 2), while

the transition between the states 0001 {1} and 0110 {6} is a non-optimal. Hence, if the non-optimal transitions are chosen, the switching frequencies of the power devices increase. Additional switchings can be produced due to transitions within the same voltage level. Nevertheless, those transitions can be avoided by using sawtoothshaped carriers [18].

B. Transition Based Cost Function

The cost function is defined as [17], [18] :

$$J_{xz} = \frac{1}{2} \sum_{j=1}^{n-2} C_{xj}(v_{Cxj} - V_{Cxj}^*)^2, \tag{5}$$

where x identifies the phase, and z is the switching state ($z = \{0, ..., 15\}$). For example, J_{a12} is the cost function calculated for Phase a and Switching State 12, i.e. $s_{a4}=1$, $s_{a3}=1$, $s_{a2}=0$, and $s_{a1}=0$ (or 1100). j is the index used for the identification of each FC $j = \{1, 2, 3\}$, C_{xj} being a particular FC and V_{Cxj}^* its reference voltage, and n is the number of levels ($n=5$ in this paper).
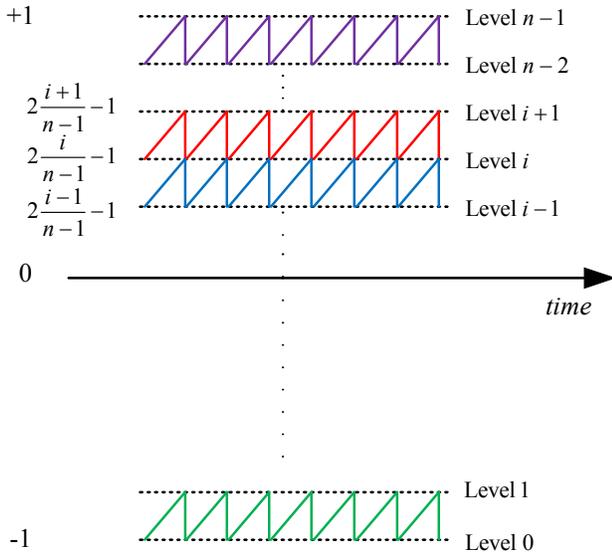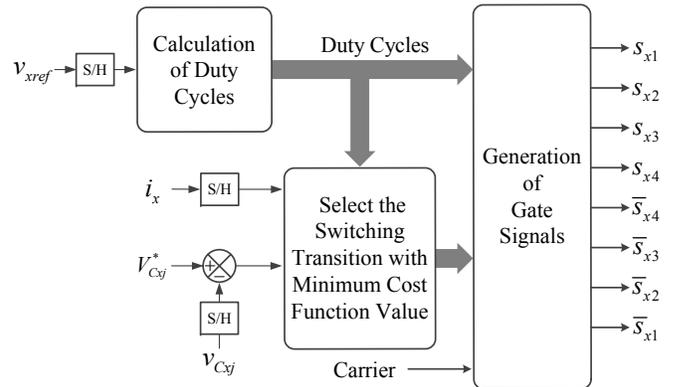

Fig. 3. Sawtooth carriers in PD-PWM.

Fig. 4. Block diagram of the voltage balancing technique for a phase-leg of a five-level FC converter using PD-PWM [19].
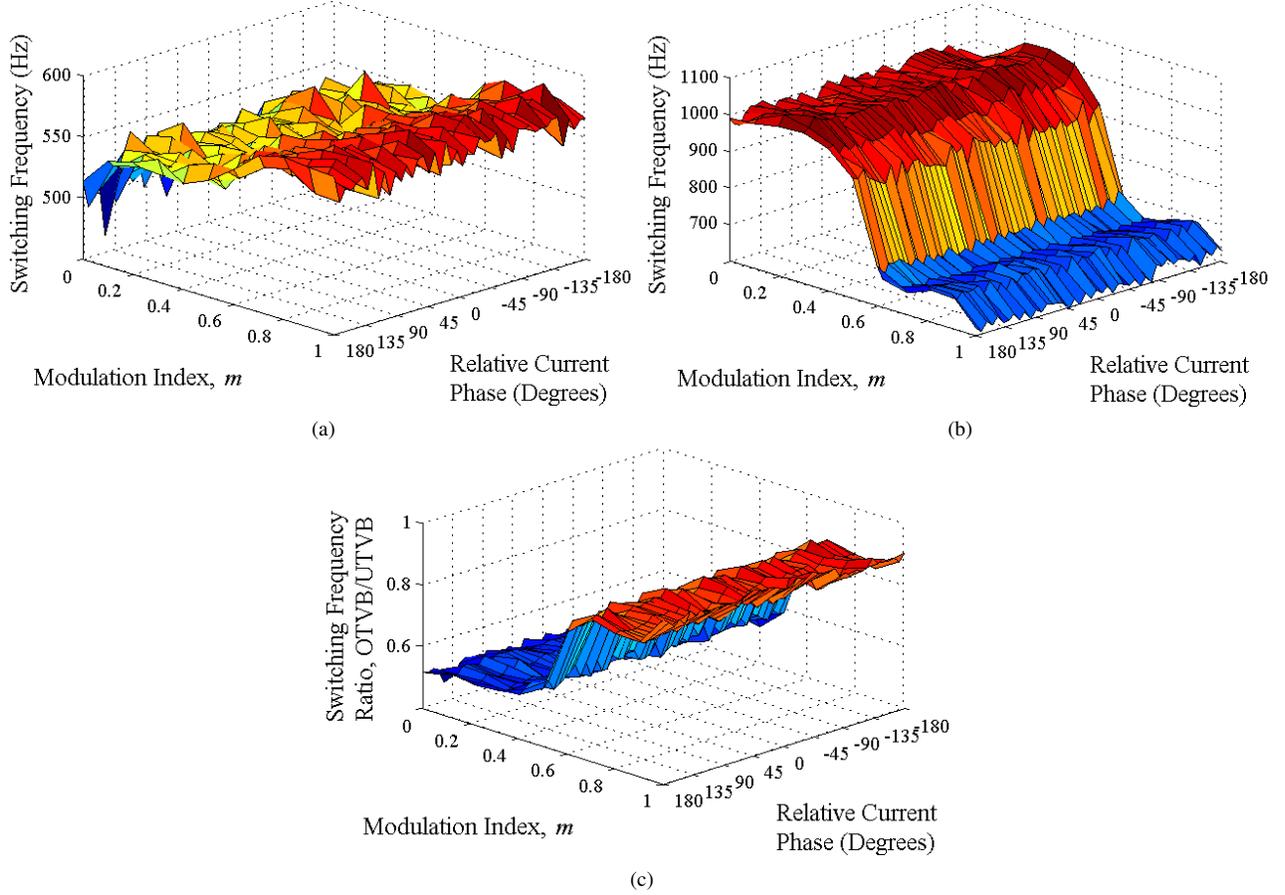
Fig. 5. Average switching frequency analysis of the power devices using a frequency modulation index $m_f = 40$: (a) OTVB technique, (b) UTVB technique, and (c) average switching frequencies ratio OTVB/UTVB of the power devices.

The cost function of (5) is modified to select the optimum switching transitions between two states of different voltage level and is given as:

$$J_{xsn1-sn2} = J_{x,sn1}d_{xi1} + J_{x,sn2}d_{xi2}, \qquad (6)$$

where x identifies the phase $(x = \{a, b, c\})$, $sn1$ is the first state, $sn2$ is the second state, $d_{xi1} \in [0, 1]$ is the duty cycle of the first state, and $d_{xi2} \in [0, 1]$ is the duty cycle of the second state. From Fig. 3, the duty cycle of an output voltage level in PD-PWM can be obtained as follows:

$$\text{for} \qquad 2\frac{i}{n-1} - 1 \leq v_{xref} \leq 2\frac{i+1}{n-1} - 1 :$$
$$d_{xi} = (i+1) - (n-1)\frac{v_{xref}+1}{2}, \qquad (7)$$

$$\text{and for} \qquad 2\frac{i-1}{n-1} - 1 \leq v_{xref} \leq 2\frac{i}{n-1} - 1 :$$
$$d_{xi} = (n-1)\frac{v_{xref}+1}{2} - (x-1), \qquad (8)$$

where v_{xref} is the modulation signal that ranges in the interval [-1,1] under linear operation mode. The cost function of the transitions between two different voltage levels is positively defined, and if all the FC voltages are regulated at their reference value, it becomes zero. Hence, in order to achieve voltage balance, this cost function needs to be minimized at any switching period. Thus, by differentiating (6), the following expression is obtained:

$$\frac{d}{dt}j_{xsn1-sn2} = \sum_{j=1}^{n-2}\Delta v_{Cxj}(i_{Cxj,sn1}d_{xi1} + i_{Cxj,sn2}d_{xi2}) \leq 0, \qquad (9)$$

where $i_{Cxj,sn1}$ and $i_{Cxj,sn2}$ are the capacitor currents of the corresponding states. They depend on the load currents and the redundant switching states, as shown in Table I. Δv_{Cxj} are the voltage deviations of the FCs ($\Delta v_{Cxj} = v_{Cxj} - V_{Cxj}^*$).

C. OTVB Technique

When the modulator defines two particular voltage levels for the following switching period, the cost function (9) is evaluated for all the optimal switching transitions available between those levels. All the non-optimal transitions are skipped in order to avoid over switching. The switching transition that provides the minimum value to the cost function is selected. Once the optimal switching transition is selected, the two consecutive switching states are determined, which define the gating signals of the transistors. The block diagram of the voltage balance technique is shown in Fig. 4.
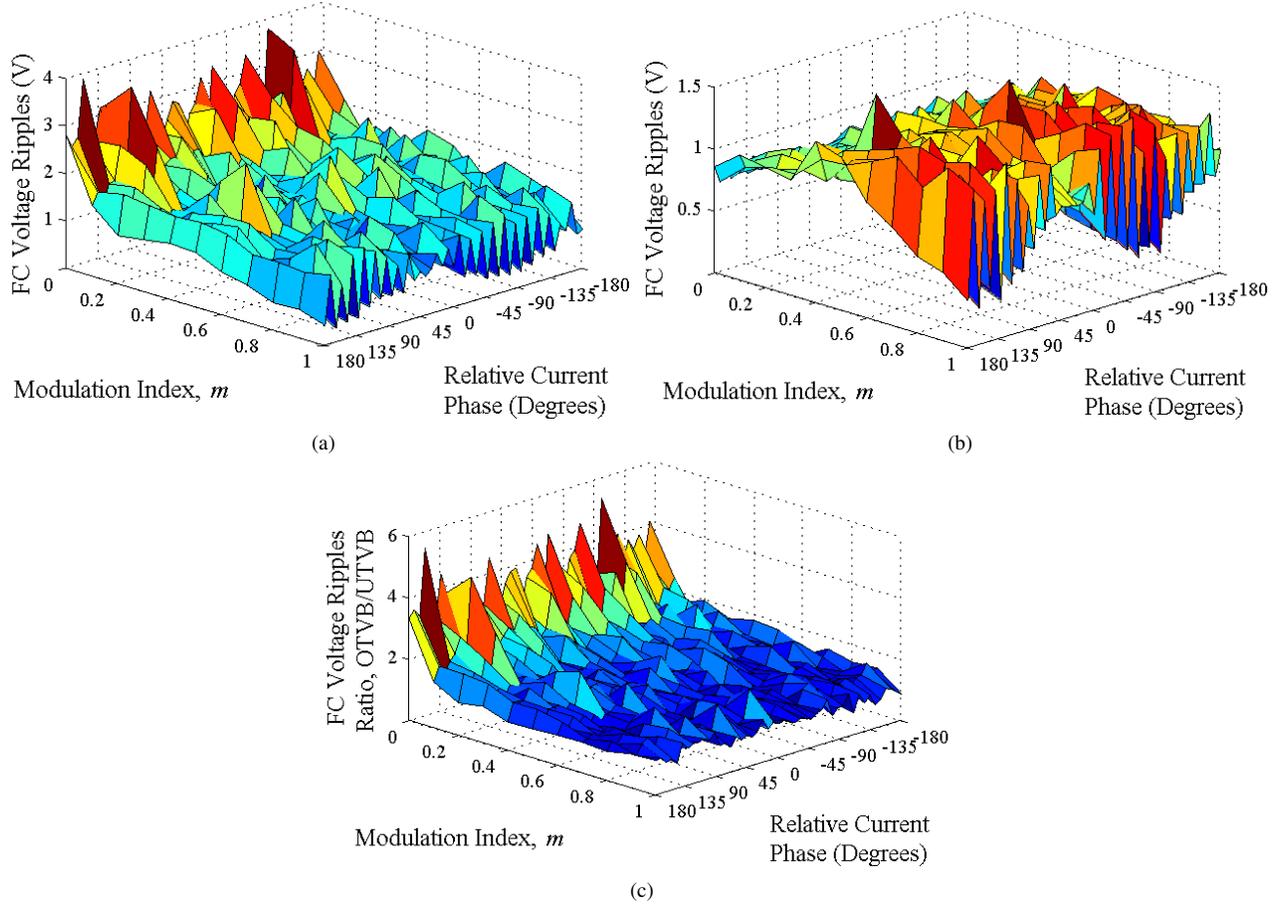
Fig. 6. FC Voltage Ripples analysis, using $m_f = 40$: (a) OTVB Technique, (b) UTVB Technique, and (c) FC voltage ripples ratio OTVB/UTVB.

D. UTVB Technique

The implementation process of the UTVB technique is the same one as in the OTVB technique. The only difference consist in that the non-optimal transitions are also considered in the UTVB technique. The same block diagram shown in Fig. 4 is used for the implementation of this technique.

IV. STUDY ANALYSIS

In this section, the proposed voltage balancing technique is applied to a low-power five-level FC converter. The converter is implemented in MATLAB/Simulink [22] using PLECS blockset [23]. The OTVB and UTVB techniques are analysed and compared. In the simulations, the dc voltage is $V_{dc} = 100$ V and a sinusoidal current source of $I_{xrms} = 2A$ is connected to the converter output. The value of the FCs is $C_{xj} = 220$ μF. The fundamental and the carrier frequencies are $f = 50$ Hz and $f_s = 2$ kHz, respectively, i.e. a frequency modulation index of $m_f = f_s/f = 40$.

Fig. 5(a) shows the average switching frequency of the power devices using the OTVB technique. It is calculated as:

$$f_{sa,avg} = \frac{(f_{sa1} + f_{sa2} + f_{sa3} + f_{sa4})}{4}, \quad (10)$$

where f_{say} for $y = \{1, ..., 4\}$ is the switching frequency of the switch s_{ay}. All possible relative current phase angles and modulation indices have been considered in this

representation. In order to achieve the maximum amplitudes of the output voltage fundamentals operating under linear mode, a zero sequence has been added to the modulation signals of the three-phase system. The zero sequence is given by $-(v_{xref\,max} + v_{xref\,min})/2$, where $v_{xref\,max}$ and $v_{xref\,min}$ are the maximum and minimum instantaneous values of the modulation signals of the three-phase system, respectively. As it can be noticed from Fig. 5(a), the output current phase angle does not significantly affect the average switching frequency. It can be noted that with the OTVB technique the average switching frequency of the power device is about 570 Hz for high modulation indices and about 500 Hz for low modulation indices. Fig. 5(b) shows the average switching frequency in the case of UTVB. It can be observed that it is about 620 Hz for high modulation indices and 1000 Hz for low modulation indices. As in the UTVB technique the non-optimal transitions are not avoided higher switching frequencies are produced when compared with the OTVB technique. Fig. 5(c) shows the switching frequency ratio of both voltage balancing techniques, i.e. OTVB over UTVB, for all modulation indices and load power factors. With the OTVB technique, there is a reduction of the switching frequency of about 12% on average for large modulation indices. Such a reduction in the switching frequency is significantly larger for low modulation indices, i.e. about 48%.

Fig. 6(a) shows the amplitudes of the FC voltage ripples using the OTVB technique. All possible relative current phase angles and modulation indices have been considered in this representation. A zero sequence has also been added to the modulation signals of the three-phase system. As it can be noticed from Fig. 6(a), the voltage ripple amplitudes increase for low modulation indices. However, in Fig. 6(b), different results have been observed using the UTVB technique, i.e. the FC voltage ripple amplitudes decrease for low modulation indices. Fig. 6(c) shows the FC voltage ripples ratio of OTVB over UTVB. It can be remarked that with the OTVB technique there is an increase in the voltage ripples of about 10 to 15% on average for large modulation indices. Such an increase in the voltage ripples becomes larger for low modulation indices.

In summary, using the OTVB technique a reduction of about 12% of the switching frequencies in the power devices for large modulation indices can be achieved at the expense of slightly increasing the FC voltage ripples. However for lower modulation indices the reduction in the switching frequency is even higher, i.e. 48%, yet the ripples increases. Hence, there is a trade-off between the switching frequency reduction of the power devices and an increase in the capacitor voltage ripples.

V. Conclusion

This paper shows a comparison study of two voltage balancing techniques applied to the FC converter. Both techniques are based on evaluating a cost function to optimize the transitions between two consecutive voltage levels. The OTVB technique avoids the use of non-optimal transitions i.e., those that produce more switching events to the power devices, while the UTVB technique considers all the possible transitions. The voltage balancing techniques are implemented in a five-level FC converter. Study analysis showed that, for large modulation indices, the average switching frequencies of the power devices are reduced by about 12% and about 48% for low modulation indices, when using the OTVB technique. This reduction comes at the cost of increasing the FC voltage ripples. Hence, there is a trade-off between achieving a reduction in the switching frequencies of the power devices with an increase in the FC voltage ripples.

Acknowledgment

References

[1] T. A. Meynard and H. Foch, "Multi-level conversion: High voltage choppers and voltage-source inverters," in *Proc. IEEE Power Electron. Specialists Conf.*, 29 Jun.-3 Jul. 1992, vol. 1, pp. 397-403.

[2] S. Lee, D. Kang, Y. Lee, and D. Hyun, "The carrier-based PWM method for voltage balance of flying capacitor multilevel converter," in *Proc. IEEE Power Electron. Specialist Conf.*, Jun. 2001, vol.1, pp. 126-131.

[3] D. W. Kang, B. K. Lee, J. H. Jeon, T. J. Kim, and D. S. Hyun, "A symmetric carrier technique of CRPWM for voltage balance method of flying-capacitor multilevel inverter," *IEEE Trans. Ind. Electron.*, vol. 52, no. 3, pp. 879-888, Jun. 2005.

[4] A. Shukla, A. Ghosh, and A. Joshi, "Natural balancing of flying capacitor voltages in multicell inverter under PD carrier-based PWM," *IEEE Trans. Power Electron.*, vol. 26, no. 6, pp. 1682-1693, Jun. 2011.

[5] B. P. Mcgrath and D. G. Holmes, "Enhanced voltage balancing of a flying capacitor multilevel converter using phase disposition (PD) modulation," *IEEE Trans. Power Electron.*, vol. 26, no. 7, pp. 1933-1942, Jul. 2011.

[6] J. P. Lavieville, O. Bethoux, P. Carrere, and T. A. Meynard, "Electronic circuit for converting electrical energy," U.S. Patent 57 268 70, 1998.

[7] B.P. Mcgrath and D. G. Holmes, "Analytical determination of the capacitor voltage balancing dynamics for three phase flying capacitor converters," *IEEE Trans. Ind. Appl.*, vol. 45, no. 4, pp. 1425-1433, Jul. 2009.

[8] B.P. Mcgrath and D. G. Holmes, "Natural capacitor voltage balancing for a flying capacitor converter induction motor drive," *IEEE Trans. Power Electron. Letter*, vol. 24, pp. 1554-1561, Jun. 2009.

[9] B. P. Mcgrath, T. Meynard, G. Gateau, and D. G. Holmes, "Optimal modulation of flying capacitor and stacked multicell converters using a state machine decoder," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 508-516, Mar. 2007.

[10] A. Ruderman and B. Reznikov, "Simple comparison of different PWM strategies for a three-level H-bridge flying capacitor converter," in *Proc. 12th Int. IEEE Opt. of Elect. and Electron. Equip.*, 20-22 May 2010, pp. 544-550.

[11] S. Thielemans, A. Ruderman, B. Reznikov, and J. Melkebeek, "Improved natural balancing with modified phase-shifted PWM for single-leg five-level flying-capacitor converters," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 1658-1667, Apr. 2012.

[12] M. F. Escalante, J. C. Vannier, and A. Arzande, "Flying capacitor mutilevel inverters and DTC motor drive applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 809-815, Aug. 2002.

[13] G. Gateau, M. Fadel, P. Maussion, R. Bensaid, and T. A. Meynard, "Multicell converters: Active control and observation of flyingcapacitor voltages," *IEEE Trans. Ind. Electron.*, vol. 49, no.5, pp. 998-1008, Oct. 2002.

[14] L. Xu and V. G. Agelidis, "Active capacitor voltage control of flying capacitor multilevel converters," in *Proc. IEEE Electric Power Applications*, May 2004, vol. 151, pp. 313-320.

[15] C. Feng, J. Liang, and V. G. Agelidis, "Modified phase-shifted PWM control for flying capacitor multilevel converters," *IEEE Trans. Power Electron.*, vol. 22, pp. 178-185, Jan. 2007.

[16] M. Khazraei, H. Sepahvand, K. A. Corzine, and M. Ferdowsi, "Active capacitor voltage balancing in single-phase flying-capacitor multilevel power converters," *IEEE Trans. Ind. Electron.*, vol. 59, no. 2, pp. 769-778, Feb. 2012.

[17] S. Choi, and M. Saeedifard, "Capacitor voltage balancing of flying capacitor multilevel converters by space vector PWM," *IEEE Trans. Power Del.*, vol. 27, no. 3, pp. 1154-1161, Jul. 2012.

[18] A. M. Y. M. Ghias, J. Pou, M. Ciobotaru, and V. G. Agelidis, "Voltage balancing strategy for a five-level flying capacitor using phase disposition PWM with sawtooth-shaped carriers," in *Proc. IEEE Ind. Electron. Conf.*, Oct. 2012, pp. 5013-5019.

[19] A. M. Y. M. Ghias, J. Pou, M. Ciobotaru, and V. G. Agelidis, "Voltage balancing of a five-level flying capacitor converter using optimum switching transitions," in *Proc. IEEE Ind. Electron. Conf.*, Oct. 2012, pp. 5006-5012.

[20] J. R. Rodriguez, J. W. Dixon, J. R. Espinoza, J. Pontt, P. Lezana, "PWM regenerative rectifiers: State of the art," *IEEE Trans. Ind. Electron.*, vol. 52, no. 1, pp. 5-22, Feb. 2005.

[21] V. G. Agelidis and M. Calais, "Application specific harmonic performance evaluation of multicarrier PWM techniques," in *Proc. IEEE Power Electron. Specialist Conf.*, 17-22 May 1998, vol. 1, pp. 172-178.

[22] Matlab/Simulink, http://www.matlab.com.

[23] PLECS, http://www.plexim.com.