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Electronic Engineering Doctoral Program in numbers
Selective Excitation of Vibration Modes in MEMS Cantilevers

Author: Jordi Ricart, Thesis Advisor(s): Manuel Domínguez, Joan Pons

I.A. Introduction

The Pulsed Digital Oscillator (PDO) is a sigma-delta based structure introduced by the authors which has been proposed as a control circuit for several applications based on MEMS [1]. A generic PDO is a sampled system that includes a MEMS resonator plus a quantizer and a digital feedback loop providing the force pulses that actuate the MEMS device [2][3] (figure1). PDO systems allow obtaining their oscillation frequencies and spectra easily from its digital output, using only standard tools for digital processing. The topology allows working above and below the Nyquist limit [4].

In a previous work, we show an application of a PDO system as a chemical gas sensor of a Organic Volatile Compounds (VOC) [5]. Our recent result shows that the PDO systems can be used to selectively excite different vibration modes of a MEMS resonator. In order to study such excitation of different vibration modes, FEM and discrete-time simulations have been carried out. Experimental data demonstrating such results are also presented.

II. Vibration Modes

The MEMS device used as resonator device in our experimental work is a SOI silicon cantilever. It consists of a squared silicon plate, with 1000 μm long, 1000 μm wide and 5 μm thick. Device actuation is thermo-electrical, performed through two heating resistors placed in the outer beams. These resistors are covered by a layer of silicon oxide, so that the difference in thermal expansion coefficients between silicon and silicon oxide causes the deflection of the beam/bridge structure. Beam deflection sensing is done using a piezoresistive Wheatstone bridge located in the central suspension beam.

According to the theory and taking into account common materials and process tolerances, the expected mechanical frequency of the fundamental vibration mode of this MEMS structure is in the range between 3.88 and 5.09 kHz. In order to locate the frequencies of the mechanical vibration modes of our MEMS structure, a series of FEM simulations using the FEM Coventorware environment have been performed.

According to this, Figure 2 shows the first three vibration modes of this type, located respectively around the frequencies 4.17 kHz, 28.36 kHz and 82.65 kHz.

III. Experimental results

In order to exactly identify the frequencies of the lower mechanical vibration modes commented above, experimental measurements of the MEMS beam deflection using a scanning microscope vibrometer equipment have been also performed.

III.A. First Resonator vibration modes

The objective of this first set of measurements was to obtain the deflection spectrum of the MEMS resonator after a frequency sweep in the 0 to 400 kHz range. As it can be seen in Figure 3, the resonant frequencies obtained with the vibrometer for the first three longitudinal modes (4.473 kHz for the first mode, 30.55 kHz for the second and 88.48 kHz for the third one) fairly agree with the previous approach based on mechanical simulations. Let us remark that all measurements made with the vibrometer equipment have been done on air conditions, thus damping losses are not negligible.
III.B. First vibration modes excitation with PDO

The main objectives of this section is to demonstrate experimentally the feasibility of separately excite different vibration modes in a MEMS device by setting a few parameters of a PDO structure. The first step was to configure a PDO circuit in order to excite the first vibration mode. To this effect, a configuration was chosen that sets an oscillation mode for frequencies around 4.4 kHz, but it also puts into anti-oscillation mode the frequency ranges around the other two longitudinal vibration modes considered. For the excitation of the second and third vibration mode, the procedure is the same of 1st vibration mode: is necessary to configure the PDO in oscillation mode around the frequencies near one vibration mode and select the anti-oscillation mode around the other two vibration modes.

<table>
<thead>
<tr>
<th>Longitudinal vibration mode</th>
<th>Measured Oscillation frequency</th>
<th>Delays</th>
<th>sign</th>
</tr>
</thead>
<tbody>
<tr>
<td>1st</td>
<td>4.46 KHz</td>
<td>4</td>
<td>plus</td>
</tr>
<tr>
<td>2nd</td>
<td>30.6 KHz</td>
<td>13</td>
<td>plus</td>
</tr>
<tr>
<td>3rd</td>
<td>88.41 KHz</td>
<td>16</td>
<td>plus</td>
</tr>
</tbody>
</table>

Table 1. Configuration parameters of PDO system in order to obtain the three first vibration modes for a 139 KHz sampling.

Table 1 shows the configuration parameters used in order to obtain the three first vibration modes: number of delays, sampling frequency and the sign of feedback loop. In all cases the sampling frequency used is 139 KHz. The sign of feedback loop is the same, also. In this context, only the number of delays is used in order to select the desire vibration mode.

Figure 4 shows the results obtained with the scanning vibrometer when PDO system was configured with the parameters of Table 1. As can be seen in fig 4, the first longitudinal vibration modes of a MEMS device measured in figure 3, can be excited separately with PDO system and are obtained good spectrum performances in the three first vibration modes. The analog and digital channels at the output of PDO system, shows good signal performances as can be seen in Figure 5. From the analog channel we obtained the MEMS position, and from the bit-stream we can be extracted the oscillation frequency at the output of comparator.

IV. Conclusions

Selective excitation of different spatial modes of a MEMS resonator with a configurable PDO system has been experimentally demonstrated. Experimental results, verified with a scanning vibrometer, agree with expectations from previous mechanical FEM simulations.

V. Acknowledgments

This work was supported by the Spanish government through a TEC2007-67951/MIC project.

VI. References


Contribution to advanced hot wire wind sensing
Author: Lukasz Kowalski Thesis Advisor: Vicente Jiménez Serres

I. Introduction

According to the NASA Mars exploration strategy 2009-2020, issued by Mars Science Program synthesis group in April 2003 Jet Propulsion Laboratory is planning to launch in 2013 Mars Science Laboratory mission. MSL Rover will be equipped with state-of-art tools to look for potential bio-signatures on Mars but also to do acquire information about geology, environmental condition and atmosphere. The government of Spain, working with investigators at the Centro de Astrobiologia (CAB) INTA-CSIC, is providing a Rover Environmental Monitoring Station (REMS), which contains among many other whether instruments a hot dice anemometer designed and developed by Technical University of Catalunya. The author role in the project was assist in development and proof that newly design sensor will be able to measure wind velocity and direction in harsh conditions characterizing 'Red Planet'.

II. Mars atmospheric conditions

In situ measurements of atmosphere fluxes on the surface of Mars are difficult because of three things: Mars is a cold planet (average temperature -63 ºC) with wide spam of diurnal temperature from -125ºC to +25ºC, has a very rarefied atmosphere of carbon dioxide with typical pressure of 6mBar to 8mBar, which is about 150 times less than on Earth, see Table 1. Both temperature and pressure reveals tendency to the fast changes especially when a storm or even a dust devil occurs.

<table>
<thead>
<tr>
<th>MARS</th>
<th>parameter</th>
<th>EARTH</th>
</tr>
</thead>
<tbody>
<tr>
<td>5.91</td>
<td>Solar constant [W/m²]</td>
<td>1373</td>
</tr>
<tr>
<td>-3.7</td>
<td>Gravity force [m/s²]</td>
<td>9.8</td>
</tr>
<tr>
<td>CO₂ =95.3</td>
<td>Atmosphere composition of planetary air [%]</td>
<td>N₂ =78.0</td>
</tr>
<tr>
<td>N₂ =2.7</td>
<td>O₂=21,Ar=0.9</td>
<td>H₂=0.01</td>
</tr>
<tr>
<td>6.8</td>
<td>Surface pressure [hPa]</td>
<td>1013</td>
</tr>
<tr>
<td>0.0015</td>
<td>Surface density [kg/m³]</td>
<td>1.2</td>
</tr>
<tr>
<td>0.01</td>
<td>Kinematic viscosity [m²/s]</td>
<td>0.0015</td>
</tr>
<tr>
<td>210 (-63ºC)</td>
<td>Average temperature [K]</td>
<td>300 (+27ºC)</td>
</tr>
<tr>
<td>-125 to +25</td>
<td>Temperature variation [ºC]</td>
<td>-80 to +50</td>
</tr>
</tbody>
</table>

Table 1. Terrestrial and Martian climate comparison.

III. Wind sensor concept

The concept of wind sensor is based on hot point transducers, where the wind speed is worked out from the forced convection measurement of a hot element. The hot point is made by an array of four equally shaped square silicon dice overheated above ambient temperature respect to a fifth reference die standing alone and away in order to sense ambient temperature as is depicted on the Figure 1.

![Hot point](image1)

Figure 1. Wind transducer with cold and hot terminals.

After fabrication, similar chip characteristic have been carefully selected from the batch of dice and assembled in four size group. Then silicon units have been glued to previously shaped Pyrex supports and wire bonded with the external electrical circuits as at Figure 5b. The pyrex structure, which has a shape of inverted table, fulfills two important for the sensor roles: mechanically it supports the suspended silicon die and thermally it isolates the hot chip from the lower temperature surface reducing in the same time thermal looses to the substrate.

IV. Sensor chip fabrication

The crucial part of the sensor is the silicon chip with printed-on titanium-platinum resistance paths. Silicon chip has a square shape 1.6mm long with a standard thickness of 0.4mm. On an oxidized silicon wafer a Titanium layer (10nm) is deposited previous to the Platinum in order to assure adherence to the SiO₂. Then deposition of Platinum material (70nm), which is linearly dependent of the temperature, is followed. In consequence of these processes every chip has three separated resistances: sensing (8000Ω), deltaR (800Ω), and heating (8000Ω), where values of these resistances were measured in reference to the typical ambient temperature (300K), see Figure 3a.

![Hot volume](image2)

Figure 2. Hot anemometry principle diagram

The effect of the wind shadowing for the dice, which are on the rear of the complex structure and effective cooling for the dice, which are in the front of the wind blow, are the thermal domain phenomena that create differences in convective power accordingly to the dice position and wind parameters. For a single die, as shown in the Figure 2, convection power ($P_{conv.}$) can be related with the air pressure ($P_{air}$), wind velocity ($V_{air}$) and also with the overheat between hot temperature ($T_{hot}$) and ambient air temperature ($T_{air}$), as follow:

$$P_{conv.} = \text{const} \cdot \sqrt{P_{air} \cdot V_{air} \cdot (T_{hot} - T_{air})}$$

![Chip mask](image3a)

b) assembled structure

Figure 3. a) Chip mask

![Assembled structure](image3b)
V. Operational circuit

In order to keep hot dice overheated a closed loop circuit with sigma-delta counter has been implemented. To control the whole process we have taken advantage of lineal characteristic of platinum material as function of temperature. The higher value resistances, have been used to monitor die temperature whereas specific current pulses were leaded trough other much thicker heating resistance in order to heat silicon die up to a preset temperature which depends on the third resistance, called deltaR. This shame is applied for each hot point die. Detailed diagram for die C shows Figure 4.

Whenever one of the dice cools down from the expected temperature level sigma-delta converter sends extra power pulses, which are consequently counted (λ) and afterwards translated into the power delivered to each unit. Monitoring temperature condition of each silicon chip and knowing amount of power supplied to every die, the thermal conductances of each die are calculated from:

\[ G_{TH} = \frac{\text{Power}}{\Delta T} = \frac{P_{\text{MIN}} + (P_{\text{MAX}} - P_{\text{MIN}}) \lambda}{(T_{\text{hot}} - T_{\text{air}})} \]

VI. Finite Element Method simulation

Detailed silicon chip analysis recently published in [3] shown uniform temperature distribution along the die unit. According to this fact series of FEM simulation has been performed. Sensor structure has been modeled as it is in original size (Figure 5a), then Martian-like air physical parameters were translated into ANSYS gas parameters used for thermal flow simulation (Figure 5b).

Simulation reveals that average thermal conductance of the group of four dice depends only on the wind velocity independently of the wind incidence angle of attack. Whereas the individual distribution of thermal conductance of each die strongly depends on wind direction. Simulation confirms that units situated in front of the wind head have bigger value of thermal conductance in comparison to the ones allocated in the rear thermally shadowed from the cooling blow Figure 6.

VII. Measurements and tests

Vacuum chamber test shows good thermal isolation of chip from the base and at the same time exposes good sensor ability for coupling with rarified Martian atmosphere. One of the measurements in the Aarhus university Marslab wind tunnel [4] shows in agreement to the previous calculation that convection power of the sensor depends on a square of wind velocity (Figure 7).

Measurements also show better sensor performance to its predecessor Viking and Pathfinder missions units [2].

VIII. Acknowledgments

This work has been done with the support of the Commissioner for Universities and Research of the Department of Innovation, Universities and Company of the Generalitat de Catalunya and of the European Social Fund (scholarship 2006FI00302).

IX. References


Figure 4. Wind transducer block diagram for die C.

Figure 5. a) ANSYS model  b) FEM simulation, 45° wind.

Figure 6. Thermal conductance of each die and average value for CO2 wind: velocity 20m/s and pressure 600Pa.

Figure 7. Average die power consumption response for different velocity flows: 0m/s, 0.3 m/s, 4 m/s, 11m/s, 20m/s.
Compensation for environmental and process variations effects over high performance digital circuits on nanometric regime.

Author: Dennis Andrade, Thesis Advisor: Antonio Rubio

I. Introduction

The transistors feature size is shrunk on every technology update enabling whole systems made of millions of devices can be integrated in one single chip performing more functions with faster response and in addition with lower voltage levels, thus increasing battery life and portability. But as long as the transistor channel length reaches tens of nanometers regime approaching to the optical lithography limit, efficient control over its precise dimensions is becoming more difficult to achieve, yielding to an increase on mismatch, but not only dimensions are suffering from this process variability, carriers mobility, doping profile, threshold voltage, among others, are highly exposed to this phenomena, deviating the resulting integrated circuit from its design specifications. Process variability impact on transistor characteristics in many different ways, this work is mainly focused on timing parameters deviations, how this deviation affects the systems reliability and provide suitable solutions to this problem with minimal penalization on system performance.

In addition to process variability, the timing deviation along the chip is not uniform and according to ITRS is expected to reach a variability of 112% in 2022[1] degrading the circuit performance [6], and it will even more affected because overhead voltage level, \((V_{\text{n}}-V_{\text{th}})\) which sets the electrical characteristics of transistor, becomes a spatial-time function with wider range so also widening the timing characteristics of transistors. In Fig. 3, an "instantaneous photograph" of \(V_{\text{n}}\) for time \(t=t_1\) is shown; this voltage could be completely different on time \(t=t_2\) taking any value within the range \(\pm \Delta V_n\) and similar situations stands for threshold but along \(x-y\) coordinates. The spatial distribution of \(V_{\text{th}}\) combined with time varying function of \(V_{\text{n}}\) provokes \(V_{\text{ov1}}\) for transistor \(M_1\) and \(V_{\text{ov2}}\) for transistor \(M_2\) could be drastically different from time to time. The impact on digital circuits has been analyzed on [7, 8, 9].

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The temperature along the chip is constantly changing because the activity of circuits inside it, and for any
given circuit this temperature will be consequence of its own activity and the heat transmitted from all the circuits in the neighborhood according with its activity profile and the distance between them as show in Fig. 4 (The RC analogy is used to model heat flux through silicon).

In spite the temperature fluctuations are slower than voltage, the temperature difference between two same sized gates un-match its behaviour for nominal conditions and the impact caused by dynamic changes, so the timing for both can be completely different even for same voltage fluctuations[10]. The impact on 90nm combinational gates delay for a given voltage and temperaure ranges are shown in Fig. 5.

II. Working with variations

Designing for the worst case is the most common approach used to avoid possible time violations due to process and environmental variability: time margins are added to clock period in such a way they enclose all the possibles time variations in the most critical paths even for the worst possible case. Working in this way, the clock frequency is penalized and advantages can not be taken from technology improvements. Meanwhile control or limiting variations on process is very difficult to achieve, for environmental factors like temperature, voltage or crosstalk is almost impossible due to its dynamic nature. In this work variability is assumed as a part of circuits characteristics and no efforts to correct or control it are done, but working with it moving from time redundancy techniques to hardware redundancy techniques using compensation methods with built-in setup circuits.

In Fig. 6, the general idea is depicted: a high performance digital system with pipeline architecture where every stage are affected by the process variability in the same manner but have uncorrelated voltage and temperature variations profile. Following the designing for the worst case approach, the maximum clock frequency should be decided considering the effects of all this factors (and some others) on logic cells in order to estimate the largest data process time from the input to the output of the critical paths. The proposed compensation method[11] consist in allocate an even number of NOT gates in the clock path close to the compensated circuit with the purpose both of them be affected by the variations in the same way. The not gate chain will regenerate the clock signal adding to it an skew depending on thermal and voltage conditions in every stage, as shown in Fig. 7. The inserted skew changes as fast as thermal and voltage conditions in every stage, ensuring no time violations and no metastability will occurs even for the largest variations on parameters.

To test the idea, simulations were performed for 8-stage system designed on 90nm technology. The inserted skew just for independent voltage variations on every stage is shown in Table 1 and in Fig. 8.

<table>
<thead>
<tr>
<th>Stage No.</th>
<th>ΔVDD(V)</th>
<th>Δt(ns)</th>
<th>ΣΔt(ns)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>0.000</td>
<td>0.000</td>
</tr>
<tr>
<td>2</td>
<td>-0.05</td>
<td>0.421</td>
<td>0.421</td>
</tr>
<tr>
<td>3</td>
<td>0.05</td>
<td>-0.418</td>
<td>0.003</td>
</tr>
<tr>
<td>4</td>
<td>-0.05</td>
<td>0.421</td>
<td>0.424</td>
</tr>
<tr>
<td>5</td>
<td>-0.1</td>
<td>-0.709</td>
<td>-0.284</td>
</tr>
<tr>
<td>6</td>
<td>-0.04</td>
<td>0.395</td>
<td>0.111</td>
</tr>
<tr>
<td>7</td>
<td>0.03</td>
<td>-0.222</td>
<td>-0.117</td>
</tr>
<tr>
<td>8</td>
<td>-0.03</td>
<td>0.241</td>
<td>0.124</td>
</tr>
</tbody>
</table>

Table 1. Inserted skew in every stage in function of voltage independent deviation from nominal value.

![Figure 6: Pipelined digital system with local compensation circuit.](image)

![Figure 7: Inserted skew as function of voltage and temperature fluctuations.](image)

![Figure 8: Simulations results for 8-stage digital circuit with compensation. The skew inserted in every stage is just funcon of voltage variations.](image)
III. Compensations on large pipeline systems

As has been mentioned, the usual approach to design large systems with critical paths and a lot of pipelined stages is the worst case approach, but the worst case is not the most frequent one and many times has a very small probability of occurrence, penalizing the clock period to avoid a situation that rarely will be present. In the proposal presented in this article, no fixed extra time margins are added to clock period; instead, it is dynamically tuned-in by the local environmental parameters fluctuations presents in each stage through a not chain acting like a buffer, adding just the necessary extra time in every one of them for its current conditions at every clock edge. The proposed technique is very easy to implement due to its simplicity and do not modify the design flow. For larger systems, the compensation is even better, because the addition of the time savings in every stage allows to reduce the clock periods needed to have the data process completed [9].

IV. Conclusions

Process variability and environmental factors affects the timing parameters of transistors and the situations is expected to become more critical for future technologies. Time redundancy philosophy has been proved to be effective in the past, but nowadays, working with variability and noisy environments considering these conditions part of the devices characteristics is mandatory. In this work compensation technique is presented as a method to alleviate the problem in high performance digital circuits with pipeline architecture. The proposal has been demonstrated a very effective and easy alternative to alleviate the effects on device timing parameters of environmental fluctuations.

V. Acknowledgments

This project has been supported by the Projects TEC2005-0293/MIC and TEC2008-01856 of the Spanish Ministry of Science and Innovation.

VI. References

I. Introduction

Ultra Wide-Band (UWB) communication techniques have received increasing attention since United States Federal Communications Commission (FCC) adopted a "First Report and Order" [1] in 2002. Unfortunately the regulations that appeared a few years latter didn’t have the same level of commitment and had much tighter constraints. The FCC part. 15 power spectral density limitation is depicted in Fig. 1, together with the European [2] and Japanese [3] regulations.

Although the word-wide common bandwidth is quite scarce (7.25 to 8.5 GHz), UWB has its niche applications, still. Impulse Radio (IR) implementation of UWB systems has very interesting features such as low complexity, low power consumption, low cost, high data-rate, and the ability of coexistence with other radio systems [4].

II. Ultra-wideband transceiver

The scope of this research is to develop a short-range moderately high data-rate ultra-wideband transceiver with the lowest possible power consumption. In fact, the power budget has mainly determined the architecture and circuit implementation used in this project.

II.A. The UWB transmitter

The usual IR-UWB transmitter consists on a pulse generator that is triggered regularly by a timing circuitry. The output of the pulse generator is connected directly to the antenna, as shown in Fig. 2. No Power Amplifier is needed since the UWB transmitted power is very low. Data is transmitted by modifying some parameter of the pulse (for example, its sign in BPSK modulation or its position in PPM modulation). The transmitted pulse waveform as well as its power spectral density is depicted in Fig. 3.

This transmitted output waveform has a very low duty cycle since sub-nanosecond pulses are sent every frame, which for usual data rates have a duration of several nanosecond. A time Hoping (TH) technique is commonly used to allow multiple users access and to avoid peaks in the spectrum of the UWB signal. A pseudorandom code locates each successive pulse in a different position along its frame.

II.B. The UWB receiver

The IR-UWB receiver can be implemented in several ways, but we focused in a very low power implementation. The receiver architecture is described in Fig. 4.

One of the most efficient ones is a coherent receiver using a matched filter to detect the received pulse [4]. The matched filter receiver, as shown in Fig. 4, decides the received symbol after integrating the result of the multiplication of the received signal with a locally generated Template Waveform (TW). The received signal is processed in the analog domain to optimize power consumption.

The Fig. 5 represents the datagram of the signals involved in this process; data was obtained from simulation. The upper most signal is the template waveform, and the next one is the received UWB pulse. These signals are then multiplied to obtain the signal in the third panel. Then, this signal is integrated to generate the correlated signal, that would be finally fed into the detector (comparator & S/H shown in Fig. 4).
II.C. Template synchronization

In coherent impulse-base UWB receivers the timing alignment between the template and the received pulse must be accurate to correctly receive the information. Fig. 6 compares the SNR degradation against timing errors of different shapes of the template waveform.

Recent works have shown that the impact of timing errors on the SNR degradation can be greatly reduced by using quadrature multiplication (i.e. two receiver paths with 90 degree phase shifted templates) [5].

II.D. Layout and chip Development

The described UWB architecture is under being development in a bulk CMOS 0.18 um technology. A microphotograph of one of the prototypes is shown in Fig. 7. Die size area is 1525x1525 um².

III. Conclusions

Impulse Radio UWB technology has been shown to perform extremely well in power-constrained short-range high data-rate transceivers. A low power transceiver is being developed.

IV. References

New Methodology of Digital IC Design
in extremely high noise and low voltage Scenarios

Author: Lancelot García Leyva
Thesis Advisors: Antonio Rubio, Francesc Moll and Antonio Calomarde

I. Introduction
With the progress on VLSI process technology, the design complexity and the transistor density in SoC increase rapidly, leading to the power consumption and power density in SoC designs rising with the same trend. The size of CMOS devices is scaled down to the nanoscale level, noise interferences becoming significantly affect the VLSI circuit performance. Future electronic devices are expected to operate at lower voltage supply to save power, especially in ultimate and new technologies.

The noise magnitude every day is more important respect the signal magnitude. Noise is a purely random signal, the instantaneous value and/or phase of the waveform cannot be predicted at any time, therefore a probabilistic-based approach is more suitable to handle signal errors than the conventional deterministic circuit design. Noise can either be generated internally in the device, from its associated passive components, or superimposed on the circuit by external sources. The main noise type that affect a digital system is the thermal and flicker noise. The resulting reduction of logic levels approaches to the thermal noise limit, and consequently reduce signal to noise margins will exposing computation to higher soft-error rates. Therefore, circuit designers can no longer assume that future circuits will have error-free operation.

Recently, as the reliability problems associated to technology scaling have become apparent, new proposals have appeared in the literature addressing the problem from the point of view of noise tolerance instead of exclusively considering hard defects. Among the new proposals, there is the so called Probabilistic Logic based on Markov Random Field theory (MRF CMOS [1]) which identifies valid and invalid states, and derives a logic implementation trying to reinforce valid states in order to increase their probability and decrease the probability of erroneous states.

Our proposal is based in detect errors by redundancy of data and correct the errors detected.

II. Proposal
The aim of this work is to increase the robustness of the devices, by introducing redundancy in them by mean of duplicated the number of signals \( x \), adding the complementary data of \( x \). This does the system has more information to detect and correct errors in its inputs and outputs, when the system is under a big amount of noise (thermal and flicker noise mainly).

Our idea is take into account the complete set of possible states that reinforce the correct states. In the present proposal we implement the reinforcement functions taking into account all possible values of the input and output ports and their complements giving a total of \( 2^N \) states, being \( N \) the number of ports. The reinforcement functions are implemented to correct possible faults in the states. The examples of a NOT gate and a NAND gate are given in next sections.

II.A. NOT gate
In a NOT gate, with 2 ports, there are 16 possible states to all the combinations of input \( (x_i, xo) \) and output \( (xo, xoc) \) variables, this is shown in Table 1. The implementation here proposed is based on reinforcement functions that correct an invalid state by forcing the nearest correct state using the Hamming distance. For example, the state 0010 should be corrected to the nearest valid state, which is 0110. With this information, feedback functions are obtained. Incorrect states with more than one faulty variable (states 0000, 0011, 0110, 1010, 1100, and 1111) in Table 1) are equidistant to both valid states, and therefore the resulting state cannot be determined. This is expressed as “x” in the truth table to implement the reinforcement functions.

<table>
<thead>
<tr>
<th>Current state</th>
<th>Corrected state</th>
</tr>
</thead>
<tbody>
<tr>
<td>( x_i )</td>
<td>( x_i )</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
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<td>0</td>
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<td>0</td>
<td>1</td>
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<td>0</td>
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<tr>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Table 1. Possible states and correction by the reinforcement function. I - Invalid state, V – valid state, x do not care for Petrick’s method.

The synthesis of the feedback function are made using Petrick’s method according to the information presented in Table 1. Its method obtains all the possible minimized functions, this allows to apply additional optimization strategies, choosing the one with the least number of gates. Equations 1 to 4 are the reinforcement functions for the variables of the NOT gate and its implementation is shown in the Fig. 1.

\[
X_i = \frac{(x_{ic} \cdot x_{oc}) \cdot (x_i \cdot x_{ic})}{(x_i \cdot x_{ic})}
\]

\[
X_{ic} = \frac{(x_i \cdot x_{oc}) \cdot (x_{ic} \cdot x_{oc})}{(x_{ic} \cdot x_{oc})}
\]
II. NAND gate

In the case of a 2-input NAND gate, the combinations of input \(x_a, x_{ac}, x_b, x_{bc}\) and output \(x_o, x_{oc}\) ports give a total of 64 possible states, of which 4 are valid combinations and the rest have at least one fault. Again, the feedback functions are chosen to correct a faulty state by reinforcing to the nearest valid state. Fig. 2 shows the resulting schematic for the NAND gate.

III. Simulation results

In order to show the robustness of our proposal two logic gates was implemented a NOT gate and a NAND gate with three different methods: standard CMOS, MRF reinforcer, and our approach, all three in a 90nm CMOS technology. A \(V_{DD}\) in the range of 0.65 V to 0.45 V are the current ITRS predictions for 2022 year [2], and therefore for show the results in this work we use a \(V_{DD}\) of 0.5 V.

The gates logic are evaluating in the inputs with an additive Gaussian random noise of mean 0V and standard deviation of 0.6V rms (from 0 to \(V_{DD}\)). Uncorrelated noise sources are applied to each of the inputs, while the outputs are left unforced.

The obtained transient waveforms are shown in Figs. 3 and 4 for the NOT and NAND gates, respectively. It can be seen how our proposal has a better Signal to Noise Ratio (SNR) especially in the NAND gate case, where the standard CMOS has a nearly useless output signal, and the MRF proposal presents spurious oscillations.

IV. Conclusions

The results shown in the previous section demonstrate an better noise tolerance of the present approach compared to the previous proposals. The improvement with respect to MRF Reinforcement is due to a better evaluation of the reinforcement functions in terms of all possible errors.

This improvement is obtained at the expense of a large overhead in area and timing that must be carefully evaluated. This area and timing penalties would be prohibitive in today’s noise environment and technologies. The target field of application of this new technique is therefore the ultimate and new technologies. One scenario is beyond-CMOS devices with a large degree of behavior uncertainty, and where the small scale of the devices makes the area overhead again affordable.

V. Acknowledgments

This research work has been supported by the Spanish Ministry of Science and Innovation (MICINN) through the project TEC2008-01856 with the additional participation of FEDER founds and CONACyT Mexico under grant 164013. The group of research is considered a consolidated group by the MICINN.

VI. References

Design of reconfigurable RF circuits for self-compensation
Author: Didac Gómez Salinas, Thesis Advisor: Diego Mateo Peña

I. Introduction
In recent years the continuous scaling of CMOS technology driven by the digital market pressure has allowed the implementation of complete SOC’s (System On Chip), where together with the digital baseband, analog and RF functions were also implemented. That level of integration has allowed manufacturers to reduce the cost associated with the use of specific technologies as SiGe HBTs or GaAs FETs for the RF part. As technology continues its scaling down it allows the operation of RF CMOS transistors at bands that previously were the domain of compound semiconductors.

Unfortunately, with every new generation the effect of process variations has a greater impact on the final yield of the product [1]. The effects of process variations in deep scaled MOSFETS is a well known issue for digital designers, but not until now analog and RF designers enter in those technology nodes pressed by the market. Due to the sensitivity of RF circuitry to parasitics and the high bandwidths usually involved the compensation techniques that must be used in RF CMOS applications differs from what one could usually use in baseband design.

Typical designs done nowadays assume a worst case scenario and designers tend to over design the system to withstand the predicted variations. This approach typically increases the power consumption of the system, what is a problem in battery powered systems. Thus, the RF design community faces a new paradigm: design of “self-healing” (self-compensating) RF circuits that are able to detect their operating point and reconfigure to meet the specifications.

The aim of this thesis is to study the effects of process, voltage and temperature variations upon the performance of deep scaled CMOS RF circuits and propose and design strategies for their compensation.

II. Design of RF circuits with variability in mind
RF design trade-off can be summarized in a very intuitive way using the RF design hexagon [2]. One drawback of that hexagon is that Yield is not included, so in this thesis we propose to add Yield as a new variable of the design space exploration.

II.A. Short-Channel effects for Yield enhancement
As CMOS technology has scaled down transistors started to suffer from short-channel effects. One not so obvious characteristic of short-channel effects is that transistor transconductance has a reduced sensitivity to process variations. The following graph shows the percentual gm variation against voltage overdrive for several transistors sized to have the same nominal transconductance:

As can be seen a foundry BSIM4 model is compared against an analytical model with and without short-channel effects. The difference between the square-law plot and short-channel one is the desensitivity of a short-channel transistor to process variations, the use of short-channel effects for robust design was explored previously in [3] for supply voltage immunity. With that idea in mind it was designed a LNA with high overdrive (LNA2) and same nominal specifications that a low overdrive one (LNA1). Montecarlo simulation results are summarized in the following table, the specification limits applied are 19 dB<\(G_V<23\) dB, \(S_{11}<10\) dB, NF<5 dB, IIP3> -10 dBm:

<table>
<thead>
<tr>
<th></th>
<th>LNA1 mean</th>
<th>LNA2 mean</th>
<th>LNA1 std deviation</th>
<th>LNA2 std deviation</th>
<th>LNA1 yield</th>
<th>LNA2 yield</th>
</tr>
</thead>
<tbody>
<tr>
<td>(G_V) (dB)</td>
<td>20.72</td>
<td>21.37</td>
<td>1.96</td>
<td>1.32</td>
<td>71.5</td>
<td>85.90</td>
</tr>
<tr>
<td>NF (dB)</td>
<td>4.80</td>
<td>4.5</td>
<td>0.48</td>
<td>0.27</td>
<td>81.2</td>
<td>96.3</td>
</tr>
<tr>
<td>(S_{11}) (dB)</td>
<td>-17.37</td>
<td>-17.3</td>
<td>6.46</td>
<td>5.8</td>
<td>90</td>
<td>90.60</td>
</tr>
<tr>
<td>IIP3 (dBm)</td>
<td>-5.03</td>
<td>-5.73</td>
<td>2.47</td>
<td>0.48</td>
<td>98.1</td>
<td>100</td>
</tr>
<tr>
<td>Total Yield (%)</td>
<td>61.9</td>
<td>78.5</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

As can be seen the use of high overdrive (short-channel) results in a Yield increase due to gm spread reduction. The trade-off paid with that approach is a nearly doubling of power consumption. If the target application is a battery powered one that approach will lead to a higher than desired power consumption. Since we have other parameters in the design space we designed a current-reuse LNA (LNA3) with high overdrive.

In a current-reuse circuit the transconductor (NMOS or PMOS) is substituted by a composite transconductor composed by NMOS+PMOS transistors. With that approach it is possible to reduce the current needed for a given transconductance. Comparing that LNA with the reference one(low overdrive) we obtain the following results:
Table 2. Comparison of Yield results between low(LNA1) and high overdrive current-reuse LNA (LNA3).

As can be seen combining current-reuse transconductors with high overdrive is possible to increase the yield, moreover no power consumption increase is needed being possible to even save power. The drawback with current-reuse approach is a reduced linearity specification, so if power is scarce but linearity is not too stringent is possible to use short-channel current-reuse transconductors to improve the yield.

II.B. Replica transconductor sense and compensation

So far we have shown that is possible to increase yield exploiting short-channel effects. The main trade-off is an increased power consumption or a reduced linearity specification, moreover the use of current-reuse limits the maximum frequency of operation of the LNA since PMOS have a lower peak $f_t$ in a given technology. If we are in a situation that we cannot apply current-reuse (due to linearity or frequency limitations) and we cannot tolerate a power consumption doubling a third alternative for Yield enhancement is desirable.

In [4] a negative DC feedback loop was used to overcome process variations, basically the approach uses the fact that a process variation will change the DC operating point of a transistor thus that transistor is a process variation on-chip sensor. The drawback of that approach is that is not truly non-intrusive and causes a parasitic signal feedback, if we could eliminate the direct sensing of the main transconductor we would avoid topology changes and unstability problems.

Based on the premise of [3] that a transistor itself is a process variation monitor it was designed a “self-compensated” LNA. In this LNA we have the main circuit plus a sense and conditioning circuit. Next figure illustrates that concept:

In this circuit the sense circuit is just a scaled down replica of the main transconductor (to reduce the power consumption of the auxiliary circuitry) and a signal conditioning circuit that tracks DC current shift of the replica transconductor and generates an inverse bias slope (negative feedback for process variations). The following table illustrate the results achieved with that approach with the following specification limits applied 19<$G_v$<23,$N_F$<5,$S_{11}$<10,$I_{IP3}$>3:

With that approach the power consumption penalty paid is a modest 10.6%. It should also be noted that simulations were done with process & mismatch and no correlation between transistors, if process only simulations are carried replica transconductor biasing achieves a 77.9% of Yield pointing that if good layout (placing main and sense transistors close together) Yield increase can be significative. Main advantages of this approach for Yield enhancement over short-channel compensation are that no circuit redesign is needed, it’s a non-intrusive compensation strategy making it suitable for mmW CMOS and no performance trade-off is made except a modest power consumption increase.

III. Conclusions:

Scaling has allowed operation at higher frequencies and/or reduced power consumption but these benefits will vanish if design margins are increased in every new generation to ensure manufacturing yield. To overcome that situation is necessary to shift the way RF circuits are designed and consider Yield as a specification since the beginning of the design process.

IV. References:


2. RAZAVI, B., RF MICROELECTRONICS. COMMUNICATIONS ENGINEERING AND EMERGING TECHNOLOGIES, ed. T.S. Rappaport. 1998: PRENTICE HALL.


Author: Luis Martinez-Alvarado, Thesis Advisor: Jordi Madrenas

I. Introduction
As complexity of mixed-signal integrated systems increases, it becomes more and more necessary to model and simulate the behavior of such systems following a top-down methodology that allows to evaluate the architecture trade-offs while at the same time avoiding long delays of the detailed simulation of devices, taking into account that long simulation times are required to obtain meaningful results as, for instance, in delta sigma modulation. After the architecture definition, a refining process would link the high-level behavior with the finest device-level, post-layout electrical simulation.

One of the most popular analog modeling languages is Verilog-A. By means of co-simulation with an electrical simulation, it is possible to combine high-level behavior descriptions with electrical-level devices, thus accelerating the simulation time while keeping precision for the sections of interest of the design in that simulation.

The previous considerations become even more valid when the mixed-signal device has to interact with external systems, such as MEMS (Micro Electro Mechanical Systems) sensors and actuators, by means of classic signal processing chain [1] or reconfigurable systems (FPAA).

Since the 1990’s, FPAA (Field Programmable Analog Arrays) have received the designers’ attention because this type of devices provides flexibility in analog circuit system design, similar to FPGA (Field-Programmable Gate Arrays) in the digital domain. However, because of scalability issues and the reduced modularity of analog blocks compared to digital counterparts, the development of reconfigurable analog hardware has been progressing very slowly.

II. High Level Modeling
In mixed systems the top-down design style is extremely useful to mix conservative (i.e., that obeys the Kirchhoff’s laws of potential and flow conservation) and signal flow components in the same system. Verilog-A was used to create and use modules that encapsulate high-level behavioral descriptions. The behavior of each module can be described mathematically in terms of its terminals and external parameters applied to the module.

For example, in Fig. 1 an advanced translinear CMOS circuit is shown, where we have the emitter (E), base (B) and collector (C) terminals named after the BJT counterpart, and \( I_{B1} \), \( I_{B2} \) are bias current terminals for calibration. The impact of \( I_{B1} \) is illustrated in Fig. 2, where this parameter moves the curve along the horizontal axis controlling the output current value (\( I_D \)) in the operation region. This means that it affects the exponential region and the distortion region. On the other hand, \( I_{B2} \) doesn’t affect the whole curve, it only adjusts the distortion region along the horizontal axis. When \( I_{B2} \) decreases, the input dynamic margin decreases too, because saturation region is reached faster.

Table 1 shows the RMS error of the high-level model of the translinear element compared with the transistor level model. The maximum error happens when \( I_{B1} \) is minimal.

<table>
<thead>
<tr>
<th>% RMS Error</th>
<th>( I_{B1} = 2 \mu )</th>
<th>( I_{B1} = 4 \mu )</th>
<th>( I_{B1} = 6 \mu )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( I_{B2} = 2 \mu )</td>
<td>11,1</td>
<td>7,5</td>
<td>6,1</td>
</tr>
<tr>
<td>( I_{B2} = 4 \mu )</td>
<td>10,6</td>
<td>2,7</td>
<td>4,1</td>
</tr>
<tr>
<td>( I_{B2} = 6 \mu )</td>
<td>11,3</td>
<td>7,3</td>
<td>5,7</td>
</tr>
</tbody>
</table>

Table 1. RMS Error %, the impact of \( I_{B1} \) and \( I_{B2} \) calibration currents in the high-level model.

III. Architecture and Modeling of a Reconfigurable Translinear Cell

Fig.3 shows the block diagram of a Reconfigurable Translinear Cell (RTC), that has been selected as testbench. The RTC has 7 different forms to be configured: 1) as pure Translinear Element (TE), 2) TE with Enz-Punzenberger connection (EP), 3) as bias current source cell, 4) as bias current source with a programmable capacitor, 5) as a current mirror cell, 6) as current mirror with a programmable capacitor and finally 7) as pure programmable capacitor cell. The available translinear FPAA testchip contains a 5 x 5 RTC array. These cells can be connected and configured as desired to form a specific circuit.
IV. Applications

In analog VLSI, the translinear approach provides compact and fast implementation of such basic blocks, being very suitable when using bipolar transistor; however, the MOS transistor exhibits an exponential characteristic only in weak inversion, which severely limits speed. The reconfigurable analog block in a FPAA proposed in [2] overcomes these limitations. Some of the most common basic operations in translinear FPAA are filtering, and non-linear functions, e.g., products and divisions. Two applications have been mapped on the FPAA: A 4-quadrant multiplier and a 4th-order low-pass filter [4].

IV.A. Four-Quadrant Multiplier.

In Fig. 5 the DC characteristic of the four-quadrant translinear multiplier at different tuning currents is depicted. The parametric analysis shows the different curves with a differential input $I_x = I_x^- - I_x^+$: -10 μA, -6 μA, -2 μA, 2 μA, 6 μA and 10 μA.

IV.B. Fourth-Order Low-Pass Filter.

Fig. 4 shows the general nth-order low-pass filter schematic. The input stage is a translinear element with EP connection, the next stages define the filter order, each i-stage provides a pole by means of capacitor $C_i$, that is placed between $TE_{2i}$ and $TE_{2i+1}$ to ground. The output stage is a simple translinear element.

The filter has been, tuned at different cut-off frequencies, as is shown in Fig. 6. The last curve has a cut-off frequency at 7 MHz approximately and a steep slope due to the translinear element bandwidth limitation. The rest of the curves have a slope of 120 dB/dec approximately, corresponding to the expected fourth-order slope.

V. Conclusion

Linear and nonlinear analog signal processing circuits have been mapped on a translinear FPAA, with promising results. A high-level simulation methodology is being developed to improve the development of complex mixed-signal FPAA.

VI. Acknowledgments

This work has been partially funded by the Spanish Ministry of Science and Innovation project TEC2008-06028/TEC. The Author holds research fellowships supported by the Catalan Department of Universities, Research and Information Society (DURSI) and the European Social Fund (ESF).

VII. References

Analysis of the high frequency substrate noise coupling mechanisms on LC-VCOs
Author: Marc-Manel Molina Garcia, Thesis Advisor(s): Xavier Aragonés and Diego Mateo

I. Work motivation
During the last years, the basic physical limits of the CMOS scaling are restricting the evolution trends of the CMOS integration [1]. The Moore’s Law is starting to be limited by the fact that reducing the size of a transistor does not necessarily imply an improvement in terms of power consumption, size, performance and even price. The CMOS industry has been investing during the last years in the improvement of the system level integration as a path to continue with the improvement in cost, size and performance that the conventional CMOS scaling alone is not able to provide.

The complete System-on-chip (SoC) IC integration (see Fig. 1 left) is one the main goals of nowadays semiconductors industry, which is always focused in getting more functionality at an affordable cost. Unfortunately, the “dreamed” situation of a complete SoC integration is presenting a lot of challenges and drawbacks, especially around R&D cost, time to marked and mixed signal design integration, which are limiting the number of scenarios where SoC is really an optimum solution.

System-in-Package (SiP) is a solution where two or more dies are integrated in the same package (see Fig. 1 right), trying to deal with the before mentioned challenges. A reduced number of dies helps in terms of reliability, high-volume cost, general performance of the system ... But other characteristics are worsen when a reduced number of dies is used, as the reusability of IPs and the capability of upgrading individual components, both critical in shorting the so important time-to-market. In any case, it is clear that the complete atomization of a design into a high number of dies is also far from being the best solution and a high effort should be done to cope with the few dies/SoC drawbacks, in order to allow the integration into a low number of dies or even into a single chip.

From the many issues involved in the decision of the optimum number of dies when implementing a mixed signal system, there is a critical limitation not mentioned before: the electrical interaction between different blocks using the same silicon substrate, which can force a SoC design to move into a SiP solution or can severely increase the number of required dies in a SiP solution.

A very sensitive RF block to the noise in the substrate is the Voltage Controlled Oscillator (VCO). The presence of noise in the substrate can harm the VCO performance [2,3] in terms of output spectral purity, phase noise and it can even modify the oscillation frequency, having an important impact in the correct behavior of the rest of the blocks connected to it.

In order to define some methods that can efficiently reduce the effect that the substrate noise has on the VCO it is important to deeply analyze the following issues:

- How does the noise propagate in the substrate?
- Which are the main coupling mechanisms from the substrate to the VCO and which factors determine the path and level of coupling?
- What kind of methods can be used to increase the isolation between the VCO and the substrate noise? Which is their frequency efficiency range?
- Which design rules should a VCO designer follow to create a noise robust VCO?

II. Work objectives and methodology

The objective of this work is to define a set of guidelines to help RF designers to create LC-VCOs immune to substrate noise.

The work will investigate the different coupling mechanisms that allow the substrate high frequency noise to impact the VCO performance. Independent analysis of each of these mechanisms will allow to determine the most sensitive nodes of the VCO and to define methods to increase the isolation with the substrate of the critical devices.

The characteristics of the noise, especially in terms of frequency, play an important role in the analysis of the coupling mechanisms and sensitive nodes as well as in the proposed isolation methods, which will be characterized to define their frequency range of effectiveness.

A successful result of the investigation will represent an increase in the VCO robustness to the hostile digital and RF environment, reducing the complexity of the design VCOs in a SoC scenario.

III. Work results

III.A. Substrate noise isolation techniques

The use of protection structures to isolate a sensitive part of a circuit from substrate noise has been widely analyzed in the literature [4], but the results of these investigations present a very dispersive range of isolation reached with each method, suggesting that the isolation efficiency has a very high dependence with the technology process and the practical condition of each isolation structure (geometrical characteristics, interconnections, substrate impedance).

It is extremely important to understand the limitations of each isolation technique and how to overcome them.

The efficiency of some substrate isolation structures as a technique to reduce the coupling between two substrate contacts has been evaluated using several test structures [4]. The test structures, see Fig.2, have
been designed and fabricated in two different CMOS technologies, 0.18µm and 0.35µm and have been measured up to 40 GHz.

Fig. 2. Test structures for the substrate coupling investigation. 0.35µm (left) 0.18µm (right)

The results of the analysis, part of them shown in Fig. 3, have shown that the efficacy of the isolation techniques has a high dependence with the frequency, concluding that it will be very important to know the characteristics of the noise prior to decide how to protect a sensitive node due to the limited frequency range of efficiency.

Fig. 3. Results of the isolation measurements for different isolation techniques (left) and for different distances (right)

A second important conclusion is the high relevance of the way that the protection structures are connected to the power distribution lines. It is extremely important to provide a low impedance return path for the noise, otherwise, the efficiency of the isolation structure will be highly limited, specially at high frequency, due to the inductive effect of the interconnections.

III.B. High performance QVCO design.

A low phase noise ultra low power 2.5GHz QVCO has been designed using a 5 GHz and a frequency divider [5]. This architecture reduces the effect that the inband noise can have over the performance of the QVCO, reducing the risk of the integration of the QVCO and the PA on the same substrate.

The 2.5 GHz QVCO has been designed using power-saving techniques to reduce the QVCO power consumption without degrading its performance, leading to an outstanding QVCO in terms of phase noise and IQ balance with extremely low power consumption. Fig.4 shows a photograph of the 2.5G GHz QVCO and a table with its characteristics.

Fig. 4. 2.5 GHz QVCO image (left) and a summary of the QVCO characteristics (right).

![Table][1]

<table>
<thead>
<tr>
<th>Technology</th>
<th>CMOS 0.18µm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>1.2 V</td>
</tr>
<tr>
<td>Power consumption</td>
<td>2 mW</td>
</tr>
<tr>
<td>Control voltage tuning range</td>
<td>2.5MHz-2.5GHz</td>
</tr>
<tr>
<td>Control voltage tuning sensitivity</td>
<td>500 MHz/1V</td>
</tr>
<tr>
<td>Digital tuning range</td>
<td>110MHz</td>
</tr>
<tr>
<td>Phase noise (2MHz)</td>
<td>375-5 dB/Hz</td>
</tr>
<tr>
<td>IQ imbalance</td>
<td>≤ 2.5% ± 0.5</td>
</tr>
</tbody>
</table>

III.C. Effect of substrate noise on a VCO

As stated before, the performance of a VCO can be degraded due to the substrate noise. Fig. 5 shows the harmful effect of low and high frequency substrate noise on the output spectrum of a VCO.

Fig. 5. Effect of high and low frequency noise on a VCO

The effect of the substrate noise on the performance of a VCO and the efficiency of some isolation techniques has been evaluated on a 7GHz LC-VCO fabricated on a 0.18µm CMOS process and on a 5GHz LC-VCO 0.35µm CMOS process.

Four test circuits have been fabricated based on a basic 7 GHz, LC-VCO including several isolation techniques (on-chip and off-chip decoupling capacitors, distance, p+ rings) as a way to reduce the effect of the noise from DC up to the VCO fundamental frequency. Fig. 6 shows the layout of two of the 7 GHz VCOs and the measured DC sensitivity curve of one of them.

Fig. 6. 7 GHz VCO layout (left) and 7 GHz VCO sensitivity curves.

Currently, the performance of the VCO alone has been measured while the measurements of the noise impact are under progress. From these measurements, the main contributor to the noise coupling, as well as the efficiency of the isolation techniques, will be identified.

The 5 GHz VCO has also been designed using different decoupling techniques and guard rings setups and will be used to support the results of the 7 GHz VCO and as a preliminary experiment.

IV. References

I. Introduction

As we enter the Deep Sub-Micron era, Integrated Circuits (ICs) manufacturers are facing the increasing amount of layout process variations that arise from the optical lithography manufacturing process and that pose many challenges for circuit design due to their effects in performance, power and yield.

In order to mitigate the impact of these process variations new Design For Manufacturability and Yield (DFM&Y) approaches are required [1-3], where DFM&Y techniques can be defined for any given industry as the methodologies to ensure that products can be manufactured repeatedly, consistently, reliably and in a cost-effective manner. In the field of ICs, Resolution Enhancement Techniques (RETs) such as Phase Shift Mask (PSM), Optical Proximity Correction (OPC) and Off-Axis Illumination (OAI) have been used to greatly improve layout printability and to reduce process variations. However, these techniques are computationally expensive and very time-consuming for large integrated circuits with arbitrary layout patterns. That is why new DFM&Y regularity-based techniques, with a reduced number of layout patterns, like Gate Arrays or Structured ASICs are emerging as a possible solution for manufacturers.

Layout regularity helps to reduce the enormous data set to be treated by RETs applied to a huge number of layout patterns. For example, in a usual Standard Cell library consisting of 1000 standard cells there are approximately 2 million possible configurations to arrange a pair of standard cells. By improving layout regularity, RETs can work properly and efficiently to reduce the variations caused by lithography.

II. VCTA proposal

Our proposal is a new regular layout style called Via-Configurable Transistor Array (VCTA) that maximizes layout regularity at device and interconnect levels in order to maximize the benefits of layout regularity [4]. VCTA is a regular fabric based on a single configurable basic cell including transistors and interconnects. Fig. 1 and 2 show the VCTA basic cell and how it is connected to obtain the complete layout.

The expected benefits of layout regularity are: (a) a reduction of the amount of process variations by allowing RETs to more effectively mitigate lithography printability issues, (b) a reduction of the yield loss associated to circuit energy and delay unpredictability due to the reduction of process variations, (c) a reduction of the time-to-market by accelerating RETs and also due to the lower number of basic cells or layout patterns and neighborhoods to be optimized, (d) a reduction of design costs as a consequence of the previous benefits.

Based on the observation that regular designs such as SRAMs get to the market long before irregular conventional logic designs such as microprocessors, we believe that VCTA maximum regularity may allow to use the next technology node with commercial yield when Standard Cells use still the old one. To explore the whole regularity trade-offs, we also have to measure and take into account area, delay and energy overheads due to VCTA regularity.

III. Results

In order to illustrate that our VCTA regular design technique allows the implementation of complex circuits we focus on combinational logic circuits like binary adders that are usually included in typical IC designs.

In particular, we have developed complete layouts in the 90 nm technology node for a 32-bit Carry-Ripple adder (CR32) and for a 32-bit Carry-Lookahead adder (CLA32) using the VCTA structure and also the Standard Cell approach (STD) to evaluate the area, energy and delay overheads in two commonly used circuits.

III.A. CR32 and CLA32 without process variations

We have performed complete electrical simulations of the extracted layouts of CR32 and CLA32 in the
90nm technology node. We have evaluated both the adders designed with our VCTA regular design as well as those based on standard cells in terms of delay and energy for 10400 inputs that we have sampled from all 26 programs in the SPEC2000 benchmark suite. We have measured the delay from input variation to the associated output transition considering the cross at 90% of the voltage rise or fall swings. We have also measured energy for each input combination integrating the current demand at the power supply source during the sum. Finally, we have measured the area directly from the layout.

First, VCTA regular design implies an increase slightly smaller than 2x in area when compared to the STD approach. In terms of delay and energy, results are complementary for CR32 and CLA32. On one hand CR32 presents more than a 2x ratio for delay but less than a 2x ratio for energy, and on the contrary for CLA32. In fact overheads introduced by VCTA when compared to STD are very much dependent on the function to implement. STD uses different standard cells depending on the circuit optimization but VCTA always uses the same basic cell.

III.B. CR32 and CLA32 with process variations

In order to evaluate our VCTA proposal under device process variations, we have performed the same electrical simulations considering 3-sigma gaussian random local process variations on PMOS and NMOS parameters.

We expect that our VCTA proposal presents some process variation decrease because of its layout regularity. Estimating how much variations would decrease is fully technology dependent, so we have studied 3 variability scenarios: (a) Considering 100% of the Gaussian distribution 3-sigma deviation percents for the MOS parameters variations, (b) Considering 75% of the technology variations (25% reduction), (c) Considering 50% of the variations (50% reduction).

As expected, the reduction due to layout regularity of the amount of device process variations implies a decrease of the variability of delay and energy for our regular VCTA proposal. The decrease is almost linear with the reduction of process variations. The strength of VCTA is to reduce the amount of process variations and not to be more robust in front of the same amount of process variations.

IV. Conclusion

Our VCTA design technique explores the impact of maximizing layout regularity to maximize its benefits. Maximum regularity reduces the amount of process variations and therefore reduces drastically the time-to-market and the investments required to reach commercial yields. We expect that VCTA permits the use of a future technology node when the STD designs still use the old one.

CR32 and CLA32 Monte-Carlo simulations have shown that, as regular designs benefit from a process variation reduction, energy and delay variability are reduced and therefore the circuit predictability is improved.

However, simulations also show that compared to the STD approach in the same technology node there is an important decrease in circuit efficiency due to regularity. Our final objective is to achieve similar performance for VCTA in the future technology node and for STD in such a way that both of them may reach the market at the same time but VCTA reduces investments required to achieve commercial yield levels and also final product cost.

V. Acknowledgments

This research work has been supported by Intel Corporation, Feder Funds, the Spanish Ministry of Education and Science under grant TIN2007-61763, TEC2008-01856 and FPU AP2007-04125 and the Generalitat de Catalunya under grant 2009SGR1250.

VI. References

I. Introduction

The increase of Process Variability (PV) on Nanometric Technologies (65-32nm) had originated that the estimation of leakage had passed through the worst and best case estimation [1]-[2] to the estimation of bounds and most recently the use of statistical techniques. The actual tendencies on leakage estimation indicate that the most accurate way to estimate leakage is through of Statistics Techniques (ST). The main advantage of Leakage Currents Estimation with ST is providing high accuracy and small time of simulation compared with Monte-Carlo (MC) analysis performed with HSPICE. Statistical Leakage Estimation (SLE) on Nanometric Circuits is based on two methodologies: a) SLE based on Analytical Expressions of Leakage (AEL) include the characterizations and modeling of the 3 most important components of Leakage (I\textsubscript{Subth}, I\textsubscript{Gate} and I\textsubscript{BTBT}) at transistor level in presence of intra- and inter-die Process Variations and Temperature (PVT) and b) SLE based on Lookup Tables (LUT) involves the characterization of the values mean ($\mu$), sigma ($\sigma$) and correlation ($\rho$) of leakage of each transistor, cell of module for each possible input vector.

This work present a brief review and analysis of SLE of Bounds based on LUT’s of Pre-Characterized CMOS Cells (PCC) [3].

II. Statistical Leakage Estimation

The method of SLE of Bounds at Circuit Level Considering PV and spatial correlations is based on the assumption of all circuit have one maximum “max” (and minimum “min”) input that generate the corresponding Upper Bound “UB” (or Lower Bound “LB”). To find the expected max (min) input is performed a fixed amount of Random Inputs (RI) where a second assumption establish that the max (min) input that generate the corresponding UB (LB) is approximated the same as the expected max (min) input selected can’t give us the real UB (LB). The answer is that the SLE of Bounds based on LUT’s of Pre-Characterized CMOS Cells (PCC) was well validated due to we take in account the correlation ($\rho$) of PV of the cells (INV, NAND & NOR with 2, 3 and 4 inputs), input state and their localization (spatial correlations ($\beta$)) inside of the circuit. LUT of cells shows that exist one input of each cell that present the max (min) nominal leakage. If we compare these values in presence of PV the increase of leakage is proportional and the same input(s) remains as the max (min) leakage. In case that exist one input that generate many cells with max inputs and high variability, the inclusion of two case of spatial correlations ($\beta$) present a good metric to obtain real estimation of leakage values avoiding the worst (best) case(s) of estimation and maintaining valid the consideration that the max (min) input generates the UB (LB).

The proposed SLE based on LUTPCC based on Nominal Bounds employs the next information and software showed in the diagram of the figure 2.

III. Results

Given a circuit under study (i.e. any ISCAS85 Benchmark) the SLE-LUTPCC works following the next steps:

1. The mean ($\mu$) and variance ($\sigma^2$) and the correspondent UB ($\mu + 3\sigma$) and LB ($\mu - 3\sigma$) for the min and max input patters are obtained using the 58 LUT of Pre-Characterized CMOS Cells. The $\mu$ of the entire circuit is calculated as the sum of all mean’s of all cells inside of the circuit.

2. The $\sigma^2$ and $\sigma$ of the entire circuit is calculated for the relationship between the 58 Pre-Characterized CMOS Cells. For example for 3 CMOS cells named A, B & C correspondent to INV\(_{111}\), NAND\(_{111}\) &
NOR is calculated with the equation (1). The analysis for 3 variables can be easily extended to complete cells inside of the circuit under study. The spatial correlation $\beta$ between cells is calculated for two options: i) without spatial correlation ($\beta=0$) and with spatial correlation between cells ($0 \leq \beta \leq 1$). The value of spatial correlation modifies the effective value variance in the circuit.

$$
\sigma^2_{\text{Leak}} = \sigma^2 + \beta^2 \sigma^2 + 2 \rho_{\text{MOSG}} \sigma \sigma_{\text{T}} + 2 \rho_{\text{BCG}} \sigma \sigma_{\text{C}}
$$

(1)

3. The leakage variation of $\pm 3\sigma$ with respect to the mean values is obtained with the next equations:

$$
I_{\text{Leak-input min}} = \mu_{\text{Input}} \pm 3\sigma_{\text{min}}
$$

$$
I_{\text{Leak-input max}} = \mu_{\text{Input}} \pm 3\sigma_{\text{max}}
$$

(2)

The figure 3 present the histograms from the ISCAS85 C17 and C7552 for 10000 Monte-Carlo PV obtained with the use of standard Monte-Carlo Leakage Estimation (MCLE) and the pointers for $\pm 3\sigma$ variation with respect to the mean values obtained with the SLE-LUTPCC with spatial correlation $\beta = 1$ (pointer “R1”) and $0 \leftrightarrow \beta \leftrightarrow 1$ (pointer “R2”).

This method has been validated using the ISCAS85 Benchmarks circuits and the results had been corroborate using Monte-Carlo simulations of 10000 Random Process Variations for technological nodes of 65 nm. The result shows closed values of $\mu$ and $\sigma^2$ and maximum absolute errors of 0.1278 & 0.3801 for the min input pattern and 0.1247 & 0.2016 for the max input pattern. The computational time for the SLE-LUTPCC is between 21.7751 to 30.4285 seconds for the load of LUT for the complete set of ISCAS85. The Statistical Leakage Estimation of our method only takes less than 0.03 seconds for each ISCAS85.

V. Acknowledgments

This work was supported by the Mexican Council of Science and Technology (CONACYT) under a Ph.D. Scholarship to Raymundo Mendoza Vázquez. I would like to acknowledge helpful discussions and comments to R. Sanahuja, A. Ferré, S. Manich, L. Balado and J. Figueras from UPC.

VI. References


IV. Conclusions

We present in brief form a fast computation of statistical leakage estimation at circuit. In order to find the Statistical Lower and Upper Bound (LB & UB) the method is based on the Lookup Tables of Pre-Characterized CMOS Cells (LUTPCC). The LUTPCC takes in consideration correlations of process variations, input state and structure of 58 CMOS cells. The Intra-Die variations related to spatial correlations ($\beta$) also were considered for values of 1 and between 0 $\leftrightarrow 1$.  

Fig. 3 Histogram of Leakage present in ISCAS85 C17 and C7552 obtained in MCLE & pointers of Statistical Leakage Estimation using 65nm BPTM

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Non destructive characterization in air of plates using ultrasonic Lamb waves
Author: Mercedes Garcia, Thesis Advisor: Juan A. Chavez

I. Introduction
The aim of this Thesis is to contribute to the development of an air-coupled non destructive inspection system based on ultrasound waves (Lamb waves), in order to inspect and characterize plate materials of high commercial value in industrial environments.

Conventional ultrasound inspection has been a standard non-destructive testing method for a long time. In most cases, though, a liquid medium, such as water or gel, is used to couple the transducer to the sample. Unfortunately, the physical contact of some important materials with a liquid medium destroys its properties. In these cases, air-coupled ultrasound systems allow to test and evaluate materials where liquid couplants can not be used.

The use of air as a coupling media implies several benefits since measurements are carried out without contact with the surface of the material under inspection and consequently the transducers can be moved at relative high speed during the inspection reducing the test time. However, air-coupled ultrasound systems have two important drawbacks: attenuation of the ultrasound in air, and energy losses at the transducer–air interface (typically near 40 dB). Therefore, there is a need to improve the dynamic range of the system, to be able to inspect materials with great attenuation.

II. Thesis description
Lamb waves are elastic waves that propagate in a solid plate with free boundaries. The inspection technique consists of launching a plane wave to the surface of the plate with an angle such as to maximize the efficiency of the plate wave excitation. The angle is a simple function of the sound speed in air and the plate mode velocity, as can be seen in Fig. 7. If the material or its properties change, this implies a change on the plate mode velocity, and the optimum angle also changes. Consequently, the transducer angle must be adjusted to continue exciting efficiently the plate mode.

The concave geometry of the employed arrays permits to steer the acoustic emitted and received beams by simply choosing the physical aperture which central radius forms the desired angle with the normal of the plate surface, without any mechanical action. And it provides great advantages because the impact point is kept and no beam shape deformation exists, independently of the steering angle.

The system proposed is based on a 0.8 MHz concave ultrasonic transducer array (showed in Fig. 8) and its electronics which is able to generate and receive Lamb waves avoiding the mechanical transducer steering to coupling Lamb waves to the material surface, necessary in the traditional systems. The system will feature a real time adaptation to the solid media wave velocity and the possibility of selecting the Lamb wave mode without modifying the transducer array inclination to the material to be inspected.

The schematic diagram of the setup to test the plates is presented in Fig. 9 and a picture of the developed system is also showed in Fig. 10. As it can be seen, the system is composed by three main parts, emission, reception and control. A personal computer controls the system, in emission configuring the excitation and in reception capturing and processing the data. The transmitting transducer generates an ultrasonic wave travelling in air that impacts in the plate and generates a Lamb wave, which travels along the material. If the material changes or has any defect, the wave properties also change and can be detected when the received signal is processed.

But this process is too complicated or impossible in materials with high attenuation or when it is needed to...
inspect long distances, due to the attenuation and the insertion losses. To achieve this goal, it is necessary to increase the dynamic range. The main contributions of the thesis to increase the dynamic range are:

- Characterize the array to obtain the transducer electrical parameters of the Butterworth-Van-Dyke model, and optimize a matching network that maximize the transfer of power and improve the transmitting efficiency of the transducer.
- Design the electronic circuit needed to increase the signal power, and suitable to be employed with an array of 32 elements.
- Emit coded burst to improve the signal-to-noise ratio.
- Use signal processing techniques and pulse compression techniques (like Chirp and Golay codes) to increase the signal-to-noise ratio.

And Table 1 summarizes the group velocity values obtained for some measurements performed with stainless steel of different thickness.

<table>
<thead>
<tr>
<th>Thickness (mm)</th>
<th>Group velocity (m/s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.2</td>
<td>1793.3</td>
</tr>
<tr>
<td>0.25</td>
<td>1936.8</td>
</tr>
<tr>
<td>0.4</td>
<td>2348.6</td>
</tr>
<tr>
<td>0.5</td>
<td>2603.4</td>
</tr>
</tbody>
</table>

Table 1. Group velocity measurements in stainless steel 304, for different thicknesses.

As results of the thesis research, papers [1-5] have been published.

IV. Acknowledgments

This work has been supported by the research project DPI2008-05898 of the Ministry of Science and Technology of Spain.

V. References

Non-destructive evaluation of civil structures using electromagnetic waves
Author: Pablo Juan-García, Thesis Advisor: Josep M. Torrents

I. Introduction
One of the main challenges concerning the construction of infrastructures, such as the subway or railways for high speed trains, is the evaluation of big concrete structures. Nowadays, the vast majority of tests put into practice for quality control in civil engineering are destructive, which are generally tedious and costly. Consequently, increasingly more non-destructive testing methods are being developed.

Electromagnetic waves are suitable for this purpose since many physical parameters change in presence of moisture or metallic content (e.g.: propagation velocity, attenuation, scattering). Many of them can be estimated from the measurement of certain electrical magnitudes, as the complex permittivity or propagation losses. Monitoring physical or mechanical parameters of structures or materials through electrical parameters has plenty of advantages: electrical measures are non-destructive, usually easy to apply, safe and inexpensive (at least compared with other monitoring alternatives).

Previous works have reported the difficulties of measuring big samples by low frequency impedance measurements [1], so there is a need to use higher frequencies to determine the electrical parameters of interest. Until now, many authors have carried out different methods to determine the permittivity of non-homogeneous materials in the range of microwaves based either on reflection (open-ended coaxial lines [2], ground penetrating radar, time-domain reflectometry, etc.) or transmission techniques (antennas, two-port coaxial lines and more). However, only few of these laboratory experiences are of direct application to an in-situ situation, as the concrete needs to be surrounded or filled with the material under characterisation, whilst usually only one of the sides of the concrete is accessible, e.g. in dams, tunnels or big walls.

II. Purposes
The main aim of this work is to design a non-destructive method suitable for characterizing different materials used in civil structures, such as concrete, mortar or cement composites.

II.A. Moisture measurement
 Particularly in the case of dams, it is crucial to know the moisture level of the walls from the outer face in order to estimate possible damages caused by leaking. Our first aim is to design a planar sensor to determine the moisture level of a mortar wall by measuring its permittivity and loss factor.

II.B. Measurement of Steel Fibre Reinforced Concrete
Secondly, in the case of tunnels, the traditional reinforcement is being progressively replaced by fibres. Steel Fibre Reinforced Concrete (SFRC) has plenty of mechanical advantages but a main drawback: the absence of information about the real fibre content and its distribution and orientation inside the concrete bulk. Our second aim is to estimate the amount and orientation of steel fibres using a planar line as a sensor.

III. Measurement principle
The principle of the characterization of non-homogeneous media using a planar line lays on the propagation of a wave through a planar transmission line attached to the material under test. For a given geometry, half of the wave will pass through the sample and the other half through the substrate and the surrounding air. Therefore, the measurement of the time delay and the attenuation of the wave will provide with information about the material characteristics. In order to do that, a wideband frequency sweep is emitted along the line and then the transmitted wave ($s_{21}$) is processed using a Time Domain Transmission (TDT) technique thanks to an Inverse Fourier Transform.

Figure 1. Measurement setup.

Wideband measurements were performed using a Vector Network Analyser (VNA) sweeping up to 3 GHz. Data was acquired by a PC via GPIB connection, using a LabView automation driver. The measurements data was calibrated afterwards using a TRL algorithm (Thru-Reflect-Line), more suitable for planar structures than the traditional SOLT (Short-Open-Load-Thru).

The planar sensor was designed using an impedance transformer to adapt the $50 \Omega$ input to the higher impedance of the centre of the sensor with minimum reflection losses. The whole structure was simulated using a Finite Element Method. In Fig. 2 the field distribution can be seen, showing the penetration of the wave in the concrete and half the wave passing through air.

Figure 2. Simulation of wave propagation along the line.
IV. Main results

The geometry of the sensor depends on the needed frequency range and the desired penetration depth of the wave into the material. Therefore, different sensors can be designed depending on the application required. It has to be stated that the same sensor may be useful for a myriad of different applications of non-destructive characterization regardless of the kind of material.

IV.A. Moisture detection

The planar line was placed over a mortar slice just after casting it (Fig. 3). The bulk was then measured for 24 hours and the $S_{21}$ parameter was analysed to obtain the permittivity of the setup as well as its propagation losses. As expected, the permittivity tends to diminish as the mortar sets, because as the reaction takes place, there is less water in it. As water has a dielectric constant of 80 and mortar of 4, the permittivity decreases as the amount of water diminishes. Different setting stages are observed in the results [3].

![Figure 4. Evolution of the mortar sample during the first setting day (a) loss factor and (b) effective permittivity.](image)

IV.B. SFRC distribution

The measurement of the amount of fibres in the material under test is analogous to the measurement of moisture. By placing metallic (and so highly conductive) fibres on a hosting medium, both the amplitude and velocity of the transmitted wave decrease proportionally to the fibre content. Fig. 5 shows the results obtained from the measurement of fibres measured on air as an indicator of the capability of the sensor to detect fibre changes. In previous works [4], it was shown that the measured variance can be a deciding parameter to accurately estimate fibre content in concrete. Other alternative methods [5] followed a similar pattern.

![Figure 5. Detection of fibre content on air.](image)

V. Conclusions

In a number of different situations, non-destructive material characterization is currently highly demanded. As electromagnetic waves are suitable for this purpose, a planar sensor able to measure by only one side of the material under test was designed. The wideband measurements applied to construction materials showed good correlation with the physical parameters of interest particularly for moisture and steel fibre detection.

VI. Acknowledgments

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VII. References

Electromagnetic analysis in the time domain of complex structures using Finite Difference Time Domain

I. Introduction

In recent years electronic devices have increased and diversified, ranging from entertainment systems, control, security, safety, etc. Each of these systems usually has an associated communications path, either by cable or by a radio link, most of which are digital. The increased density of systems and buses also increases the probability of mutual electromagnetic interferences.

Nowadays, digital communication systems are very immune to continuous interferences, but their digital nature makes them vulnerable to impulsive noise [1]. For that reason it would be interesting to assess the immunity in the time domain when a transient appears.

One might think that the best way to do this is to perform measurements, but sometimes this is impossible, because of the cost and limitations of the equipment able to measure in the time domain with the required sensitivity and accuracy or because we are in an early design phase. For this reason, we propose to analyze the interference in an alternative way, the numerical methods.

In recent years several studies have been published to obtain the distributions of electromagnetic fields in complex structures based on numerical methods. However, most of the results have been published in the frequency domain, although in many cases using numerical methods that work in the time domain.

The work proposed in this thesis is to develop a methodology to predict, in the time domain and using numerical methods, to predict the electromagnetic behavior of a complex structure [2]. Particularly, we used the Finite Differences Time Domain (FDTD) method to be able to analyze the effect of electromagnetic interference caused by transients.

II. Contributions

The thesis highlights three important contributions:

a. Development of a new measurement method of high sensitivity and high bandwidth.

b. Development of a simulation methodology for transients in the time domain.

c. Development of a new validation method for the comparison of transients in time domain.

II.A. Measurement method

The easiest way to perform the measurements needed to validate the numerical simulations is to use the oscilloscope. This can only be done when the transients have enough amplitude but, usually, the levels of the transients involved in radiated EMC problems are too low for the oscilloscope’s sensitivity.

The method developed combines the RF spectrum analyzer (or EMI receiver) and the oscilloscope time domain ability and is presented in figure 1. This method uses the oscilloscope to acquire in time domain the signal after the IF stage of the frequency domain instrument. This produces a high sensitivity time domain measurement of the transient signal contained in the RBW of the spectrum analyzer [3].

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II.B. Simulation methodology

Our principal aim is to develop a correct method to simulate and analyze the transient interference. We select a vehicle as a complex structure. Among the different situations studied, we can highlight two:

a.- When the transient occurs in a monopole and we analyze the different interference couple on different monopoles located throughout the vehicle (figure 2a).

b.- When the transient occurs in cables and we analyze the interference couple in different places throughout the vehicle (figure 2b).

Figure 1. Measurement method developed.
II.C. Validation method

Today we can find several validation methods. The aim of all those methods is to quantify the similarity of two datasets, making them an objective tool for test engineers to discuss data on a similar base. It also has the possibility of a qualitative assessment of the ranked results to be interpreted as an expert opinion.

The method most used today for its versatility and simplicity in the field of EMC, is the feature select validation method (FSV). FSV method has the advantage of analysing and, at the same time, comparing two major aspects that are considered in any validation, the different levels of magnitude and the graph shape.

Normally, the transient pulses have a high peak of magnitude that decreases very rapidly in time. These particular characteristics make the FSV method is unable to interpret correctly the results.

To solve this, we propose a new method of validation of transient signals in time domain (TTDV). This method allows rapid and objective quantification of the simulations results. It is proposed to use four indicators to assess the parameters of the transition:

1. - Feature Difference Measure (FDM).
2. - Maximum Amplitude Levels (APL).
3. – Maximum Rate Time (MRT).
4. - Energy Contained in the Signals (ECS).

A fifth additional indicator (TEA) was developed to enable a quick and easy interpretation combining the last three indicators (amplitude, rate time, energy). In this way an overall assessment of the results can be obtained.

III. Results

The results obtained in the monopole (figure 2a) and the cable (figure 2b) configurations will be used to perform a comparison between the simulated and measured waveforms. This comparison will validate the simulations results. It is clearly observed in both graphs (Figure 3a and 3b) that the calculated and measured signals have a very similar trend. With the help of the TTDV method is possible to establish an objective comparison between the results.

IV. Acknowledgments

This work has been partially supported by the Spanish Ministerio de Educación y Ciencia under project DPI2007-63878.

I’m grateful to SEAT SA, Martorell, Spain for the help providing the Cordoba car frame to perform the measurements.

V. References


I. Introduction

Autonomous sensors (AS) are wireless measurement systems used in multiple applications from healthcare to environmental monitoring. Their active power consumption is in the milliamp level and, in order to reduce mean power consumption, they remain in sleep state (several microamps) most of the time. Consequently, they can be modeled as a low duty cycle pulse load.

In addition to the typical blocks that form the signal path (sensor, processor and transceiver; i.e. the load) an AS needs a power source:
- Primary batteries are by far the most prevalent power source currently used in AS. They can offer easy, reliable and cheap designs but no free of problems. Batteries have several unsolved issues such as: size, need for replacement (limited energy), determination of remaining capacity and proper extraction of the stored energy.
- Energy harvesting relies on extracting energy from the environment providing AS an almost perpetual operation with little or no maintenance. On the downside, energy harvesting raises circuit complexity and it is an ongoing research topic with some challenging issues.

This thesis addresses how to power autonomous sensors in an energy-efficient manner. Both alternatives, primary batteries and energy harvesting, are considered. Both options may need a power conditioning block (see Fig. 1) to match the supply voltage range of the load and to safely deliver the full energy available. On the other hand, energy harvesters need an energy transducer (e.g. solar cell) in order to convert the ambient energy to electrical energy. Then, an energy conditioning block is necessary to adapt the transducer output (ac or dc voltage or current source) to the ensuing block and extract maximum energy. Finally, the ambient power source variability (e.g. day/night periods for the sun) asks for a storage stage (Fig. 1) [1]. We propose to deal with two different ambient energy sources: Optical (dc source) and RF (radiofrequency, ac source). Optical energy presents high outdoor energy densities, hence it can power relatively high-power loads. RF energy can be beamed, as in RFID (RF Identification), or harvested from the environment.

II. Developed work

II.A. Hybrid Storage

Batteries, either primary or secondary, present an internal impedance that can be not negligible. Whenever the sensor node wakes up ($I_o$ in Fig. 2b), a significant power, and then energy, can be lost at this internal impedance ($R_b$ in Fig. 2a). Moreover, the voltage drop across the internal impedance ($I_cR_b$ in Fig. 2b) can prevent to squeeze all the available charge from the battery, thus leading to a reduction of the runtime of the sensor nodes. Capacitors have complementary characteristics to batteries. Their joint use can increase power capabilities of batteries and reduce the voltage drop ($\Delta V_o$ in Fig. 2b) at activation time. In [2] we analyzed theoretically and experimentally the performance of hybrid storage for AS and we proposed some design guidelines.

II.B. Optical energy harvesting

A solar cell delivers a dc current that can be easily, but not optimally, stored on a battery by just using a blocking diode. The power delivered by a solar cell versus the voltage presents a maximum power point (MPP in Fig. 3). This point varies with solar irradiation and temperature, so, in order to always work at MPP, an MPP tracker (MPPT) circuit is necessary.

![Figure 2. (a) Hybrid storage equivalent circuit and (b) voltage behavior under a pulsed load.](image)

![Figure 3. I-V and P-V characteristic of generic solar cell.](image)

![Figure 4. MPPT block diagram.](image)

![Figure 5. Block diagram of the power source of an Autonomous sensor (load).](image)
[3] we have proposed and implemented a new MPPT control method suitable for low power solar cells based on the power measurement at the input of the DC/DC converter during the sleep states of a commercial PFM converter.

II.C. RF energy harvesting

RF power must be collected by using an antenna. An antenna can be modeled as a low level ac voltage source with a series radiation resistance. The work developed up to now stores in a battery the energy from an UHF RF wave by using the Dickson charge pump as rectifier. A single stage rectifies and doubles the input voltage. Fig. 5 shows a two stage Dickson charge pump. The voltage generated at the antenna must be multiplied many times in order to achieve a useful output voltage. When using off-the-shelf components the number of stages is limited because of efficiency drops at low input powers. UHF RFID tags use CMOS and other integration processes to stack a great amount of stages with a reasonable efficiency.

Figure 5. Two stage half Dickson charge pump.

III. Experimental results

III.A. Hybrid Storage

Fig. 6 compares the discharge of a 25 mAh Lithium battery with that of a hybrid storage unit composed by the same battery and a 0.1 F supercapacitor. The load was a sensor node composed of a temperature sensor, a microprocessor and a transceiver. The hybrid storage unit achieved a longer runtime. The insets zoom in the load voltage at the activation time and show that voltage drop is reduced in more than ten times helping to squeeze the battery. Several more tests were carried out and hybrid storage units always achieved longer runtimes than single batteries.

Figure 6. Discharge profile with the lithium battery and the corresponding hybrid storage unit when using an AS as load.

III.B. Optical

The tracking efficiency of the MPPT method was over 99.6 % validating its effectiveness. Fig. 7 shows the overall efficiency of the MPPT circuit versus the PV power for several load voltages (e.g. battery). Efficiency is around 94 % which was mostly delimited by the chosen commercial DC/DC converter.

Figure 7. MPPT circuit efficiency versus input power.

III.C. RF

A signal of 868 MHz and 0.5 W (EIRP) transmitted power was radiated. Fig. 8 represents the obtained efficiency versus distance for a 2 and 3 stage Dickson charge pump with different antennas when charging a battery (2 V). A three stage rectifier with a 50 Ω antenna just gained a few centimeters if compared to two stages. As can be seen, efficiency at a distance higher than 0.5 m is better when using a folded dipole as antenna. This is due to the higher radiation resistance of this antenna (300 Ω) that helps to achieve higher input voltages for the same input power. Nonetheless, more work has to be done and an MPPT circuit is also in progress.

Figure 8. Efficiency versus distance from the RF source.

IV. Acknowledgments

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V. References


LAMB: a Simulation Tool for Air-Coupled Lamb Wave Based Ultrasonic NDE Systems
Author: José Luis Prego Borges, Thesis Advisor: Miguel J. García-Hernández

I. Introduction
Air-coupled ultrasonic Lamb waves represent an important advance technique in non-destructive testing and evaluation (NDT & NDE) of laminar materials and structures. Examples of these are characterization and assessment of plate like material properties in the industry, and location and/or monitoring of damage structures in airplanes and tanks.

However, the complex nature of mechanical vibrations encountered in acoustics, makes the subject of analysis and treatment, as a very difficult task.

Under these circumstances, the possibility to count with a simulation tool that permits evaluation and testing of different scenarios using the flexibility of a computer model, it's of an invaluable aid and advantage.

The objective of this thesis is to provide the field of acoustics with a free GNU simulation software: The LAMB Matlab® toolbox; that allows the simulation of a complete air-coupled ultrasonic Lamb wave based NDE system for ideal isotropic materials. In this respect the tool is aimed to explore different possible scenarios, and add a signal processing capability with help of a computer model.

The software is based around a pitch-catch philosophy for an NDE system, and it’s composed of three integrated core blocks which individually models a feature in the system: 1) Excitation, 2) Propagation, and 3) Reception.

II. Lamb waves: their role in NDT/NDE and key issues
Lamb waves are natural, two dimensional vibrations that occur in plates. They were first discovered by the English physicist Horace Lamb in 1917.

Intrinsically related to Rayleigh waves, which are also 2D vibrations that take place on the surface of half spaces; they can basically be classified into: symmetric, and anti-symmetric modes (see Fig. 1), and they can propagate long distances. This feature, have made Lamb waves to be very attractive for NDE of structures and laminar materials.

Since its discovery, they were subject of continuous studies an application attempts on the NDT/NDE arena to master their complex nature and interaction richness.

Main areas of application, as mentioned before, involve defect location and/or characterization of big structures (tanks, aircrafts, & ships), and assessment of quality properties during manufacturing of plates-like materials. In this respect non-contact ultrasound techniques are of an invaluable aid with materials that can not be touched, contaminated or wet, such as paper.

On the other hand, some key important issues to bear in mind when dealing with Lamb waves are:

Dispersion: they are dispersive waves. This means that the wave phase velocity (Cp) depends on frequency (f) in a non-linear way (see Fig. 2).

Attenuation: due material attenuation and the leakage effect (radiation into surrounding media), the amplitudes of waves decrease with distance.

Non pure modes: although “pure” mode excitation is made possible by an appropriate selection of the incidence angle, due to finite size of transducers, more than one mode could be excited with the excitation field.

Mode conversion phenomena: the existence of mode conversion phenomenons in the test piece (by the presence of defects, borders, impedance changes, etc.) can make the receiver detect signals that contains simultaneously, more than one Lamb mode present.

The air-coupled problem: due heavily attenuation of ultrasound in air (about 166.4 dB/m@1MHz), received signals are usually deep embedded in noise (average is required).

III. LAMB software modeling structure
The Basic structure of a developed Lamb wave based NDT system [1] could be appreciated in following Fig. 3.

![Figure 3. Schematic description of air-coupled ultrasonic Lamb wave based NDE system with concave 1D arrays.](image)
As it can be appreciated, the system is composed of two main electronic stages: Emission and Reception, plus two 1D air-coupled concave arrays (R=35mm) made of 32 rectangular piezoelectric elements [2].

Then the LAMB software recreates all of them, plus corresponding part to propagation on an ideal isotropic plate (see Fig. 4). These are described in the following:

III.A. Emission module

The emission module is build around a custom made acoustic field simulator: FIRST (Field Impulse Response Software). The simulator is based on the method of impulse response (IR) for rectangular apertures [3], and can compute radiated fields (see Fig. 5) by the concave arrays, including the air-attenuation effect.

III.B. Propagation module

The propagation module of LAMB toolbox is based around solution to the problem of an infinite ideal isotropic layer, excited by a time harmonic signal exerting pressure over a circular region. The so called time harmonic solution or THS.

Then, by assuming a double value (over surface of a plate), of emitted acoustic fields into air and by using a space-time superposition methods, any incident wide-band field profile can then be reproduced (see Fig. 4).

III.C. Reception module

Finally, the reception module is recreated by use again of the IR method for rectangular apertures, but this time on the plate’s radiation zone (see Fig. 4).

Then, by computing plate’s radiated acoustic field into the array reception zone, the whole NDE system can be modeled. These include further complementary issues such as: amplification, filtering, trace delay & re-sampling, and signal processing algorithms.

In this respect, the design and specification of a beamforming and/or any nonlinear filtering strategy (e.g. use of wavelets) is left open and can be added.

IV. Simulation results

Fig. 6 depicts an example of a full system simulation for a Rad. diagram in an AL plate using 10 eles. arrays.

V. Conclusion and future lines of work

A full air-coupled array based ultrasonic NDE Lamb wave based simulator “LAMB”, has been build in order to explore different excitation/reception strategies. While as a future work, signal processing and denoising algorithms are willing to be investigate and added. Obs: the LAMB Toolbox will soon be available for free downloading from author’s page at the MatlabCentral: www.mathworks.com/matlabcentral/fileexchange/authors/23152

VI. References

Fast Electrical Impedance Spectroscopy measurement techniques for dynamic bioimpedance characterization.

Sánchez, B., Bragós, R.

I. Introduction

The Electrical Impedance Spectroscopy (EIS) is a non-destructive measurement method to characterize biological materials and systems. In concrete, the study of a biological object whose electrical characteristics change quickly with time (lung, heart, etc) makes necessary to ensure that the bio-impedance measurement is free of the modulation associated to the intrinsic cyclic movement of the object under test. On the other hand, the acquisition of this modulation could add useful information about the tissue behaviour. Such kind of fast function transfer measurement is used in areas like Biomedical, Control, Acoustic, Microelectronics among others.

There are different signals for biomedical applications. One solution consists on using the classical frequency sweep technique. However, this technique is discarded when high-throughput data and real-time measurement are needed. In these cases, EIS should be acquired performing simultaneous measurements at different frequencies. Thus, it is necessary use broadband burst signals in order to acquire in a single shot burst the whole impedance spectra.

The application field is the cardiac tissue regeneration in regenerative medicine applications.

II. Broadband signals: Multitone fundamentals

The optimal waveform, using as a criteria the optimization of Signal to Noise Ratio at the measurement frequencies and a limited energy applied to avoid stimulation is the multitone signal. A multitone signal is composed by the addition of several tones with its own amplitude and phase. The design of frequency distribution and phases are critical to optimize the signal Crest Factor in order to obtain maximal SNR.

We proposed a new distribution based on a Bilateral Quasi-Logarithmic distribution for multitone signals optimized for the identification of impedance relaxations. Intermodulation effects are taken into account by applying a custom algorithm which shifts slightly the original tones to minimize the effect of non-linearities due to electronics and electrodes.

Fig. 2 depicts the spectral output of a multitone signal. Instead of spreading energy over the frequency range as does white noise or pseudo random binary sequences, most part of the multitone energy is focused at the measurement frequencies. This scenario gives as a result a better accuracy when estimating the amplitude and phase of the response.

As is shown in Fig. 3, if we compare the theoretical SNR obtained from a multitone versus frequency sweep based on a single carrier frequency we observe that they have the same slope but different y-axis crossing. This constant depends on how the multitone signal is distributed over the amplitude range. It can be calculated using the Crest Factor parameter, which is directly related with the phas angle distribution. Fig. 3 shows how for N bit converter with full scale input range, a small Crest Factor is preferred since it maximizes the SNR with the optimal case.

Crest Factor, also known in the communication’s literature as Peak Average Ratio (PAR), gives an idea of signal’s compactness and it depends on the multitone signal’s peak and its rms value. While the rms level is independent from the phas angle of the tone, the peak’s signal changes dramatically. We have developed a genetic algorithm for computing phase angle of a selectable number or tones of multitones when the goal is to identify impedance relaxations.
Comparing Fig. 2 and Fig. 3, we observe how theoretical SNR obtained from an ideal n-bit ADC converter does not match with the SNR value of the FFT. The reason is that FFT noise floor is not the SNR of the ADC, because the FFT acts like an analog spectrum analyzer with a bandwidth that depends on sampling frequency and number of FFT points. The theoretical FFT noise floor is therefore \(10 \log_{10}(M/2)\) dB below the quantization noise floor due to the processing gain of the FFT.

**III. Measurement Validations**

A FPGA based Arbitrary Waveform signal Generator (AWG) board has been designed, built and verified. First set up was carried out using the FPGA AWG, an oscilloscope as acquisition system and a PC for processing data [1]. We are currently working on a compact solution based on a PXI implementation for on-the-fly computing and monitoring bioimpedance time evolution. At this moment, a preliminary validation scenario has been built around the PXI adding a 4-electrode impedance measurement front end. Validations measurements have consisted on characterizing yeast suspension deposition over an interdigitated 4-electrode located at the bottom of a small bioreactor [2] by changes at impedance. Fig. 4 shows the impedance and phase changing with time.

Other measurement campaign has been done in collaboration with the “Grup de Recerca en Micro Nanotecnologies” MNT from the UPC. In this case, we have contributed to characterize biosensors [3] using multitone impedance measurement. A biosensor is a chemical sensor able to transform chemical information into an electrical signal related to the chemical phenomena. The goal of biosensors is to recognize specific biological elements by using antibody. The application field consists on the fast detection of small amount of pesticides in the food chain supply.

Biosensors impedance spectra characterization using multitone has been demonstrated as a reliable technique for detecting bacteria concentration and a proof of that is Fig. 5, which depicts changes according to different concentration of antibodies.

![Figure 4. Dependency of the magnitude and phase with time in biomass yeast suspension characterization.](image)

**IV. Future work**

Next steps are focused on implementing a multichannel front end for in-vitro cell cultures characterization. System will be able to measure in the impedance range 100Ω-10KΩ and in the frequency range 1KHz to 1MHz for simultaneous non destructive cell culture monitoring. The validation of the system will be carried out in in-vitro cell growing differentiation with myocytes precursors cultures obtained from stem cells characterized during in-vitro differentiation stages. Regarding to in-vivo measurements, an implantable system will be developed. The resulting engineered tissue will be characterized in-vivo after implantation in porcine models in collaboration with Institut Català de Ciències Cardiovasculars (ICCC) at Sant Pau Hospital.

**V. Acknowledgments**

The work has been supported by projects SAF2008-05144-C02-02 from MICINN and 080331 from Fundació La Marató de TV3.

**VI. References**


Figure 5. Immunosensor response obtained from a multitone burst characterization.
I. Introduction

Polymeric structures including microchannels and microwells were used in order to constrain neuronal geometry and ensure proximity of electroactive compartments to recording sites [1-4], for the recording and stimulation of neuronal activity in vitro. This thesis project consists to improve the polymeric structure and adapt it for culture cells to record the neural network electrical activity in vitro.

II. Description

The neurons are very similar to the electronic circuits: they can be represented as resistance and capacitors and they use electricity (and chemicals components) to communicate between each other.

II.A. The system

The polymeric structure consists in a polymer block with 2 wells and one microchannel as connection between them. The cells are constrained across the microchannel as shown in Fig. 1. The cells need medium for survive and this medium (inside of the wells) is electrically conductive, so this allow to us to introduce 2 electrodes in the medium to measure the electrical activity in the microchannel without touching the cells.

Right now it is possible to record from 40 different channels in simultaneous way (we use Multichannel Systems Amplifier for this task) that means 40 different cultures cells as shown in Fig. 2.

III. Results

We can record signals of the neurons that are constrained inside of the microchannel of the polymer block structure (Fig. 3).

The activity of all the cells that inside of one well are very similar between them and almost constant, but any external or internal change (temperature, ph, osmolarity, etc) can affect their activity as you can see in Fig. 4.

The electrical activity of each well is almost unique. Right now we are analyzing the data and making tests to set up the correct parameters to make drug screening.
IV. Acknowledgments

This project has been supported by “Departament d'Universitats, Recerca i Societat de la Informació de la Generalitat de Catalunya” and the Institut de Bioenginyeria de Catalunya.

V. References


Design of a multi-phase hysteretic regulator for low voltage applications
Author: Juan Cruz, Thesis Advisor: Miguel Castilla

I. Introduction

Efficient and optimization power delivery for next generation of multi-core high performance processors and multichannel memory systems, are the challenges required to achieve the high restrictions to design a Voltage Regulator Module (VRM). The challenges imposed for a VRM are a high current capability, low output voltage deviation in both steady-state and transient conditions, and high efficiency and optimal power delivery [1]. Multiphase interleaving techniques with voltage-mode and current-mode hysteretic control techniques can to match that challenges [2].

Different control approaches have been considered in the literature for VRM design. Classical solutions such as voltage-mode and current-mode control based in PWM (Pulse Width Modulation) techniques require PI (Proportional Integral) feedback loop compensation circuitry [3]. The dynamic characteristics of these controllers are relatively slow, due to actual limitations to the unity-gain bandwidth imposed by the switching frequency. The voltage-mode hysteretic control is one of the most appropriate solutions for powering microprocessor loads with high slew-rate current transients. Advantages of this control approach include simplicity and excellent dynamic characteristics. The controller does not have feedback loop compensation circuitry, thus it reacts in the switching cycle where the transient occurs. The hysteretic controller no has the restrictions on the conduction interval of the power switches, this is very important to decrease the recovery time of the output voltage after a current transient [4].

The classical hysteretic controller also has some drawbacks. The output voltage ripple is always higher than the fixed window of the hysteretic comparator, because of delays the switching frequency depends significantly on the power stage components, including output filter parasitic elements. The advanced voltage-mode hysteretic controller includes two sensing networks [5-6]. The switching frequency of this modified controller becomes invariable from optimal parameters controller and the output filter of the regulator.

Multiphase interleaving techniques has several advantages: lower output voltage ripple, harmonics current cancellation, current sharing with high current capability, and fast transient response. Combining the advantages of both techniques, voltage-mode hysteretic control and multiphase interleaving, will result in a efficient and high performance VRM [7].

II. Design of the multi-phase hysteretic regulator

Fig. 1 shows the general diagram of the proposed multi-phase hysteretic regulator, where each phase of the buck converter has its own advanced voltage-mode hysteretic controller. The power stage, include the power components and their respective parasitic elements. The large signal model of this multiphase regulator and the control model are explained in [7]. The controller senses the $v_{io}(t)$ of each phase and the output voltage $v_{o}(t)$ and the inductor current of each phase $i_L(t)$.

II.A. Hysteric controller design

The implementation of the model of control surface for the advanced voltage mode hysteretic controller is detailed in [7]. The optimal control parameters for the stability and optimal transient response of the output regulator can be determined using the design procedure explained in [7]. The parameters of each hysteretic controller also must satisfy the requirement of resistive output impedance.

II.B. Design example

The multi-phase hysteretic regulator shown in Fig. 1 has been designed according to the requirements given in [7]. A four phase power topology is chosen as good design trade-off between efficiency and cost. The solution to the example is listed in Table 1. The control parameters are calculated according to [7]. The parameters of the current equalization loop are selected by simulation.

![Diagram of the multi-phase buck regulator and i-phase hysteretic controllers.](image)

Figure 1. General diagram of the multi-phase buck regulator and i-phase hysteretic controllers.
Table 1. Summary of design parameters for a 4 phase hysteretic controller.

III. Simulation results

Fig. 2 shows the output voltage during a load step change from 0 A to 40 A. Note that output impedance is perfectly resistive given that no over or under shoots are noticeable in the output voltage waveform. Fig. 3 shows the four phase currents. Note that both the current equalization and the interleaving are preserved even during load transient.

IV. Experimental results

This section verifies the proposed control design procedure with selected experimental results. A prototype with a selectable number of active phases has been build. Fig. 4 shows the experimental load transient response for four-phase prototype. As it can be seen, the closed-loop output impedance is resistive given that no over-voltage or under-voltage is noticeable.

V. Conclusions

A multi-phase advanced voltage-mode hysteretic regulator has been proposed in this work. The advanced voltage-mode hysteretic controller has been designed and prototyped. The selected simulations and the experimental results demonstrate the validity of the proposed controller. With this laboratory prototype has been achieved the objectives of the proposed multi-phase hysteretic controller.

VI. References

Efficiency Improvement in Autonomous Electric Vehicles using Dynamic Commutation of Energy Resources.

Author: Julio García, Thesis Advisors: Rafael Pindado Rico, Ricard Bosch Tous

I. Introduction

Transportation is necessary. Autonomous transportation systems like trucks, cars or motorbikes are evolving from internal combustion motor (ICM) to an electric vehicle (EV). ICM causes air pollution, global warming and petroleum resource depletion. Then, this evolution or revolution is mandatory.

This evolution has slow pace mainly due to the limited autonomy and efficiency of these alternative systems. Battery limits autonomy. EV's efficiency is greater than ICM's. Furthermore, EV's torque is higher than ICM's even at very low speed. Consequently, it's necessary to make an effective control of the internal resources in order to maximize the efficiency [1].

Traditional grid distribution mains feed motors in industrial systems and trains using power converters. Besides, grid distribution mains always provide normalized voltage values in the power bus. Then, a rule of thumb arises that power converter feeding voltage is always constant (with tolerances). But, it is possible the use of a variable voltage bus to feed the power converters.

Starting motor does not require nominal voltage but it needs a peak current that is up to seven times the nominal current. A convenient combination of energy resources (series and parallel connection of batteries) can provide levels of voltage and current nearly matched to motor needs.

A variable bus voltage has some advantages and a few problems that should be studied. As an advantage, it is possible to make EV with the same autonomy with less battery, (space, weight and cost) or with the same battery, it is possible to increase the autonomy. Moreover, variable voltage bus may improve regenerative braking process. As a problem, the system has to manage, and also control, several energy sources and storage combinations.

The main goal of this PhD research is to demonstrate, with dynamic commutation of energy resources, the advantage of working with variable voltage bus rather than with a constant one. This variable voltage bus may increase the efficiency and the autonomy of the EV. This method and developed prototype behind variable voltage bus are subject to patent.

As a particular example of this PhD research, this communication shows acceleration process, from zero to nominal speed (1500 RPM), of a 1.5 kW squirrel cage motor using variable bus voltage. This characteristic of the power bus is obtained by series and parallel commutation of batteries.

II. Description of the work and methodology applied

To accelerate a motor from zero to nominal speed, power converters use the characteristic voltage frequency function depicted in black trace in Fig. 1. Discrete bus voltage values feasible to do this with sixteen 17 Ah 12 V batteries it is showed in red trace in Fig. 1.

Motor acceleration is a function of load and the torque. The evolution of bus voltage switching depends of the motor speed. Besides, it's possible to use a variable voltage bus to be greater than motor voltage requirements at each moment, red trace represents a voltage greater or equal as black trace in Fig.1. Finally, the green trace shows the voltage requirements to work the machine as a generator in a variable voltage bus.

As written below, discrete voltages were obtained from sixteen batteries arranged in two arrays (negative and positive) in order to minimize the maximum absolute voltage and provide also a real neutral point to the power converter who controls the electrical motor. Each array may deliver any discrete voltage multiple of individual nominal battery voltage.

To decide which battery is connected or disconnected to the power bus, additional information of each battery is required. The system control has to manage a few additional variables: evolution of the State of Charge (SOC) and evaluation the State of Health (SOH) of each battery. It is necessary to provide a shared control over the system, because each single control of battery does not know the complete system state.

The main battery control has a table to know the voltage required at each moment in function of accelerating or decelerating sequences and the information provided by the inverter. The inverter knows the motor speed due to an encoder inside the motor.
A main control system is needed to introduce the orders by the driver. It is also possible to connect to an SCADA. The main control system and several control algorithms are also subject to patent.

The constructed prototype uses 26 microcontrollers communicated across a CAN network. It was necessary to take special care to ensure a galvanic isolation of the CAN bus keeping the voltage references of the individual batteries. The batteries change their electrical position and consequently their reference values during operation.

In the battery arrays, like a common power bridge, there are some states that must be avoided because make a short circuit in power bus. Then, it is also important to study the commutation sequences used during the operation.

Figure 2. Block diagram of the system.

During the test sequence, different voltage levels were required.

During the test, control system managed to follow red trace in Fig. 1. voltage supplied by the battery arrays with small delays in each step change, the total delay required to commutate both arrays are less than 200 ms, and has not effect over the acceleration process. At the beginning, when motor started to rotate, current observed was roughly seven times the nominal motor current with a 10 kg, 30 cm diameter flywheel load in high acceleration levels. This amount of current decreases with soft acceleration levels. The current level needed for each acceleration level is also function of the mechanical load.

Along this acceleration process, it is possible to observe the current supplied by the batteries never reaches the nominal motor current, consequently the peak current needed by the motor at start or acceleration sequence it is supplied by the battery arrays, sharing the current needs and avoiding overload the batteries. Avoiding extra current peaks can also contribute to increase the autonomy and the battery life [2]. This is an extra advantage because the battery is an expensive part in the EV.

In industrial applications, the obtainable energy savings depends on the drive cycle, the kind of vehicle, the user needs, and many other variable characteristics. Then, the exact benefit is a function of the particular conditions of each situation or experiment.

The operation must be sure; the system is designed keeping electric, mechanic, electronic, and software security levels.

III. Results and conclusions

Fig. 3. shows the sliding operation of the squirrel cage motor in both operation (motor and generator). The inverter looks the speed encoder to follow the characteristic voltage frequency rising up the motor speed to the target value.

In the carried out experiments, we succeed in accelerating process from stop to the nominal 1500 RPM speed following the black trace showed in Fig. 1. 

The obtained results show that the proposal is reliable and the improvement is feasible.

IV. Acknowledgments

The main author wants to acknowledge to the “Dirección de Planificación y Calidad de Red de Endesa” and “Departamento de Formación y Recursos Humanos”. In addition, the author also wants to acknowledge to R. Pindado and R. Bosch as supervisors of the present thesis research work.

V. References

High efficiency RF power amplification for 3G mobile communications
Author: Lázaro Marco, Thesis Advisor(s): Eduard Alarcón

I. Introduction
Those late years, mobile communications systems have suffered an explosion of capabilities, produced by the hunger of bandwidth for multimedia extensions such as MP3, DIVX, and so on. On the other hand, the trend to integrate different devices in one, such as in the advanced mobile phones, has lead to further miniaturization, however, this trend in miniaturization and the increase of capabilities require a bigger energy density increase than the provided by battery evolution.
In order to allow going a further step beyond integration, it is mandatory to adapt efficient energy processing circuits and topologies, which require, as well as other things, the use of switching converters, both for voltage regulation and amplifying.
A further complexity is added because in the RF part, in order to increase bandwidth, the old but power-amplification-efficient constant-envelope modulations have to be left in order to adopt more bandwidth-efficient modulations, as shown in table 1. The main drawback of those high-performance modulations is that due to their non-constant-envelope nature, they cannot be amplified by means of a switching amplifier, requiring a linear amplifier, with a typical maximum efficiency up to 40%, which represents around 10% average efficiency, much lower than constant envelope designs which are up to 80% efficient. Considering that the RF transmitting part is one of the most power hungry of the complete terminal, the efficiency of RF power amplifier impacts severely on the overall terminal performance (autonomy).

<table>
<thead>
<tr>
<th>Standard</th>
<th>Channel Bandwidth</th>
<th>Data rate</th>
<th>Modulation</th>
</tr>
</thead>
<tbody>
<tr>
<td>GSM</td>
<td>200 kHz</td>
<td>14.4 kbps</td>
<td>GMSK</td>
</tr>
<tr>
<td>EDGE</td>
<td>200 kHz</td>
<td>384 kbps</td>
<td>8PSK</td>
</tr>
<tr>
<td>WCDMA</td>
<td>5 MHz</td>
<td>144 kbps-2 Mbps</td>
<td>Dual channel</td>
</tr>
<tr>
<td>802.11g</td>
<td>20 MHz</td>
<td>6 Mbps</td>
<td>BPSK</td>
</tr>
<tr>
<td>802.11g</td>
<td>20 MHz</td>
<td>54 Mbps</td>
<td>64QAM</td>
</tr>
</tbody>
</table>
Table 1: Standard list, applied to uplink channel.

II. Paradigm of High Efficiency Power Amplification
Several different alternatives have been proposed to achieve high efficiency and high linearity, however, this PhD is focused in the Envelope Elimination and Restoration technique (EER from now on), highly similar to the less efficient Envelope Tracking. Both techniques are based in the same schematic, depicted in Fig. 1.

The main principle is to divide the signal in its two polar components, envelope and phase, to amplify both of them in an efficient manner. When each of the two amplifiers is considered to be either linear or switching mode, there exist four different combinations as presented in table 2.

Please notice that the overall amplifier has to met requirements in terms of spectral distortion, (via spectrum mask, as shown in Fig. 2) and in terms of EVM, defined within the standard.

<table>
<thead>
<tr>
<th>Envelope Amp</th>
<th>Phase Amp</th>
<th>Efficiency</th>
<th>Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>Linear</td>
<td>Linear</td>
<td>Very Low</td>
<td>-</td>
</tr>
<tr>
<td>Linear</td>
<td>Switching</td>
<td>Moderate</td>
<td>EER (1)</td>
</tr>
<tr>
<td>Switching</td>
<td>Linear</td>
<td>Moderate</td>
<td>Envelope Tracking</td>
</tr>
<tr>
<td>Switching</td>
<td>Switching</td>
<td>High</td>
<td>EER (2)</td>
</tr>
</tbody>
</table>
Table 2: Different configuration options for Fig. 1 amplifiers

The Envelope Tracking topology can be seen as an adaptive biasing of a linear amplifier. The fact is that it increases the overall efficiency of the amplifier up to the maximum efficiency of the linear amplifier, which is much better than average linear efficiency, although it is still under EER capabilities.
On the other hand, Envelope Elimination and Restoration technique uses a RF switching amplifier which behaves as a multiplier regarding its supply voltage, thus allowing to provide the envelope information via supply port. When using a linear amplifier as an envelope amplifier (EER 1 in table 2), the efficiency is improved related to a single RF linear amplifier, such as class-A, although it still remains moderate.
Although the most promising configuration is the one based in RF and envelope switching amplifiers (EER 2 in table 2), it is the most difficult to implement, due to different implicit limitations that exist not only in both envelope and phase amplifier but also due to several topology issues such as delay mismatch.

III. Envelope Elimination and Restoration open challenges
When the implementation of the EER topology in which the envelope amplifier is a switching amplifier, there are several open challenges, namely:
A. The envelope switching amplifier itself, which requires the use of advanced topologies and control techniques in order to get rid of the numerous limits intrinsic to simple switching converter amplifiers.
B. The delay mismatch between the two signal paths (envelope and phase) has to be properly compensated in order to avoid mismatch between recovered envelope and phase, which causes very poor signal integrity when recovered.

C. The AM/PM distortion at the PA degrades system linearity if pre-compensation is not provided; therefore, an optimized design to diminish this distortion has to be done.

III.A. Envelope switching amplifier

Due to its intrinsic filter and switched operation, a combination of ripple and filtering affects the envelope. To minimize these effects, it is mandatory to increase the switching frequency, often reaching non-practical values leading to switching losses so high that render the overall EER amplifier useless. However, by increasing the complexity of the envelope amplifier, these limits can be overcome. Among other topologies and control techniques, it has been pointed the benefits in term of distortion by using higher level modulations than conventional 2-level PWM. The three-level buck converter depicted in Fig. 3 can decrease the switching effects, allowing a practical decrease in switching frequency requirements, as shown in Fig. 4.

III.B. Delay mismatch between polar paths

As the complete amplifier operates with two different polar paths any mismatch between them will degrade the overall characteristics of the complete amplifier. It should be pointed that due to the inherent low pass filter embedded in the envelope amplifier, the filter characteristics will affect as a delay, which should also be addressed. For instance, Fig. 5 shows the effects of a delay mismatch.

III.C. Distortion on the phase RF amplifier

The RFPAs usually are modeled from their RF input port to the output port, however, in EER application, the supply is also considered a port, requiring proper modeling, as it will affect to the output signal. One of the effects is the non-linearity from the supply to the output, defined as AM/AM distortion, it impacts on the quality of the recovered signal. Besides that, when the supply voltage of a switching RFPA is changed, the RF-input-to-RF-output delay also changes, adding a distortion known as AM/PM distortion, due to the impact of the supply port AM on the signal phase.

IV. Application of this technique

The EER technique can be applied to any non-constant envelope modulation with the benefits of increased efficiency, thus allowing longer runtimes between charges. To help to the EER application, standards can be modified, even developed bearing in mind the weak points of the EER technique, leading to increased performance, compared with regular standards, being able to achieve both high throughput and high battery efficiency. As an example, Fig. 6 shows the application of the EER topology to an actual EDGE modulated signal, with 880MHz carrier frequency. Notice how the adjustments of parameters allow fulfilling the standard specified mask.

V. Acknowledgments

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VI. References

Contributions towards adapting electronic technology courses to the requirements of the European Higher Education Area (EHEA): a systematic method
Author: Francesc J. Sànchez, Thesis Advisors: Miguel Valero, Pere J. Riu

I. Introduction

Digital and analogue electronics at university level have been taught ever since in a classical way in which the teacher is the one who have the expertise in the field and transmits the course content to a class of passive students in lectures. Today, considering the indications and the methodologies proposed by the EHEA, the traditional teaching method is no longer valid. Learning at higher education must be an active student-centred activity which has to tackle both, the acquisition of content and cross-curricular skills, which are precisely continually demanded by employers in our professional sector.

The research in this thesis aims to develop a new systematic design of instruction which aligns: learning outcomes including cross-curricular skills, problem solving, in and out of class active cooperative methodologies, student assessment and course evaluation. Fig. 1 shows the main concepts involved in our approach to teaching and learning.

II. Methodology

II.A. Learning objectives

The first step in designing instruction resides in specifying the course’s learning goals from the student’s point of view, which is never easy. They are subject to many changes in successive revisions, and there are of vital importance to establish the final activities by which students will learn. Once the new objectives considered, the subject’s syllabus became far more elaborated than in traditional teaching, as shown in Fig 2. Here you are a pair of examples of learning objectives:

1. “After completing the unit, students must be able to: plan and structure a top-down design of an standard sequential block like a counter or a register, analyse and simulate its electric characteristics, and compare commercial integrated circuits of the kind.”

2. “After completing the course, students must be able to: work effectively in teams for solving problems, distribute tasks, estimate their study time, and communicate effectively their results in written and oral formats.”

II.B. Learning by doing problems

The key point to fulfil the new objectives is the problem-based learning (PBL) strategy. All course activities go around solving the proposed “real world” problems or exercises and the application project as presented in Fig 3. Teacher role is guiding students through the solving process and student autonomy is introduced in stages depending on the students’ experience gained through the studies. Even in a single course, activities have to be paced so that students will start with instructor-guided problems, and end with problems planned and scheduled by the students themselves like in the application project.

Figure 1. The proposed 5-step student-centred systematic method of teaching and learning.

Experiences have been carried out to refine the system and take into account the many particularities of students at different levels (from freshmen to senior) and in various subjects in the area of electronic technology. Our approach, which finally has reached a structure consisting of a repeatable and adaptable pattern, has been to teach content through the use of some cross-curricular skills: teamwork, self-directed learning, and effective communication involving as well the English language.

II. Methodology

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Figure 3. Activities and the weekly study plan in and out of the class centered around the “problem” or exercise.
II. Cooperative learning in and out of the class

Cooperative learning derives its strength by defining base groups formed by putting students in a small team environment for the whole semester, as pictured in Fig. 4, for the purpose of learning together as a group (sink or swim together). In the classical method of lecturing, which is predominantly in use at UPC, a student learns in isolation or directly in competition with his or her colleagues. The cooperative approach represents a real change in the way teaching and learning is being conducted at the school. The five elements which define the cooperative learning are: mutual interdependence, individual accountability, face-to-face interaction, interpersonal and small group skills, and group processing [1]. Exactly as in problem-based learning, developing all these skills is not reasonable in a single semester. This is why our proposal consists in adopting our systematic methodology every semester until students develop their maximum competency once in senior courses.

II. D. Assessing students and the learning portfolio

Student learning assessment has to be continuous, formative and embedded into the task, therefore, there is no room left for classic final exams, which is of great satisfaction and relief. Exams have always been a source of never ending problems, discouragement and mistrust between students and instructors. Every course, teams prepare a final learning portfolio in which they assemble their best works and reflect about their achievements [2]. Fig. 5 shows the main items involved in the student assessment. Even though practically all activities are graded in group, controls of minimums allow us to check efficiently individual accountability in the cooperative team.

II. E. Course evaluation and reflection

All the experiences for implementing the new methodology have been carried out harvesting data systematically concerning the course evolution and academic results. For instance, an adapted version of the students’ evaluation of education quality (SEEQ) questionnaire, produces valuable information about which aspects of the course can be reconsidered for improvement in future editions of the courses. A web of resources containing learning materials and references from previous courses is kept constantly updated through the web [3].

III. Results

Results show that our approach to replace traditional lectures by an active student-centred teaching and learning environment based on real-world problems and cooperation among students, has been highly successful and accepted by our students and staff.

The author firmly considers, after analysing all the fundamental aspects of the research being carried out in this thesis, that the proposed methodology is highly effective in introducing the teaching changes required to adapt university studies to the requirements of the EHEA. We can definitively confirm that all our experience in the field of electronic technology, and in teaching content and cross-curricular skills in an integrated fashion, will be applied in teaching the subjects planned in the new Bologna-based 4-year bachelor degrees.

IV. Acknowledgments

This work, from 2003 to 2009, has been repeatedly sponsored by projects in Improving Quality in Teaching (MQD) of the Ministry of Universities, Research and the Information Society (DURSI), and the Agency for Administration of University and Research Grants (AGAUR) of the Generalitat, the Government of Catalonia. This work was also sponsored by the Technical School of Castelldefels (EPSC) and the Institute of Education Sciences ICE, UPC.

V. References


Ph.D. Thesis abstracts
2008/2009 academic year
Direct torque control of permanent magnet synchronous machines using matrix converters.

Author: Dr. Carlos Ortega García
Ph.D. Advisors: Dr. Antoni Arias, Dr. Cedric Caruana
Date: 23/10/2008

Abstract:

The control of AC machine drives is a continuously advancing subject satisfying increasing high performance applications demands. Induction Motor (IM) drives with cage-type machines has been the workhorses of industrial variable speed drives applications, including pumps and fans, paper and textile mills, electric vehicles, locomotive propulsion, wind generation systems, etc. In addition to performance requirements, energy saving aspects of variable speed drives is gaining attention nowadays.

Permanent Magnet Synchronous Machines (PMSM) are becoming a very attractive alternative to IM. Among other advantages, these type of machines offer higher efficiency, high power density and very fast dynamic performance. PMSM, in particular in the low power range, are already widely used in industry and recently, the interest in their application is growing, particularly up to 100 kW.

Variable speed drives fed by voltage source inverters has been traditionally employed in industrial applications. In the past few years, matrix converters have emerged to become a close competitor to the conventional inverter. A matrix converter is an advanced circuit topology capable of converting AC-AC, providing generation of load voltage with arbitrary amplitude and frequency, bi-directional power flow, sinusoidal input/output waveforms, and operation under unity input power factor. Furthermore, since no inductive or capacitive elements are required, MC allows a very compact design.

There are several methods to control AC machines, vector control methods being the most suitable for high performance demands. Among others, field oriented control and direct torque control are the most widely used. Although being one of the emerging control techniques for industrial applications, the direct torque control has some inherent drawbacks that are still being investigated by researchers. The work reported in this thesis is devoted to the investigation of direct torque control of PMSM drives fed by matrix converters.

This work considers the replacement of the conventional voltage source inverter by a matrix converter. The features of matrix converters are exploited to reduce the inherent electromagnetic torque and stator flux ripples arising from the direct torque control driving a PMSM. A new direct torque control using small and large voltage vectors of matrix converters has been developed during the course of this work.

The undesirable effects of the common mode voltage related with the utilization of the conventional voltage source inverter, like electromagnetic interferences and the machine early failures, are other issues with which this work is also concerned. A very simple algorithm to reduce the common mode voltage in direct torque control drives using matrix converters is developed and investigated in this work.

The main limitation of all sensorless vector control schemes, based on the conventional fundamental frequency models or observers, is that they fail at very low speeds. The desirability to operate continuously at low or zero speed has led to another sensorless approaches where the saliency of the machine is tracked through some form of signal injection to obtain flux or position information. A new algorithm to inject a rotating vector in the reference frame when employing a direct torque control has been developed in this thesis.
Dynamic range improvements of non destructive testing systems based in Lamb waves generated using air-coupled concave piezoelectric transducer arrays.

Author: Dr. Yago Yáñez Marco
Ph.D. Advisor: Dr. J.A. Chávez Domínguez
Date: 20/11/2008

Abstract:

The improvements performed in non destructive systems based in Lamb waves are presented in this thesis. In our case, the Lamb waves are generated and received using concave circular profile air-coupled piezoelectric transducer arrays.

Using air as ultrasound couplant implies increase very much the energy losses, but it increases the system flexibility, because no water or gel is needed to transmit the ultrasound waves. Being an array system, it is possible to steer the acoustic beam without moving the transducers. Its circular concave profile allows steering the beam without changing the beam impact point, if the plate is positioned in the geometric centre of the array.

Lamb waves are mechanical waves that can be only generated in plates; bulk materials with both free faces separated a similar distance than the Lamb wave wavelength. Lamb waves are dispersive (the propagation speed varies with the frequency) and multi-mode (more than one wave can be propagated in the same material at the same frequency, but with different propagation velocities). They have also a very interesting property, because using the wedge method to generate the Lamb waves, they have a preferential propagation direction, so they are not omnidirectional. This characteristic allows inspecting greater areas in less time.

One of the system critic points is its dynamic range. Air coupling implies a great loss increase, therefore a considerable amount of work have been devoted to increase the transmitting power, to reduce the receiving noise and to improve the signal processing to increase as much as possible the dynamic range.

To raise the effective transmission power, a new set of generator based in square wave burst has been designed and tested. This circuitry allows a better control over the signal bandwidth, keeping a simple circuit, basic to be replicated for each of the array transducers. The new system allows generating square pulses with amplitude up to 50 V.

To generate a Lamb wave is necessary to impact a plane ultrasonic wave front in the plate. Owing the fact that the array has concave profile, two delay laws have been used to generate the plane wave fronts from the array.

An analytic model of the piezoelectric transducer noise has been introduced. This model allows the selection of the best value for the reception circuitry components to minimize the output noise. The noise model is based in the Butterworth – Van Dyke impedance model of a piezoelectric transducer.

The digital processing system has been designed testing several filters and processing techniques. The mechanical parameters of the tested plates are strongly related with the Lamb wave velocity. Therefore, a critic point is the delay signal calculation used to calculate the Lamb wave velocity.

To test the validity of the presented improvements, a complete system that allows measuring plates of different thicknesses and materials. The inspected materials are copper, stainless steel 304, aluminium and polyester. The obtained results in the metallic plates are consistent with the theory, with errors in the velocities around 5%. Polyester is the material with a greater attenuation (13,7 db/cm), but the results couldn’t be validated due the great variation in the mechanical properties of the polymers.
CMOS architectures and circuits for MEMS control and signal conditioning.
Author: Dr. Daniel Fernández Martínez
Ph.D. Advisor: Dr. Jordi Madrenas Boadas
Date: 26/11/2008

Abstract:

In this thesis, architectures and CMOS circuits for controlling MEMS electrostatic actuators and for generating signals and perform signal processing tasks on microsystems are shown. In the first chapter, two circuits for estimating the capacitance or distance between plates are introduced, including their application in characterising the actuators static and dynamics, the failure and aging detection, the application as part of a pulsed digital oscillator and their use in a resonant low-voltage actuation system. Second chapter shows an analysis of the viability of monolithic integration of electrostatic actuators in the CMOS process using only a simple, low-cost, wet-etching procedure for releasing the structures.

In the third chapter, two CMOS, high-bandwidth and high-precision translinear elements are presented, including their application as multipliers, dividers, filters and as a part of a reconfigurable cell that is used for building an FPAA capable of performing the most common functions of analog signal processing. In the fourth chapter, some additional designs are shown, such as a control law capable of electrically adjusting all parameters that govern the electrostatic actuator movement and a digitally-controlled power converter based on an asynchronous finite-state machine. Finally, in chapter five, the final conclusions of this work are presented.
Tolerant cell for nanoelectrónica based computing.
Author: Dr. Ferran Martorell Cid
Ph.D. Advisor: Dr. Antonio Rubio i Solà
Date: 4/02/2009

Abstract:

For the last decades our life style has greatly evolved thanks to information technology. This technology is at the core of our society and it has been grounded on the design of electronic processing systems. The constant evolution of these devices depends on the continued refinement of the silicon MOS fabrication technology. Industry has been able to roughly double the device density every two years following Moore’s law. However, the use of silicon as the building material for high performance electronic devices is reaching to an end as the MOS device shrinks to its minimum theoretical dimensions. Recent predictions indicate the practical MOS limit is around 6 nm. Therefore, alternative technologies and computation paradigms need to be investigated to keep the technology evolution pace.

Emerging technologies promise device dimensions reduction down to 1-2 nm using devices based on single electron tunneling (SET), quantum effects, carbon nanotubes, molecules or DNA. These new technologies hold the promise of a device integration density increase of more than three orders of magnitude and, accordingly, an increase of system performance and functionality. However, it is also expected a dramatic reduction of several orders of magnitude on the device quality and, in general, on the operation reliability of circuits. The causes for this high error rate are inherent to the device’s dimensions. The improvement of the fabrication techniques is expected to alleviate this problem, but not completely solve it. Therefore it is widely acknowledged that fault and defect tolerant strategies will be required in future electronic systems.

The main objective of this work is to provide a gate architecture that increases the extremely low reliability of nanodevices in a structure feasible for being implemented. This objective is part of a larger objective to build a hierarchical fault tolerant structure able to provide reliable electronic systems out of extremely unreliable nanodevices. In this context this work proposes a solution to implement the first layer of such hierarchical tolerant system.

To achieve our goal we have identified the principal aggression sources to be: noise fluctuations, parameter variations and fabrication defects. We have analyzed the effects of these sources of variation and developed models to estimate the reliability of structures fabricated with nanoscale devices. These models have pointed out averaging as a feasible tolerant strategy for the nanoscale. Therefore, we have proposed an averaging cell structure and described how reliable logic gates can be built using those. Finally, we have shown that the proposed redundant structure can produce reliable gates (with error probabilities in the range $10^{-5}$ to $10^{-7}$) with an area cost between 1 to 2 orders of magnitude lower than NAND multiplexing. The averaging cells are based on a simple structure which ensures a low defect rate. In fact, similar structures have been already implemented.
Characterization of viscoelastic food masses by means of ultrasound.
Author: Dr. Javier García Álvarez
Ph.D. Advisor: Dr. Jordi Salazar
Date: 25/02/2009

Abstract:

This Thesis contributes to the development of measurement systems based on ultrasound techniques intended to the characterization of viscoelastic food masses. Moreover, the potential of the ultrasound measurement systems developed in this work in the characterization of two viscoelastic masses, dough and batters, has been analysed.

In many food industries, the analysis of the viscoelastic masses relies only on sensorial inspections carried out by a skilled operator. In other industries, the control of the masses is performed by means of methods with more scientific approach, such as rheology. Conventional rheology presents some drawbacks like the requirement of relative high cost equipment, which are usually slow and difficult to implement in a production line (off-line). In contrast, the measurement systems based on ultrasound are fast, low cost and hygienic, and can allow the performance of no-destructive analysis on the production line (on-line).

One of the main critical aspects of the ultrasound analysis of viscoelastic food masses is the very high attenuation that these materials generally presents, which hinders the performance of reliable and accurate measurements of some of their ultrasound parameters. Other aspect to consider is the relatively high quantity of air bubbles within some masses, which can strongly affect the measurement of their acoustic properties.

In order to perform reliable and accurate ultrasound measurements in a wide range of viscoelastic masses, the development of an ultrasound velocity, attenuation and rheology measurement system for the analysis of very attenuating masses has been proposed. The measurement system, based on shear waves, has been characterized and its main limitations have been identified. The application of several improvement actions has lead to a measurement system which allows the characterization of very attenuating materials (up to 450 dB/cm).

Moreover, the design and development of an acoustic impedance measurement system with low noise considerations for its application to the study of viscoelastic masses with very high gas content, such as batters, has been proposed. A design procedure, which gives relatively low noise geometries (SNR 43 dB) with only few equations and the observation of the signal given by a part of the sensor, has been described.

The potential of the developed ultrasound measurement systems in the quality control of viscoelastic food materials has been studied. The correlation between ultrasound measurements and conventional ones has been analysed for gluten-free dough and batters, without any known precedent in the scientific literature.

With regard to the characterization of gluten-free dough, the ultrasound system developed in this work is sensitive to the addition of enzymes (transglutaminase) and proteins (soybean isolated protein) in rice flour masses.

With respect to the analysis of batters, the acoustic impedance measurement offers significant correlation levels with quality parameters of the final product, especially high for parameters related to the produced expansion and the shape of the final product. Furthermore, the level of correlation is significantly higher in most cases than the offered by the traditional quality measurement in batters, based on its density determination, and higher than the obtained with the others conventional quality parameters in batters.

All these results show the feasibility of the ultrasound measurement systems developed in this Thesis for the characterization of dough and batters, with capability of extension to the study of other viscoelastic food materials.
Bidirectional inverters with high-frequency isolation for photovoltaic applications.
Author: Dra. Montserrat Mata Dumenjó
Ph.D. Advisors: Dr. Sergio Busquets, Dr. Joan Salaet
Date: 14/04/2009

Abstract:

The solar energy is a universal good and it is well distributed. That is why it is very interesting, particularly in places far from big energy facilities. One way to take advantage of this energy is to generate electric energy by using photovoltaic panels.

This thesis is focused on standalone photovoltaic installations, where electric energy is generated with photovoltaic panels, it is stored in batteries and then it is converted into standard ac.

In particular, the study focuses on the inverter, the element in charge of generating the alternate current from the continuous current of the battery in order to be able to use standard electric equipment.

With the aim to achieve more efficient, more compact and cheaper converters, two concepts are studied: bidirectionality of the energy flow and integration of high-frequency transformers.
To develop this task, the analysis and deployment of different converter families which are able to accomplish the specifications of the system are deployed and analyzed. The most compact element of family is studied in detail.

Several modulations for the converters are designed, for both CCM and DCM. These modulations must consider the transformer requirements and the reliability of the bidirectional energy flow.

Finally, different generic controls are presented, which allow driving the energy in both directions and connect the inverter to a generation set.
Study of dielectric charging effects on MEMS switches.
Author: Dr. David Molinero Giles
Ph.D. Advisor: Dr. Lluis Castañer Muñoz
Date: 13/05/2009

Abstract:

The microelectromechanical systems, known as MEMS, have been in the past few years an authentic revolution in the microelectronics area, based on the interaction between mobile parts and electrical signals in the micron scale. Furthermore, MEMS can be fabricated with the same technology as conventional CMOS devices, making them interesting in the technology market. There are many types of MEMS devices, but in this work we have concentrated on microelectromechanical switches. The main applications of MEMS switches are in the radio frequency range, as filters and phase shifters, or more recently in the optic area, such as mobile display. The microelectromechanical switches have many advantages with respect to conventional CMOS devices, such as low power consumption, linearity and low loss, but their commercialization is hindered by reliability problems. The MEMS lifetime is determined by mechanical and electrical problems, which dielectric charging is the most important, based on the charge trapped inside the dielectric that avoids a short-circuit when the switch is actuated.

In order to study the dielectric charging problem, several types of microelectromechanical switches have been designed and fabricated with two different dielectric materials: thermally grown silicon dioxide and deposited silicon nitride by plasma assisted. These dielectrics show different physical properties that help to quantify the switches reliability. The fabrication process is based on surface technology by placing different layers patterned to provide the final device. The MEMS process is limited by the sacrificial layer that forms the final beam shape, which is considered as a critical point. Thus, a new process based on a commercial photoresist has been developed that makes easy the fabrication itself and reduce costs.

The charge effects showed in the microelectromechanical switches are similar to those related to MOS gate problems investigated years ago. Thus, by using the same physical theory, we have developed a novel theory based on a dynamic model that uses the transient current to extract the dielectric physical properties and quantify the microelectromechanical switch. Furthermore, this theory is also used to study the reliability concerning different actuation modes. The test procedure consists in applying different voltage and current values and measuring the charging and discharging current. The discharge current provides information about the amount of charge trapped in the dielectric, trap energy level and the dielectric conductivity. These parameters have been used to create a novel figure of merit that provides a reliability parameter based on the dielectric and type of actuation used.
Energy harvesting from human passive power.
Author: Dra. Maria Loreto Mateu Sáez
Ph.D. Advisor: Dr. Francesc Moll Echeto
Date: 05/06/2009

Abstract:

The trends in technology allow the decrease in both size and power consumption of complex digital systems. This decrease in size and power gives rise to the concept of wearable devices which are integrated in everyday personal belongings like clothes, watch, glasses, et cetera. Power supply is a limiting factor in the mobility of the wearable device which gets restricted to the lifetime of the battery. Furthermore, due to the costs and inaccessible locations, the replacement or recharging of batteries is often not feasible for wearable devices integrated in smart clothes. Wearable devices are devices distributed in personal belongings and thus, an alternative for powering them is to harvest energy from the user. Therefore, the energy can be harvested, distributed and supplied over the human body. Wearable devices can create, like the sensors of a Wireless Sensor Network (WSN), a Body Area Network. A study of piezoelectric, inductive and thermoelectric generators that harvest passive human power is the main objective of this thesis. The physical principle of an energy harvesting generator is obviously the same no matter whether it is employed with an environmental or human body source. Nevertheless, the limitations related to low voltage, current and frequency levels obtained from human body sources bring new requirements to the energy harvesting topic that were not present in the case of the environment sources. This analysis is the motivation for this thesis.

The type of input energy and transducer form a tandem since the election of one imposes the other. It is important that measurements are done in different parts of the human body while doing different physical activities to locate which positions and activities produce more energy. The mechanical coupling between the transducer and the human body depends on the location of the transducer and the activity that is done. A specific design taking this into account can increase more than a 200% the efficiency of the transducer as has been demonstrated with piezoelectric films located in the insoles of shoes.

Acceleration measurements have been performed in different body locations and different physical activities, in order to quantify the amount of available energy associated with usual human movements.

A system-level simulation has been implemented modeling the elements of an energy self-powered system. Physical equations have been used for the transducer in order to include the mechanical part of the system and electrical and behavioral models for the rest of the components. In this way, the process of the design of the complete application (including the load and an energy storage element when it is necessary) is simplified to achieve the expected requirements. Obviously, the load must be a low power consumption device as for example a RF transmitter. In this case, it is preferable to operate it in a discontinuous way without a battery as it is deduced from simulation results obtained. However, the evolution in low power transmission modules can change this conclusion depending mostly on the evolution of the power consumption in stand-by mode and the configuration time in transmission operation.

It has been deduced from the analysis of inductive generators that time-domain analysis allows to calculate some magnitudes that are not available in frequency domain. For example, the maximum power can be calculated in frequency domain, but for energy harvesting applications it is more interesting to know the value of the recovered energy during a certain time, or the average power since the power generated by human activities can be highly discontinuous.

It has been demonstrated that energy harvesting transducers are able to supply power to present-day low power electronic devices as was demonstrated with a RF transmitter powered by a thermogenerator that employs the temperature gradient between human body and the environment (3-5 K) and that it is able to sense and transmit data once every second.
Autonomous sensor for the detection of static vehicles.
Author: Dr. Ernesto Sifuentes de la Hoya
Ph.D. Advisors: Dr. R. Pallas, Dr. J. Oscar Casas.
Date: 28/09/2009

Abstract:

The demand for a safe and smooth traffic flow in our roads in the face of ever increasing traffic volumes and a limited number of available roads and parking lot spaces, asks for the implementation of effective traffic management solutions able to guarantee the safety and efficiency of road traffic and to meet pollution control requirements. Time spent looking for a parking spot decreases if there is an accurate real-time inventory of available parking places. In order to prevent the congestion and parking problems from getting worse, particularly at rush hours, some governmental departments initiated the so-called Intelligent Transportation Systems.

The most important prerequisite for traffic management is information about the traffic flow and one way to obtain the required data is through vehicle detectors. These should ideally be small, sturdy, low power, easy to install and maintenance-free. Currently available vehicle detector systems are based on the classical inductive loop, magnetic, ultrasound, and infrared sensors. They are mainly applied in parking management systems where there is a sensor above each parking spot, connected into a wired network. Those sensors are expensive, powerhungry and expensive to deploy and maintain, so they are not suitable for sensor nodes in wireless sensor networks.

Because of the very high deployment and maintenance costs, wired sensors networks to cover large areas would be impractical. It is far more economical and power-efficient to use battery-powered sensor nodes and wireless communications. Wireless sensor network is a technology that combines networking software with ultra low-power sensor nodes and radio transceivers to enable sensor applications on a density and scale that were unthinkable of twenty years ago. However, wireless sensor networks will probably be an integral part of most ITS systems in the near future.

This dissertation presents the conception, design and implementation of a wireless vehicle detector (sensor node) to detect the presence of a vehicle in a predetermined zone. The sensor node proposed includes two passive sensors: magnetic and optical. Magnetic sensors based on magnetoresistors are quite sensitive and can detect magnetic anomalies resulting from the presence of a car. However, they can be fouled by a close magnet, or another ferromagnetic material, and its continuous operation implies large power consumption. Optical sensors can detect a reduced illumination resulting from the presence of a car, or any other object. However, they can be designed to consume very little power. As a result, combining both sensors can result in a sensitive but also specific and low power sensor node. This goal has been achieved by designing new interface circuits and software detection algorithms, and by applying power management strategies. The result has been a vehicle detector that is simple, compact, low power, and easy to install and maintain.

Theoretical and experimental analysis show that resistive sensors in quarter, half-, and full-bridge configurations can be directly connected to a microcontroller without using any analogue integrated circuit in the signal path. Such a direct interface circuit relies on measuring the discharging time of an $RC$ circuit network that includes the resistances of the bridge. This interface circuit is a simple, compact, low-cost, and low-power solution for wireless sensor nodes intended for measurement and control systems in many application areas such as industrial automation, remote metering, building and home automation, automotive networks, and vehicle detection and traffic data. Further, we show that life-time of the sensor node is greatly extended by using software and hardware based on events.

The wireless sensor node proposed is a very attractive alternative to inductive loop detectors. Wireless sensor networks are reconfigurable, which makes the system scalable and deployable everywhere in existing or new traffic and parking networks, at a much lower life-cycle cost than inductive loops, ultrasound and infrared detector systems. Further, also sensor networks are cost-effective to cover large areas. Wireless communication allows the interchange of traffic parameters between different ITS systems. Because sensor nodes are located on the pavement, a multifunction wireless surveillance system could be deployed by adding other sensor modalities to the ITS. For example, to sense road conditions such as temperature, snow, moisture, and pollutants. All this information could the basis for an accurate, real-time inventory of available parking places, road conditions and traffic statistics systems.
Development and validation of the thermal diagnostics instrumentation in LISA pathfinder.

Author: Dr. Josep Sanjuan Muñoz
Ph.D. Advisors: Dr. Juan Ramos, Dr. J. Alberto Lobo.
Date: 28/09/2009

Abstract:

This thesis focuses on the issues related to the thermal diagnostics aboard the space mission LISA Pathfinder (LPF). LPF is a technological mission devoted to put to test critical subsystems for the LISA mission. LISA will be the first space born gravitational wave (GW) observatory with the main objective of detecting GWs. GWs are ripples of the space-time geometry caused by acceleration of masses in an asymmetric way. Their detection requires put test masses (TMs) in an almost perfect inertial frame (or free fall).

Non-inertial forces perturbing the TMs must be less than 6 fN/sqrt(Hz) in the frequency range of 0.1 mHz to 0.1 Hz and the noise in the measurement between the TMs (separated by 5 Gm) must be of 40 pm/sqrt(Hz) in the same band. To reduce the risks of a direct launch of LISA, ESA has decided to first launch LPF to put all the LISA technologies to test. The payload of LPF, the LISA Technology Package (LTP), contains two TMs placed in two cylinders inside a single spacecraft (SC) and an interferometric system that measures the relative distance between them. The SC isolates the TMs from the external disturbances but internal stray forces will still perturb the TMs. Their levels must be bounded not to challenge the free fall accuracy. One of these disturbances is temperature fluctuations and the aspects related to their measurement are the leitmotif of this thesis. In chapter 1 we have presented how temperature fluctuations couple into the key subsystems of the LTP to degrade their performance. The foreseen effects are radiation pressure, radiometer effect, temperature coefficient of optical components, etc.

The task of the thermal diagnostics in the LTP is twofold: on the one hand, temperature fluctuations in different subsystems must be measured with noise levels of 10 microK/sqrt(Hz) in the LTP band. On the other hand, a set of heaters will generate heat pulses that in conjunction with temperature measurements will be used to estimate the actual coupling between temperature and Systems performance. These actions will provide information on the behavior of the system and will permit to identify the fraction of noise in the system coming from temperature issues. The main function of LPF, as precursor mission of LISA, is the understanding of all the noise sources in the system. This will provide clues to the final leap from LPF sensitivity to LISA one.

The main investigations carried out during this thesis can be split into three main categories: (i) the design and validation of the LTP temperature measurement subsystem (TMS); (ii) the extension of the system to the LISA requirements; and (iii) the analysis of the in-flight thermal experiments in the LTP. The thesis is organized as follows: in chapter 2 we describe the designed electronics and the temperature sensors chosen. Aspects related to the coupling of the TMS with other subsystems nearby are discussed in chapter 3. Chapter 4 focuses on the design of the testbed needed for the validation of the TMS. Two different testbeds are described: one for the LTP measurement bandwidth (MBW) and another one for the LISA MBW, 0.1 mHz. In chapter 5 we present the results of the test campaigns: the prototype, the engineering model and the flight model systems were put to test. The results of the investigations in the LISA band are also shown. Chapter 6 contains investigations in view of LISA requirements to reduce excess noise at very low frequency and to reduce the floor noise of the measurement. Chapter 7 focuses on the thermal experiment on-board LPF: a set of thermal excitations are proposed to extract information of the thermal behavior of the key subsystems of the LTP.
The Doctoral Program in Electronic Engineering
2008/2009 academic year

This Doctoral Program is jointly organized by the Electronic Engineering Department of the Universitat Politècnica de Catalunya (UPC) in Barcelona and the Physics Department of the Universitat de les Illes Balears (UiB) in Palma de Mallorca. The goal of the program is to offer highly motivated graduated students the possibility to extend their education in the various fields of research related with Electronic Engineering. The academic activities of the program are designed both to introduce the students to highly specialized research topics and to extend their skills with methodologies oriented to the tasks, tools and procedures required to develop a high quality research activity. The Doctoral Program is closely linked with the Electronic Engineering Master, which is jointly organized by the TelecomBCN School at UPC and the Physics School at UiB. The courses and other activities offered in the framework of the Electronic Engineering Master provide the students enrolled in the Doctoral Program the necessary academic background for efficiently perform the research work in their Ph.D. Thesis.

<table>
<thead>
<tr>
<th>The program in numbers (2008/2009 academic year)</th>
<th>UPC</th>
<th>UiB</th>
</tr>
</thead>
<tbody>
<tr>
<td>New students</td>
<td>25</td>
<td>11</td>
</tr>
<tr>
<td>Students in the training period</td>
<td>17</td>
<td>12</td>
</tr>
<tr>
<td>Students in the research period</td>
<td>73</td>
<td>1</td>
</tr>
<tr>
<td>Thesis proposals</td>
<td>20</td>
<td>-</td>
</tr>
<tr>
<td>Ph.D. thesis presented</td>
<td>10</td>
<td>-</td>
</tr>
<tr>
<td>Total number of students 08/09</td>
<td>100</td>
<td>13</td>
</tr>
</tbody>
</table>
During their Ph.D. thesis research the students are hosted in one of the 14 research groups with more than 16 research laboratories and facilities that cover a wide range of specialties in four main fields of investigation: Integrated Circuits and Systems, Industrial and Power Electronics, Measuring and Instrumentation, and Semiconductor Devices and Microsystems.

<table>
<thead>
<tr>
<th>Research groups</th>
<th>Contact person</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Semiconductor Devices and Microsystems</strong></td>
<td></td>
</tr>
<tr>
<td>MNT- Micro and Nanotechnologies</td>
<td>Dr. Luis Castañer, <a href="mailto:castener@eel.upc.edu">castener@eel.upc.edu</a></td>
</tr>
<tr>
<td><strong>Integrated Circuits and Systems</strong></td>
<td></td>
</tr>
<tr>
<td>HIPICS- High Performance Integrated Circuits and Systems</td>
<td>Dr. Antonio Rubio, <a href="mailto:antonio.rubio@upc.edu">antonio.rubio@upc.edu</a></td>
</tr>
<tr>
<td>AHA- Advanced Hardware Architectures</td>
<td>Dr. Joan Cabestany, <a href="mailto:cabestan@eel.upc.edu">cabestan@eel.upc.edu</a></td>
</tr>
<tr>
<td>QINE- Low Power Design, Test, Verification, and Fault Tolerance</td>
<td>Dr. Joan Figueras, <a href="mailto:figueras@eel.upc.edu">figueras@eel.upc.edu</a></td>
</tr>
<tr>
<td>GTE- Electronic Technology Group</td>
<td>Dr. Jaume Segura, <a href="mailto:jaume.segura@uib.es">jaume.segura@uib.es</a></td>
</tr>
<tr>
<td><strong>Measuring and Instrumentation Systems</strong></td>
<td></td>
</tr>
<tr>
<td>GSS- Sensor Systems Group</td>
<td>Dr. Miguel García, <a href="mailto:mgarcia@eel.upc.edu">mgarcia@eel.upc.edu</a></td>
</tr>
<tr>
<td>IEB- Electronic and Biomedical Instrumentation</td>
<td>Dr. Xavier Rosells, <a href="mailto:jrosell@eel.upc.edu">jrosell@eel.upc.edu</a></td>
</tr>
<tr>
<td>SARTI- Remote Acquisition and Data Processing Systems</td>
<td>Dr. Antoni Manuel, <a href="mailto:antoni.manuel@upc.edu">antoni.manuel@upc.edu</a></td>
</tr>
<tr>
<td>ISI- Instrumentation, Sensors and Interfaces</td>
<td>Dr. Ramon Pallas, <a href="mailto:ramon.pallas@upc.edu">ramon.pallas@upc.edu</a></td>
</tr>
<tr>
<td><strong>Industrial and Power Electronics</strong></td>
<td></td>
</tr>
<tr>
<td>EPIC- Energy Processing and Integrated Circuits</td>
<td>Dr. Alberto Poveda, <a href="mailto:poveda@eel.upc.edu">poveda@eel.upc.edu</a></td>
</tr>
<tr>
<td>MCIA- Motion Control and Industrial Applications</td>
<td>Dr. Luis Romeral, <a href="mailto:luis.romeral@mcia.upc.edu">luis.romeral@mcia.upc.edu</a></td>
</tr>
<tr>
<td>TIEG- Terrassa Industrial Electronics Group</td>
<td>Dr. Josep Balcells, <a href="mailto:balcells@eel.upc.edu">balcells@eel.upc.edu</a></td>
</tr>
<tr>
<td>SEPIC- Power and Control Electronics Systems</td>
<td>Dr. J.L. García de Vicuña, <a href="mailto:vicuna@eel.upc.edu">vicuna@eel.upc.edu</a></td>
</tr>
<tr>
<td>GREP- Power Electronics Research Group</td>
<td>Dr. Josep Bordonau, <a href="mailto:bordonau@eel.upc.edu">bordonau@eel.upc.edu</a></td>
</tr>
</tbody>
</table>

The Electronic Engineering Department leads the following multi-disciplinary research centers at the Universitat Politècnica de Catalunya:

**CETpD**: Technical Research Center for Dependency Care and Autonomous Living.  
Contact person: Dr. Joan Cabestany (cabestan@eel.upc.edu), web: [http://www.upc.edu/cetpd/](http://www.upc.edu/cetpd/)

**CRNE**: Center for Research in NanoEngineering.  
Contact person: Dr. Ramon Alcubilla (alcubilla@eel.upc.edu), web: [http://www.upc.edu/crne/](http://www.upc.edu/crne/)

**PERC**: Power Electronics Research Centre.  
Contact person: Dr. Josep Bordonau (bordonau@eel.upc.edu).