4 mm and \( L_p = 3 \) mm, the first and third resonances occur at 1.82 and 2.04 GHz, respectively.

As seen in Figure 1(b) and (c), the fabricated antenna is sitting on the left upper corner of FR4 substrate (66 \( \times \) 30 \( \times \) 1 mm\(^3\), \( \varepsilon_r = 4.2 \)) in consideration of its placements in a handset. The antenna is fed by 50\( \Omega \) grounded coplanar waveguide (CPW) input line.

3. RESULTS

In order to validate the behavior of the proposed antenna, numerical simulation has been carried out with Microwave Studio\textsuperscript{TM} (MWS). The fabricated antenna with the selected dimensions was measured using an Agilent 8510C Network Analyzer. The measured and simulated return losses are compared in Figure 2 and are in reasonably good agreement with each other. From the measured results, it is seen that the operating frequency is in the range of 1.75–2.17 GHz with impedance bandwidth of 21.4\% at VSWR < 2.0. It is confirmed that the proposed antenna can be used in the KPCS/IMT-2000 dual band.

Radiation patterns have been simulated and measured at the frequency of 1.89 GHz. The simulated and measured radiation patterns of the \( x-z \) and \( y-z \) planes are shown in Figure 3(a) and (b), respectively. As seen in Figure 3, there is good agreement between the measured and simulated results. Note that the radiation patterns are approximately omnidirectional and similar to that of a monopole antenna. Both simulated and measured antenna gains in the \( x-z \) plane have 2.6 dBi.

4. CONCLUSION

It has been demonstrated that the proposed antenna with branch structure provides a wide impedance bandwidth of 21.4\% based on VSWR < 2, maximum measured gain of 2.6 dBi, and an omnidirectional radiation pattern similar to that of a monopole antenna. Its advantages in terms of the cost, size, and ease of surface-mount assembly are attractive features for KPCS/IMT-2000 applications.

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REFERENCES


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Key words: on-wafer noise source; excess noise ratio; small-signal model; noise model

1. INTRODUCTION

Noise sources based on active devices such as FETs in a one-port configuration have been proposed in the literature [1–3] as an alternative to avalanche-noise diodes (normally included in coaxial and waveguide noise sources) [4, 5] and other devices [6]. In [1], a FET is used as an equivalent “cold” source, and more recently a FET-based cold/hot noise source [2] has been proposed, where the selection between states is obtained through device-bias control and switching the device input port between the gate-source and drain-source ports, respectively. To extend the operating bandwidth, a MMIC active cold load has been proposed [3], composed of two MMIC cold-load circuits designed to cover the 2–10-GHz and 10–26-GHz ranges, respectively. While FET-based noise sources present the advantage of being easily compatible with microwave on-wafer measurement systems [7], it is necessary to know their excess noise ratio (ENR) in a wide frequency range, in order to be able to calibrate the noise receiver. To determine the noise-source ENR, usually its output-noise temperature is measured with a receiver previously calibrated, using a well-known room-temperature and/or cryogenic noise reference [1–4, 6]. In a preceding work [5], it has been shown that equivalent noise models for the noise devices are useful in the determination of their ENR, because they help to reduce measurement uncertainty, in particular, when the device’s reflection-coefficient magnitude is high, as occurs in unmatched on-wafer FET or avalanche-diode-noise sources.

In this paper, a method to extract the noise circuit-model of a cold-FET \((V_{ds} = 0)\) with a reverse-biased gate is presented. The cold-FET is used as an on-wafer “hot” noise source in a one-port configuration, with the gate-source port as the output noise port, while the drain-source port is loaded with an arbitrary reflection coefficient. The model is used to estimate the device noise temperature and, therefore, characterize its ENR. The noise analysis is performed from noisy networks theory in order to derive an expression for the device output’s noise-current spectral density as a function of its intrinsic noise sources. Then, using broadband \(S\) parameters and noise-power experimental measurements as a function of frequency, a regression technique is applied for the best fit between the measured and estimated “multiplier” factor \(M\) associated to the noise sources, in order to “estimate” the device’s ENR, thus reducing the measurement uncertainty. Experimental results of the estimated \(M\) and ENR of a 2 × 50 \(\mu\)m gate-width DPD-SQW HEMT up to 40 GHz are presented and applied to perform full receiver noise calibration.

2. NOISE MODEL FOR A REVERSE-BIASED “COLD”-FET

Figure 1 shows the small-signal equivalent circuit of a cold-FET \((V_{ds} = 0)\) with the gate reverse-biased \((V_{gs} < 0)\), including the noise sources associated with the passive components and two intrinsic uncorrelated noise sources associated with the gate-source and gate-drain diodes, \(I_{gs}\) and \(I_{gd}\), respectively [7]. It is assumed that all passive components, except \(L_g\) and \(C_{gd}\), introduce thermal noise. The noise-current spectral density of the gate-source noise source can be expressed as [7]:

\[
\overline{I_G^2} = 2qI_{GS}M^2
\]

where \(I_{GS}\) is the gate-source DC-bias current, \(q\) is the electron charge, and \(M\) is a breakdown multiplier factor that has a low-pass frequency dependence [9]. An analogue expression can be written for the gate-drain diode. Note that if the FET layout is symmetrical with \(I_{GS} = I_{GD}\), the breakdown multiplier factors and the current spectral-densities are the same \((\overline{I_G^2} = \overline{I_D^2}\)).

2.1. Extraction of the Small-Signal Equivalent Circuit Elements

The extrinsic elements, \(R_g, R_d, R_{gs}, R_{gd}, L_g, L_d, C_{gs}, C_{gd}\), and \(C_{pg}\), represent the access and contact resistances and the pad effects, and they are assumed to be bias-independent. To obtain these elements, first the transistor is pinched-off, and \(C_{gs}, C_{gd}\), and \(C_{pg}\) are computed from the imaginary part of its \(Y\) parameters using the method proposed in [10]. Then the transistor is forward-biased \((V_{ds} > 0, V_{ds} = 0)\), and \(L_g, L_d\), and \(I_{gs}\) are computed from the imaginary part of its \(Z\) parameters, and \(R_{gs}, R_{gd}, R_{gd}\) from the real part of its \(Z\) parameters using a procedure similar to [11].

Since the extrinsic elements are known, the intrinsic \(Y\) matrix, \(Y\) (Fig. 1), is readily obtained, and the intrinsic parameters are calculated from identification with \(\pi\)-branch admittances \(Y_{gs}, Y_{gd}\), and \(Y_{dr}\). Elements \(R_{ds}\) and \(C_{ds}\) are computed from the real and imaginary parts of \(Y_{dr}\), respectively. The junction resistances \((R_{gs}, R_{gd})\), intrinsic capacitances \((C_{gs}, C_{gd})\), and channel resistances \((R_{gs}, R_{gd})\), are estimated from admittance \(Y_{gs}\) and \(Y_{gd}\) as functions of the frequency. The frequency dependence of \(Y_{gs}\) is:

\[
\frac{1}{Y_{gs}} = Z_{gs} = \frac{(R_{gs} + R_{pg}) + s(R_{gs}R_{pg}C_{gs})}{1 + sR_{gs}C_{gs}},
\]

where \(s = j\omega\), \(\omega\) is the angular frequency, \(i = 1, \ldots, N\) is the frequency index, and \(N\) is the number of measured frequency points. An expression similar to Eq. (2) can be written for \(Y_{gd}\).

From Eq. (2), a linear equation system is obtained:

\[
[Z_{gs}] = [\begin{bmatrix} R_{gs} + R_{pg} & R_{gd}R_{pg}C_{gs} \\ R_{gs}R_{pg}C_{gs} & R_{pg} \end{bmatrix} \cdot [R_{gd}, C_{gd}]].
\]

The system of Eq. (3) is solved for \(R_{gs} + R_{pg}, R_{gs}R_{pg}C_{gs}\), and \(R_{gs}R_{pg}C_{gs}\) using the pseudo-inverse method. The results are used as initial estimates in an iterative Newton gradient-conjugate method to obtain the final values.
2.2. Noise Model

The procedure to obtain a noise model of the reverse-biased cold-FET is based on determining its total noise correlation matrix in admittance configuration, \( C_{Y}^{\text{TOT}} \) (see Fig. 1) and its equivalent output noise current spectral density, \( \bar{I}_{o} \). To obtain \( C_{Y}^{\text{TOT}} \), first the expression for the “admittance” noise correlation matrix \( C_{Y}^{\text{admit}} \) is written in terms of the gate and drain noise-current spectral densities, \( \bar{I}_{g}^{2} \) and \( \bar{I}_{d}^{2} \), respectively, as shown in Figure 1.

In Eq. (5), \( Y_{g} \) and \( Y_{d} \) are the \( \pi \)-branch admittances, where the former is given by Eq. (2) and a similar expression can be written for \( Y_{d} \) and \( Y_{s} \) are the gate-source and drain-source diode admittances, respectively, as shown in Figure 1.

Next, the intrinsic admittance noise correlation matrix \( \mathbf{C}_{Yd}^{\text{admit}} \) is transformed into the “impedance” representation and the thermal-noise sources of the parasitic resistances, \( \bar{e}_{g_{s}} = 4T_{a}kR_{g_{s}}, \bar{e}_{g_{d}} = 4T_{a}kR_{g_{d}}, \) and \( \bar{e}_{d_{s}} = 4T_{a}kR_{d_{s}} \), are added [12]. The resultant correlation matrix, \( \mathbf{C}_{Z} \), is expressed as follows:

\[
\mathbf{C}_{Z} = \mathbf{Z} \cdot \mathbf{C}_{Yd}^{\text{admit}} \cdot \mathbf{Z}^\dagger + 4kT_{a}R
\]

where

\[
\mathbf{Z} = \begin{bmatrix}
1 & 0 \\
0 & 1
\end{bmatrix}
\]

and \( \mathbf{Z} = (\mathbf{Y})^{-1} \) is the intrinsic impedance matrix (see Fig. 1). Finally, \( \mathbf{C}_{Z} \) is transformed into the admittance configuration to obtain the total admittance noise correlation matrix \( \mathbf{C}_{Y}^{\text{TOT}} \).

The resulting expression is given by

\[
\mathbf{C}_{Y}^{\text{TOT}} = \mathbf{Y} \left( \mathbf{Z} \cdot \mathbf{C}_{Yd}^{\text{admit}} \cdot \mathbf{Z}^\dagger + 4kT_{a}R \right) \mathbf{Y}^\dagger
\]

where \( \mathbf{Y} \) is the device admittance matrix.

Once \( \mathbf{C}_{Y}^{\text{TOT}} \) has been determined, the equivalent output noise current spectral density \( \bar{I}_{o} \) referred to the FET gate-source (G-S) port, can be derived. It is assumed that the drain-source (D-D) port is connected to an arbitrary admittance, \( Y_{s} \). The analysis is as follows. The reverse-biased cold-FET is a noisy two-port that can be represented (see Fig. 2) as a noiseless two-port with two noise-current sources, \( i_{n1} \) and \( i_{n2} \), connected at the G-S port (2-2′) and D-S port (1-1′), respectively (admittance configuration). The thermal noise source, \( i_{n} \), associated with the \( Y_{s} \) admittance is also considered. From analysis of noisy two-ports in admittance representation [13], the following expression for \( I_{1} \) is obtained:

\[
I_{1} = \left( Y_{11} - \frac{Y_{12}Y_{21}}{Y_{22} + Y_{21}} \right) I_{n} - \frac{Y_{12}Y_{21} + Y_{12}i_{n1} + Y_{12}i_{n2}}{Y_{22} + Y_{21}} + i_{n1}
\]

where

\[
P = \frac{Y_{12}}{Y_{22} + Y_{21}}
\]

Then, assuming that \( i_{n} \) is not correlated with \( i_{n1} \) and \( i_{n2} \), the output noise current spectral density \( \bar{I}_{o} \) is given by

\[
\bar{I}_{o} = |P|^{2} \bar{I}_{1}^{2} + \left| \frac{Y_{12}Y_{21} + Y_{12}i_{n1} + Y_{12}i_{n2}}{Y_{22} + Y_{21}} \right|^{2} + |P|^{2} \bar{I}_{i_{n1}}^{2} + |P|^{2} \bar{I}_{i_{n2}}^{2} + |P|^{2} \bar{I}_{e_1}^{2} + |P|^{2} \bar{I}_{e_2}^{2}.
\]

The self and cross-power spectral densities of the noise sources \( i_{n1} \) and \( i_{n2} \) [12] can be arranged in matrix form \( \mathbf{C}_{Y}^{\text{TOT}} \), thus obtaining

\[
\bar{I}_{o} = |P|^{2} \bar{I}_{1}^{2} + [1 \quad P] \cdot \mathbf{C}_{Y}^{\text{TOT}} \cdot [1 \quad P]^\dagger.
\]

where

\[
\mathbf{C}_{Y}^{\text{TOT}} = \begin{bmatrix}
\bar{I}_{1}^{2} & \bar{I}_{12} \\
\bar{I}_{12} & \bar{I}_{i_{n1}}^{2} + \bar{I}_{i_{n2}}^{2}
\end{bmatrix}
\]

The total admittance noise-correlation matrix \( \mathbf{C}_{Y}^{\text{TOT}} \) was obtained in Eq. (8). Substituting (8) into (14), \( \bar{I}_{o} \) is written as the sum of a contribution due to the intrinsic noise sources, \( \bar{I}_{g_{s}} \) and \( \bar{I}_{g_{d}} \), and a contribution due to thermal noise \( \bar{I}_{e_1} \) (known from small-signal analysis):

\[
\bar{I}_{o} = \mathbf{H} \begin{bmatrix}
\bar{I}_{g_{s}} \\
\bar{I}_{g_{d}}
\end{bmatrix} + \bar{I}_{i_{n1}} + \bar{I}_{i_{n2}} + |P|^{2} \Re(Y_{s}).
\]

\[
\bar{I}_{o} = 4kT_{a}(U \cdot \mathbf{R} \cdot U^\dagger + (Q \cdot \mathbf{H}) \cdot \mathbf{Y}_{p} \cdot (Q \cdot \mathbf{H})^\dagger + |P|^{2} \Re(Y_{s})).
\]
From Eq. (15), the output current spectral density $i_{o}$ can be computed if $i_{gs}$ (or $i_{gd}$ if they are assumed to be the same) are known; however, to compute these terms the multiplier factor $M$ must be known [see Eq. (1)]. Since $M$ depends on the reverse-biased cold-FET physical characteristics under prebreakdown conditions, that is, drift and avalanche zone width, ionization coefficient, and saturation drift velocity (which typically are not known), the calculation of $M$ can be difficult. Alternatively, $i_{o}$ can be expressed as a function of the device noise temperature $T_{d}$ and its admittance $Y_{d}$, both measured at the gate-source port (plane 2-2 in Fig. 2):

$$\overline{i_{o}} = 4k \cdot T_{d} \cdot \text{Re}(Y_{d}).$$

(18)

Considering the assumption that $i_{gs} = i_{gd}$, substituting (18) into (15), and solving for $\overline{i_{gs}}$, the next expression is derived as follows:

$$\overline{i_{gs}} = (4k \cdot T_{d} \cdot \text{Re}(Y_{d}) - i_{o}) \cdot (H \cdot H)^{-1}.$$  

(19)

Finally, using (19) in (1), the multiplier factor $M^{2}$ is determined at each frequency:

$$M^{2} = \overline{i_{gs}} / 2qI_{gs}.$$  

(20)

To measure the reverse-biased cold-FET noise temperature $T_{d}$ and its gate-source admittance $Y_{d}$, an experimental on-wafer setup, and calibration and measurement procedures such as those described in [5], are used. To reduce the jitter in the computed factor $M^{2}$ (due to random measurement errors in $T_{d}$ and $Y_{d}$), a simple regression technique in log scale is applied to $M^{2}$ for a sufficient number of frequency points, in a similar way as that proposed in [5]. Thus, a smooth characteristic over the frequency is obtained for $M^{2}$, in agreement to theoretical predictions [9]. Then, $T_{d}$ is calculated again from Eqs. (1) and (15), estimated $T_{d}$ ($T_{d}^{est}$) is computed from Eq. (18), and the ENR estimated of the reverse-biased cold-FET is found by using

$$\text{ENR} = 10 \cdot \log \left( \frac{T_{d}^{est}}{T_{0}} - 1 \right).$$  

(21)

where $T_{0}$ (=$290^\circ$K) is the standard temperature.

3. EXPERIMENTAL RESULTS

The device characterized in this work is an on-wafer 0.5-μm gate-length, 2 × 50 μm gate-width DPD-SQW HEMT from the
Figure 6 Receiver’s noise parameters up to 40 GHz, measured with a coaxial noise-source (––) and with an on-wafer noise-source (reverse-biased cold-FET) (– –△– –)