

On Passive Bias Networks for Drain-Modulated Power Amplifiers

Eduard Bertran^{1*}, José Angel Garcia², Gabriel Montoro¹, Pere L. Gilibert¹ and Jordi Berenguer¹

¹ Dept. of Signal Theory and Communications, Technical University of Catalonia (UPC), C/Esteve Terradas, 7 - 08860 Castelldefels, Barcelona, Spain. Email: [bertran, montoro, plgilibert, berenguer]@tsc.upc.edu

² Dept. of Communications Eng., Univ. of Cantabria, Avda. Los Castros, Santander, Spain, joseangel.garcia@unican.es

Abstract- This paper revisits usual passive bias networks for microwave power amplifiers (PA), considering not only their effects on PA stability, but also its suitability to be used in drain modulated amplifiers. Some technical limitations and challenges regarding the design of PA in structures based on envelope tracking techniques, such as Polar Transmitters or Envelope Elimination and Restoration (EER) are presented.

Index Terms- Microwave amplifiers, Intermodulation distortion, Polar transmitters, Envelope tracking.

I. INTRODUCTION

Power amplifiers (PA) suitable for new communications systems have to cope with strong specifications in frequency selectivity (transmit power mask) and high linearity, shown both in band (EVM, Error Vector Magnitude) and out-of-band (ACPR, Adjacent Channel Power Ratio) parameters [1]. Moreover, the PA used in mobile terminals (responsible of the 70 – 80 % of the power consumption of the transmitters) has to be also very power efficient, in order to improve the battery lifetime, a critical aspect to produce terminals commercially competitive. When the modulation has constant (or quasi-constant) amplitude, the PA linearity-and power efficiency trade-off may be relaxed (i.e, biasing the PA at minimum operative back-off levels) or, even, efficient switched PAs may be used. However, in non-constant amplitude modulations, it has been widely recognized that a good solution to the trade-off is the use of linearizers, and a significant research effort is being made in this area.

Because communication standards are continuously advancing, new design challenges are consequently appearing: adaptive modulation formats, transmodulations, scalable bandwidths (i.e: 3G-LTE, Mobile WiMAX) as well as the need of multiband-multimode equipment, capable to simultaneously communicate with different standards and/or frequency bands (i.e., laptops using GSM-UMTS and WiFi). A common

characteristic of PAs for advanced communication systems is the necessary capability to cope with high PAPR (peak to average power ratio) as well as to operate at high bandwidths (and, in some applications, also scalable). These facts have focused the research on linearization structures to those capable of high bandwidth operation and without the need of delicate adjustments. Besides, the wider bandwidths have introduced the need to also consider memory effects in the PA linearizers designs [1]. Additionally, the high PAPR values makes difficult to fix an efficient biasing point, so it is preferable to move it according to the instantaneous amplitude of the signal to be amplified. This is the fundament of different kinds of Polar Transmitters (PT) [2],[3]. Current research in PT is mainly twofold: their combination with digital predistorters to compensate PA nonlinearities and/or to cope with wider bandwidths, and the research on adjustable power supplies (DC-DC or power saturated solutions), capable to follow fast envelopes. This limitation is the main impediment to extensively apply PT to new communications systems.

Traditionally, PA designers have considered the bias network as only seen from the transistor side, by fitting the network low pass response (i.e, allowing the pass of filtered supply voltages to the active device and blocking the RF energy from being wasted in the dc supply network and wires: chokes –beads-, capacitors, $\lambda/4$ open stubs, ...) [4]. Recently, some investigations have faced the effect of the bias points and networks on PA linearity (IMD) [5], [6]. In [7] it is presented the difficulty to remove the resulting nonlinearity as consequence of the variations in the DC supply impedance even by using the most sophisticated predistortion techniques. And memory effects have been reduced by allocating transmission zeros (series resonances) in the transfer function of the bias network, like in [8].

Keeping the abovementioned low-pass functionality, in the case of PT the bias networks

have also to permit the necessary drain voltage variations to follow the RF signal amplitudes, thus leading to some design compromises. An example is the use of capacitors, beneficial for DC voltage stabilization and RF blocking, but at the price of slowing the drain voltage variations because of their low-pass behavior. Other problem may be as consequence of the chokes because inductances limit the slope of current variations, so then becoming a potential cause of distortion when the transistor has to follow high PAPR values in a wide bandwidth.

In this paper, some issues related with the use of choke inductors in the bias networks for PT are investigated and experimentally assessed from both the amplifier stability and its capacity to linearly follow drain voltage variations. In order to set-up an experimental benchmark to make experiments, drain voltage variations have been limited to a reduced set of quantified values, stepped in a similar way as it is done in class-G power amplifiers used in line driving. Therefore, the conclusions will be only as consequence of the PA bias network, not depending on the particular profile of the modulated signal amplitudes.

II. STABILITY STUDIES

We have designed a WiMAX 3.5 GHz class-A medium power amplifier, with two different bias networks. The transistor used for the PA is a commercial GaAs HEMT, the ATF-54143 and the matching networks have been designed in the standard way, tuned with adequate rectangular stubs in microstripline. For both bias networks, the amplifiers under test have been feed by a power supply of the bipolar type (gate and drain).

Assuming ideal behavior of the bias network, the ADS simulated S parameters are shown in Fig. 1.

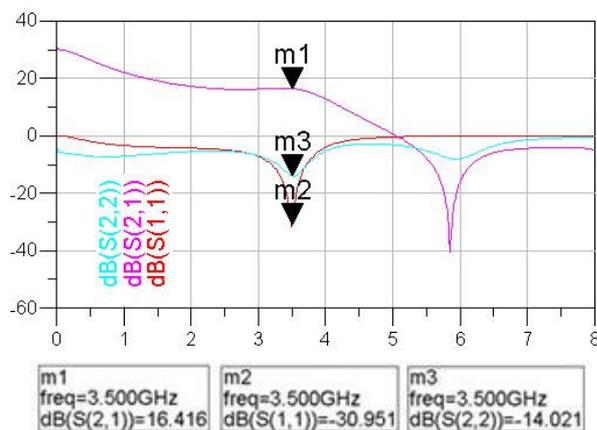


Fig. 1.- Power amplifier and simulated results.

Regarding the two different bias network, both are based a low-pass ladder network, with some blocking capacitors connected with stabilizing resistors. As usually, the first element of the ladder network is an inductor. Here a quarter wavelength line has been preferred for this functionality because its capability to act as 2nd harmonic trap: 50 Ω rectangular $\lambda/4$ open stubs have been used for this purpose in both the gate and the drain bias networks (Fig.2).The quarter wavelength and the blocking capacitors have been connected with stabilizing resistors in a ladder network.

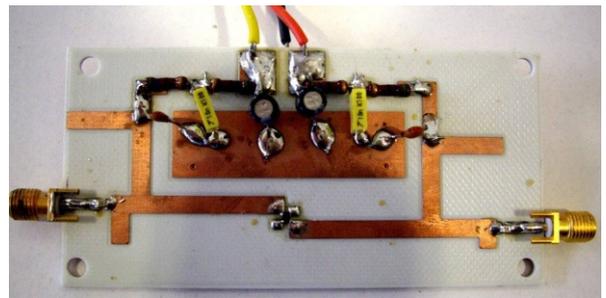


Fig. 2. Amplifier biased with stubs.

The second bias network (Fig. 3) is similar, but two chokes placed at $\lambda/2$ from both the transistor drain and gate, have been added to the previous $\lambda/4$ open stubs.

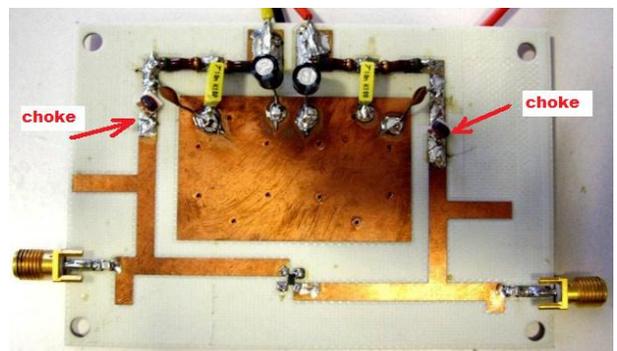


Fig. 3. Amplifier biased with stubs and chokes

The stability of both circuits has been studied from ADS simulations. In the case of the first bias network (no chokes), the “mu” factor from 100 MHz to 4 GHz is shown in Fig. 4. Notice that, in spite of having a value clearly higher than 1 at the band of interest (3.5 GHz), in the lower band (around 700 MHz), the “mu” factor announces instability risks.

Since in microstrip technology the RF blocking $\lambda/4$ stubs are not ideal because of the different propagation constants in the circuit board and in the air, the output stability circles (Fig. 4, bottom), are closer the center of the Smith chart at frequencies below 1 GHz. Obviously, this

instability risk may be reduced with larger stabilizing resistors in the matching network, but we don't consider it because the consequent loss in power efficiency.

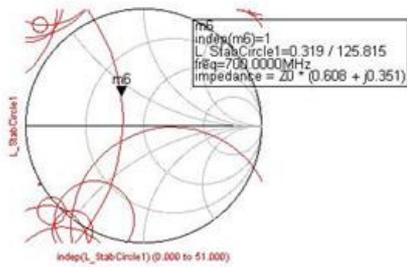
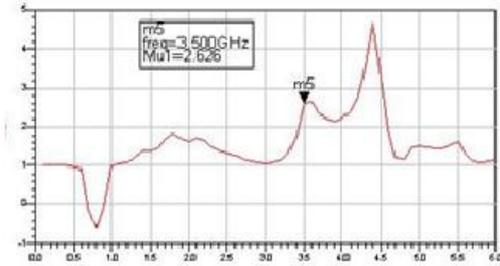


Fig. 4. Mu factor of the bias network without chokes (up), and stability circles (down).

With the second bias network (chokes), the “mu” factor (Fig. 5) is also fragile in the 700 MHz band, but its value is not as low as in the previous case. Now, in spite to be lower than 1, at least it is positive. In coherency both input and output stability circles have resulted more separated from the origin of the Smith chart, in comparison with Fig. 4. So, the use of stabilizing resistors is not so necessary.

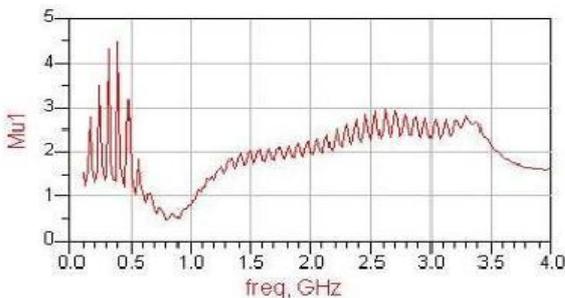


Fig. 5. Mu factor of the bias network with stubs and chokes.

III. MEASUREMENTS

In Fig. 6, the parameter S_{21} of the PA operating with the first biasing network is shown. Notice the strong resonance around 650 MHz, which has resulted significantly higher in practice than the value previewed in the simulation studies.

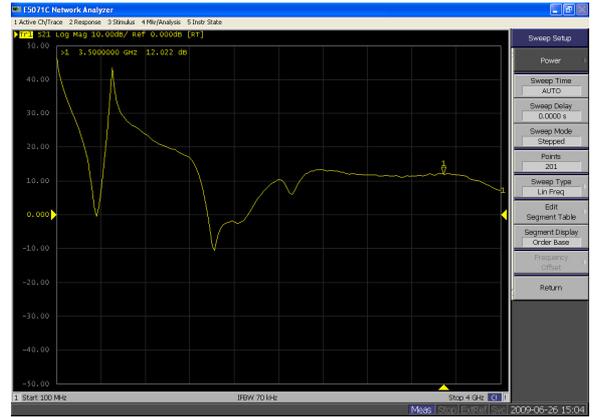


Fig. 6. Measured S_{21} with the first bias network

This difference is because of the use of microstripline technology in the printed circuit (non-ideal pads): two conjugated poles with small damping factor have appeared at 650 Hz, evidencing a feedback path from drain to gate through the blocking capacitors soldered at the root of the $\lambda/4$ stubs and the upper ground plate (Fig. 2). On the contrary, in the second bias network (Fig. 7) the chokes shrink the feedback signal level (lowering the open-loop gain), and the resonance is practically negligible without the need to reduce closed loop gain for enlarging stability.



Fig. 7. Measured S_{21} with the second bias network

Consequently, from the stability point of view, it is verified that the use of chokes additionally to $\lambda/4$ open stubs at the beginning of the ladder RC network is beneficial from both design restrictions (less critical instability circles) and practical effects (reduction of undesired feedback paths in printed circuits).

IV. DRAIN VOLTAGE MODULATION

In order to evaluate the effects of the choke inductor on the capability of the bias network to allow fast drain voltage variations in PT, a circuit based on the *bias switch array* proposed in [9] has

been made. The circuit we have constructed is based on an envelope detector, a signal level conditioner and an analog windows comparer, thus quantifying the envelope amplitude in three voltage ranges (symmetrical along the maximum and minimum possible envelope values). Each voltage range connect the drain of the power amplifier to a different power supply trough power MOS, with fly-back diodes protection.

Figure 8 show the IMD results when a single tone modulated signal is applied to the switched bias amplifier operating with the first biasing network (no chokes). The modulated signal is directly applied to the gate (with fixed bias), while the three quantified voltages obtained from the detected envelope are applied to the drain through the bias network.

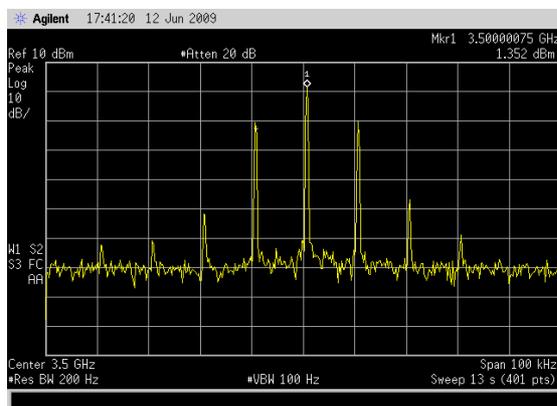


Fig. 8. IMD without chokes. Switched bias.

Figure 9 corresponds to the same measurement, with the same modulating signal (in order to keep the separation between tones for avoiding other causes of appearance of memory effects), when the chokes are placed in the bias network.

V. CONCLUSION

Chokes included in the ladder bias network are beneficial for PA stability. However, in this paper it has been proved that in switched bias, and likewise in drain modulated amplifiers as is the case of polar transmitters, their inclusion produces an increase of distortion. Measured in the conventional way, IMD is not necessarily enlarged, but additional spurious appear both in-band and out-of-band, being the first ones comparatively higher. This fact may directly shrink the resulting EVM values. Because the additional memory effects due to the bias network are not very dependent on the carrier spacing (distortion bandwidth) they become a new source of memory effects, as it was pointed in [7] and [8].

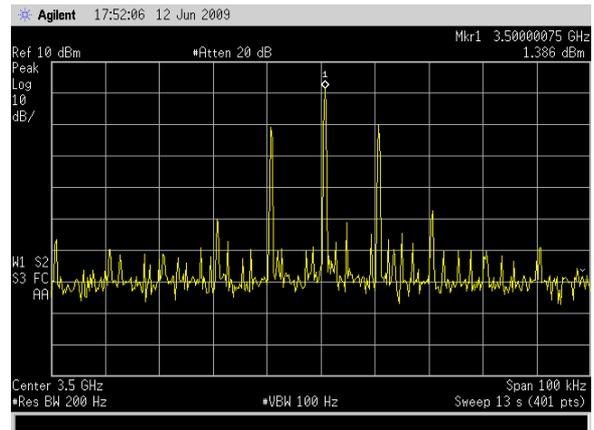


Fig. 9. IMD with chokes. Switched bias

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REFERENCES

- [1] Gilabert, P.L.; Cesari, A.; Montoro, G.; Bertran, E.; Dilhac, J.M., "Multi-Lookup Table FPGA Implementation of an Adaptive Digital Predistorter for Linearizing RF Power Amplifiers With Memory Effects", *IEEE trans. on MTT*, Vol 56, n 2, Feb. 2008
- [2] Groe, J. "Polar Transmitters for Wireless Communications". *IEEE Communications Magazine*, Vol. 45, n. 9, September 2007
- [3] Priyanto, B.E.; Sorensen, T.B.; Jensen, O.K.; Larsen, T.; Kolding, T.; Mogensen, P. "Impact of polar transmitter imperfections on UTRA LTE uplink performance", *Norchip*, Nov. 2007.
- [4] *RF Circuit Design: Theory and Applications*, R. Ludwig, P. Bretchko, G. Bogdanov, 2007, Prentice Hall.
- [5] J. Santiago, J. Portilla, T. Fernández, "Study of the influence of bias and matching networks on the distortion and memory of FET-based power amplifiers", *International Journal of RF and Microwave Computer-Aided Engineering*, vol. 18, n. 6, Nov. 2008.
- [6] P. M. Cabral, J. C. Pedro, N. B. Carvalho, "Bias Networks Impact on the Dynamic AM/AM Contours in Microwave Power Amplifiers," *International Workshop on Integrated Nonlinear Microwave and Millimeter-Wave Circuits*, January 2006
- [7] Khanifar, A.; Maslennikov, N.; Vassilakis, B. "Bias Circuit Topologies for Minimization of RF Amplifier Memory Effects". *33rd. European Microwave Conference*. Munich, October. 2003.
- [8] W.M. Fathelbab, Design of a new class of microwave bias networks with modal-matching properties, *IET Microwaves, Antennas & Propagation*, vol 2, June 2008.
- [9] Kyoungsoon Yang; Haddad, G.I.; East, J.R.;" High-efficiency class-A power amplifiers with a dual-bias-control scheme", *IEEE trans on MTT*, vol 47, n. 8, August 1999.