Hot Spot Detection in Integrated Circuits Laterally Accessing to the Substrate

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Abstract: Thermal management of nano estructures requires the use of temperature monitoring strategies. In this work, we expose a strategy based on sensing the heat-flux within the chip substrate with a probe-laser beam. As the beam passes through the die, it experiences a deflection directly proportional to the heat-flux found along its trajectory (Internal Infrared-laser deflection technique, IIR-LD) [1, 2]. As application example, we expose how hot spots can be detected in Integrated Circuits (ICs).

Hot Spot detection and localisation has been a common practice in failure analysis and system design debugging. Classical non-invasive and non-contacting approaches to localise hot-spots in ICs have been based on the measurement of the temperature [3, 5] or MOSFET hot-carriers' luminescence [6, 7] on the IC top surface (frontside techniques). However, all of them present a common limitation: the attenuation that temperature (partially) [3] and photon emission (totally) [8] experiences due to metal layers placed over the chip. This is a concern in nowadays and future nanometer CMOS technologies, which may reach up to thirteen levels of metal layers and metal fills are a must [8]. For this reason, backside probing was suggested (backside techniques) [3, 8]. This is possible by either opening a window on the die rear metallization (temperature case) [3], or reducing and polishing the substrate thickness to enhance the photon transmission (luminescence case) [8]. In both cases, a background specific preparation is required.

The experiment explained allows inspecting the chip through its lateral sides (lateral access), avoiding the metal and passivation layers placed over the die. The obtained results demonstrate the suitability of this technique to locate and characterise devices behaving as hot-spots in nowadays IC CMOS technologies. To show this approach, a specifically designed IC with MOSFET (Metal-Oxide-Semiconductor Field Effect Transistor) devices working as hot-spots has been used (see Fig. 1 (d)).
To demonstrate the technique's feasibility, a MOSFET device (see Fig. 1 (a)) is periodically activated by an unipolar power pulse train and its location is found by processing the amplitude corresponding to the first harmonic of the vertical ($V_{out,v}^1$) and horizontal ($V_{out,h}^1$) components of the laser beam deflection (see Figs. 1 (b) and (c)). This is presented as a function of the lateral coordinate at a given inspection depth, after performing the IC perimeter scanning. The location is determined when a maximum and null value (minimum) is obtained for the vertical and horizontal deflection signals, respectively (see Figs. 1 (b) and (c)).

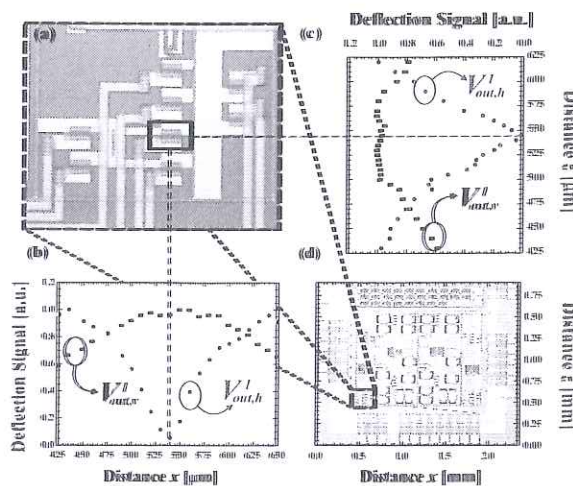

Fig 1. (a) Photograph of the region of the layout where a MOS transistor behaves as a hot spot. (b) Amplitude of the vertical and horizontal beam deflection components for n=1 as a function of the IC layout x coordinate. (c) Amplitude of the vertical and horizontal beam deflection components for n=1 as a function of the IC layout z as a function of the IC layout z coordinate. The maximum in the vertical component and the minimum in the horizontal component in both scan directions locate the dissipating MOS transistor. (d) IC top view photograph, partially illustrating the IC dimensions and the coordinate

system adopted in this work.

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