Frequency-Modulation Control of a DC/DC Current-Source Parallel-Resonant Converter

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***Abstract*—This paper proposes a frequency-modulation control scheme for a dc/dc current-source parallel-resonant converter with two possible configurations. The basic configuration comprises an external voltage loop, an internal current loop, and a frequency modulator: the voltage loop is responsible for regulating the output voltage, the current loop makes the system controllable and limits the input current, and the modulator provides robustness against variations in resonant component values. The enhanced configuration introduces the output inductor current as a feed-forward term and clearly improves the transient response to fast load changes. The theoretical design of these control schemes is performed systematically by first deriving their small-signal models and second using Bode diagram analysis. The actual performance of the proposed control schemes is experimentally validated by testing on a laboratory prototype.**

***Index Terms*—Control design, control systems, dc–dc power converters, frequency modulation, resonant converters.**

I. Introduction

SINCE the emergence of the resonant technology, major research efforts have been conducted to apply the enhanced features of resonant converters to practical applications [1]–[8]. Induction heating [1], electric vehicle [2], lighting system [3], robotic industry [4], [5], and contactless energy-transfer system [6]–[8] are just a short list of examples. DC–DC conversion category is another industry example of great importance for these converters. Battery charging, electronic air purifiers, and switching power supplies are among these applications, ranging from low to high power [9]–[15]. A great interest has been taken in these converters due to their generated high frequency sinusoidal waveforms, reducing the electromagnetic interference and switching losses [16]. The control strategy has been one of the challenging research keys in this field. For voltage-source series-resonant converters, many control strategies have been analyzed and investigated [17]–[23], turning this into a mature technology nowadays. However, compared to the series-resonant topologies, parallel-resonant converters absorb a continuous smooth current from the input source, offering low current stress to switches [24]. Likewise, the reactive power circulates inside the parallel resonant tank and only the active power is supplied through the switches. This feature provides the capability of generating high current and voltage levels by using low VA-rated switches, reducing conduction losses. In addition, these converters provide more facilities such as short-circuited protection and paralleling capabilities. For the reasons outlined above, the research on the current-source parallel-resonant converters (CSPRC) has recently attracted more interest [25]–[31]. In particular, in [25], a current source topology has been proposed to supply a multireceiver inductive contactless energy transfer system. In this topology, a buck converter has been utilized to obtain an input current source with constant amplitude, supplying the resonant inverter. In [26], a simple modulation technique has been proposed for this type of converter and then applied to an induction heating system [27]. This method is then further developed in [28]. In [29], the modulation technique has been applied to an inductive contactless energy transfer system. A delta–sigma modulator is also applied to a class-D CSPRC in [30]. In all these works, the current-source converters operate in open loop and thus they exhibit a high sensitivity to external disturbances and parameter variations. In [31], a closed-loop control scheme with amplitude modulation has been presented for a dc/dc CSPRC. A robust behavior against load changes was demonstrated in this study by simulation results; however, some drawbacks inherent to the amplitude modulation limit its practical use.

The aim of this paper is to introduce a control scheme for the dc/dc class-D CSPRC intended for switching power supplies. The control scheme has two possible configurations. The basic configuration is responsible for both regulating the output voltage and providing zero voltage switching (ZVS) conditions. A cascaded control scheme is proposed to this end, including an external voltage loop and an internal current loop. ZVS conditions are guaranteed by driving the switches with a robust frequency modulation technique. In addition, an enhanced control configuration is presented in this paper in order to further improve the load transient response of the basic configuration. The design of the control schemes is based on two steps. First,

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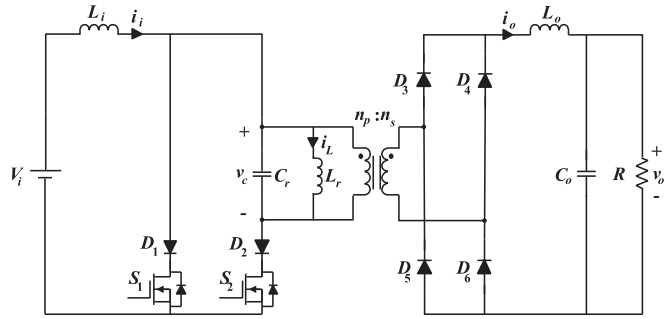

Fig. 1. Power circuit of the class-D CSPRC.

a dynamic model of the open-loop CSPRC is obtained. Afterward, the small-signal characteristics of the obtained averaged model are derived. Second, the dynamic model for the closed-loop system is formulated and a systematic procedure to design the control gains is presented.

The theoretical contributions of this paper are: the large-signal model of the CSPRC operating with frequency modulation; 2) its small-signal model; 3) the control scheme, including the basic and enhanced control-loop configurations and the frequency modulator (FM); and 4) the systematic design procedure for deriving the control gains. As far as authors know, there are no previous studies exploring these four topics together or separately for the considered resonant topology.

This paper is structured as follows. Section II derives the large-signal model of the class-D CSPRC and its averaged small-signal model. Section III introduces the basic and enhanced control configurations, including the FM. Section IV presents the design process of the proposed control scheme intended for dc/dc applications. Section V verifies the theoretical contributions by selected experimental results in a laboratory prototype. Finally, Section VI gives the conclusions.

II. Dynamic Modeling of the Class-D CSPRC

Fig. 1 shows the power circuit of the dc/dc class-D CSPRC. The class-D resonant inverter includes an input inductor (L_i), a second-order parallel-resonant tank (L_r and C_r) and a high-frequency transformer with winding turns ratio $n_p : n_s$. The resonant tank is loaded through a full-bridge diode rectifier and a second-order low-pass filter (L_o and C_o) to get a dc output voltage. The operation principle of this converter using frequency modulation was presented in detail in [24], and thus it is not repeated here.

The first contribution of this paper is the development of an adequate dynamic description of the class-D CSPRC converter for dc switching power supply applications. This model is essential for the control design process. Below is a step-by-step derivation of the dynamic model.

A. State-Space Model

The assumptions to derive the model are: 1) the components are ideal and 2) the circuit is driven by frequency modulation. In this case, the control input is the angular switching frequency ω_s. This variable will be provided by the control system in order to reach the control objectives (i.e., output voltage regulation and operation under ZVS conditions). Under these assumptions and taking into account the equivalent circuits of the converter presented in [24], the differential state-space equations can be expressed as follows:

$$\frac{di_i}{dt} = \frac{1}{L_i}\left[V_i - \left(\frac{1+\text{sgn}\,(\sin\omega_s t)}{2}\right) v_c\right] \tag{1}$$

$$\frac{dv_c}{dt} = \frac{1}{C_r}\left[\left(\frac{1+\text{sgn}\,(\sin\omega_s t)}{2}\right) i_i - i_L - \frac{n_s}{n_p}\,\text{sgn}(v_c)\, i_o\right] \tag{2}$$

$$\frac{di_L}{dt} = \frac{1}{L_r} v_c \tag{3}$$

$$\frac{di_o}{dt} = \frac{1}{L_o}\left[\frac{n_s}{n_p}\,|v_c| - v_o\right] \tag{4}$$

$$\frac{dv_o}{dt} = \frac{1}{C_o}\left[i_o - \frac{v_o}{R}\right] \tag{5}$$

where i_i stands for the input current variable, v_c and i_L are the resonant state variables, and v_o and i_o are the output filter state variables. According to [32], the state-space variables can be divided in two subgroups: fast and slow variables. The resonant state variables are fast variables and evolve the following sinusoidal waveforms. Input current and output voltage and current are slow variables. They evolve slowly compared to the dynamics of resonant waveforms.

B. Averaged Modeling of the Resonant State Variables

The averaged method presented in [32] is used here to obtain a proper dynamic model. In this method, the resonant state variables are approximated as sinusoidal waveforms including slow time-varying amplitudes and phases, defined as

$$v_c = V_c \sin(\omega_s t - \alpha) \tag{6}$$

$$i_L = I_L \sin(\omega_s t - \beta) \tag{7}$$

where V_c and I_L are the peak values of the resonant state variables, and α and β are the initial phases. These variables are then inserted into (2) and (3). By applying harmonic linearization and harmonic balance to the resulting model, the following equation is derived:

$$\frac{d\bar{v}_c}{dt} = \frac{1}{C_{\text{eq}}}\left[\frac{m}{2}\,\bar{i}_i - \frac{n_s}{n_p}\,\bar{i}_o\right] \tag{8}$$

where the symbol – denotes averaged value over a half-switching cycle, and the equivalent capacitor C_{eq} and the new variable m can be expressed as

$$C_{\text{eq}} = \pi^2 C_r/8 \tag{9}$$

$$m = \sqrt{1 - \left[\frac{\pi^2 Q}{4R}\,\frac{\bar{v}_c}{\bar{i}_i}\left(\frac{\omega_s}{\omega_o} - \frac{\omega_o}{\omega_s}\right)\right]^2}. \tag{10}$$

Note that m is a variable that contains information about the system state in an averaged sense (through the variables $\bar{v}_c$ and $\bar{i}_i$) and the control action ω_s. It is used here simply

to compact the final expressions of the models. In (10), the variables Q and ω_o represent the quality factor and angular resonant frequency of the resonant tank. In addition, Z_o is the characteristic impedance. These variables are defined as

$$Q = R/Z_o \tag{11}$$

$$\omega_o = 1/\sqrt{L_r\, C_r} \tag{12}$$

$$Z_o = \sqrt{L_r/C_r}. \tag{13}$$

Further details on model derivation can be found in [33]–[35], where the averaged models of other resonant topologies have been derived. Note that, in this case, the resonant tank is described in an averaged sense because only one differential equation (8) models the dynamics of the averaged resonant capacitor voltage. This equation contains all the necessary information to reproduce the transient and steady-state behavior of the resonant tank in an averaged sense. Also, note that this equation is nonlinear.

C. Averaged Modeling of Slow Variables

The averaged dynamics of the slow variables, including the input and output state variables, are derived by using the time-varying averaging over a half-switching cycle, resulting in

$$\frac{d\bar{i}_i}{dt} = \frac{1}{L_i}\cdot\left[V_i - \frac{m}{2}\,\bar{v}_c\right] \tag{14}$$

$$\frac{d\bar{i}_o}{dt} = \frac{1}{L_o}\left[\frac{n_s}{n_p}\bar{v}_c - \bar{v}_o\right] \tag{15}$$

$$\frac{d\bar{v}_o}{dt} = \frac{1}{C_o}\cdot\left[\bar{i}_o - \frac{\bar{v}_o}{R}\right]. \tag{16}$$

Therefore, the complete averaged large-signal model of the class-D CSPRC is expressed by (8) and (14)–(16).

As far as authors know, the large signal model for the frequency-modulated CSPRC has not been previously studied. Hence, this model constitutes the first contribution of this paper. The accuracy of this model is validated in Section II-E by selected simulation results.

D. Equilibrium Point

In steady-state conditions, all the averaged variables reach their equilibrium point. By considering $d\bar{i}_i/dt = 0$, $d\bar{v}_c/dt = 0$, $d\bar{i}_o/dt = 0$, and $d\bar{v}_o/dt = 0$, the equilibrium point of the model (8) and (14)–(16) can be expressed as

$$I_i = \frac{V_0^2}{R\,V_i} \tag{17}$$

$$V_c = \frac{2V_i}{M} \tag{18}$$

$$I_o = \frac{V_o}{R} \tag{19}$$

$$V_o = \frac{n_s}{n_p}\frac{2V_i}{M} \tag{20}$$

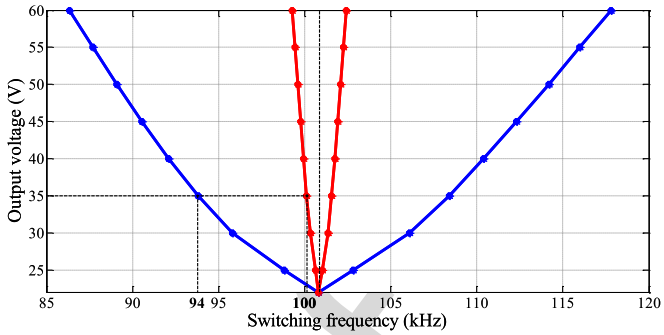

Fig. 2. Output voltage as a function of the switching frequency (FL in blue and 10% of FL in red).

TABLE I
VALUES OF THE POWER COMPONENTS

Symbol	Quantity	Value
V_i	Input voltage	12 V
L_i	Input filter inductor	300 μH
C_r	Resonant capacitor	470 nF
L_r	Resonant inductor	5.3 μH
$n_p : n_s$	Transformer turns ratio	1:1
L_o	Output filter inductor	100 μH
C_o	Output filter capacitor	470 μF
V_o	Output voltage	35 V
R	Full-load resistor	20 Ω

where M is the steady-state value of m (i.e., the equilibrium point of m), which can be written as

$$\frac{1}{M} = \sqrt{1 + \left[\frac{\pi^2}{8}\,Q\left(\frac{n_s}{n_p}\right)^2\left(\frac{\omega_s}{\omega_o} - \frac{\omega_o}{\omega_s}\right)\right]^2}. \tag{21}$$

Note that the equilibrium point depends on the control input ω_s, the resonant circuit parameters, the input voltage, and the load.

The output voltage in steady state can be easily determined from (20) and (21). Fig. 2 depicts this voltage as a function of the switching frequency for two load conditions: full load (FL) in blue and 10% of FL in red. The nominal values of the power components listed in Table I are used to draw the figure. Note that the output voltage can be maintained constant in steady state by adjusting conveniently the switching frequency. In fact, Fig. 2 also shows the theoretical values of the switching frequency that provides the nominal output voltage for the two considered load conditions.

E. Validation of the Averaged Large-Signal Model

The validity of the derived large-signal model expressed in (8) and (14)–(16) is evaluated by comparing selected simulation results with those obtained by the state-space model expressed in (1)–(5). Both models are implemented in MATLAB–Simulink, and the obtained results are shown in Fig. 3. Two different switching frequencies are considered to validate the averaged model in different operating points. During the first interval, the switching frequency is fixed at 91 kHz. At $t = 10$ ms, the

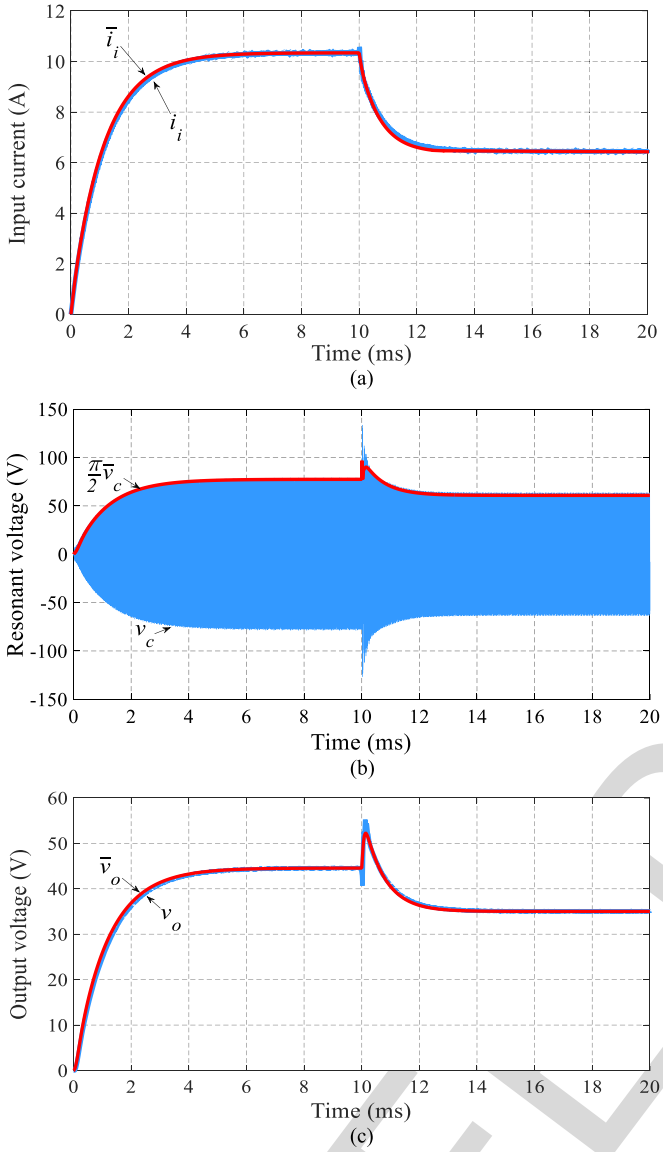

Fig. 3. Comparison of waveforms generated by the state-space model and the averaged large-signal model for two different switching frequencies ($0 < t < 10$ ms: 91 kHz, 10 ms $< t < 20$ ms: 94 kHz) and FL condition: (a) input current, (b) resonant capacitor voltage, and (c) output voltage.

switching frequency is changed to 94 kHz. This frequency is maintained to the end of the test. The results show good agreement between the models, although some small differences appear when the switching frequency is abruptly changed at $t = 10$ ms. These mismatches are clearly caused by the assumptions made in the large-signal model derivation. However, for control design purposes, the observed high-frequency transients are not important due to the limited control bandwidth (BW).

F. Small-Signal Model

The small-signal model of the converter is derived by following the conventional approach based on perturbing and linearizing the large-signal model [36]. The systematic procedure is presented below. First, the state variables are decomposed in dc (I_i, V_c, I_o, V_o and M, all defined in [17]–[20]) and ac ($\hat{i}_i$, $\hat{v}_c$, $\hat{i}_o$, $\hat{v}_o$, and $\hat{m}$) terms, given as follows:

$$\bar{i}_i = I_i + \hat{i}_i \tag{22}$$

$$\bar{v}_c = V_c + \hat{v}_c \tag{23}$$

$$\bar{i}_o = I_o + \hat{i}_o \tag{24}$$

$$\bar{v}_o = V_o + \hat{v}_o \tag{25}$$

$$m = M + \hat{m}. \tag{26}$$

Second, the amplitudes of the ac terms are considered small in comparison to the dc quantities (obtained equilibrium values), i.e.,

$$\hat{i}_i \ll I_i \tag{27}$$

$$\hat{v}_c \ll V_c \tag{28}$$

$$\hat{i}_o \ll I_o \tag{29}$$

$$\hat{v}_o \ll V_o \tag{30}$$

$$\hat{m} \ll M. \tag{31}$$

Third, by substituting (22)–(26) in (8) and (14)–(16), and taking into account that the products of two ac terms are negligible, the small-signal model is derived. It can be written in matrix form as follows:

$$\begin{bmatrix} sL_i & M & 0 & 0 \\ -M & sC_{\text{eq}} & n_s/n_p & 0 \\ 0 & -n_s/n_p & sL_o & 1 \\ 0 & 0 & -1 & sC_o + (1/R) \end{bmatrix} \begin{bmatrix} \hat{i}_i(s) \\ \hat{v}_c(s) \\ \hat{i}_o(s) \\ \hat{v}_o(s) \end{bmatrix} = \begin{bmatrix} -V_c \\ I_i \\ 0 \\ 0 \end{bmatrix} \cdot \hat{m}(s) \tag{32}$$

where s is the Laplace operator. Note that all the transfer functions that characterize the behavior of the converter in small signal can be derived from (32).

The obtained small-signal model constitutes the second contribution of this paper. This model is then utilized for control design as explained in Section IV.

III. Proposed Control Scheme

This section introduces a control scheme for the parallel-resonant converter with two possible configurations for the external voltage loop. The internal current loop and the FM are also presented in detail.

A. Voltage and Current Control Loops

Fig. 4 shows the diagram of the proposed control scheme. It is based on two control loops and an FM. The internal control loop makes the system controllable and limits the input current. To this end, it processes the input current error using a

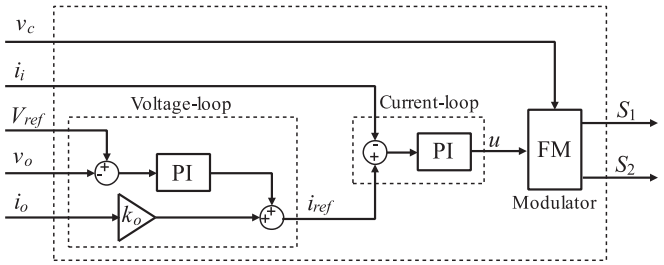

Fig. 4. Diagram of the two proposed control schemes. Basic configuration (i_o is not measured in this case and $k_o = 0$) and enhanced configuration (i_o is measured in this case and $k_o = V_{\rm ref}/V_i$).

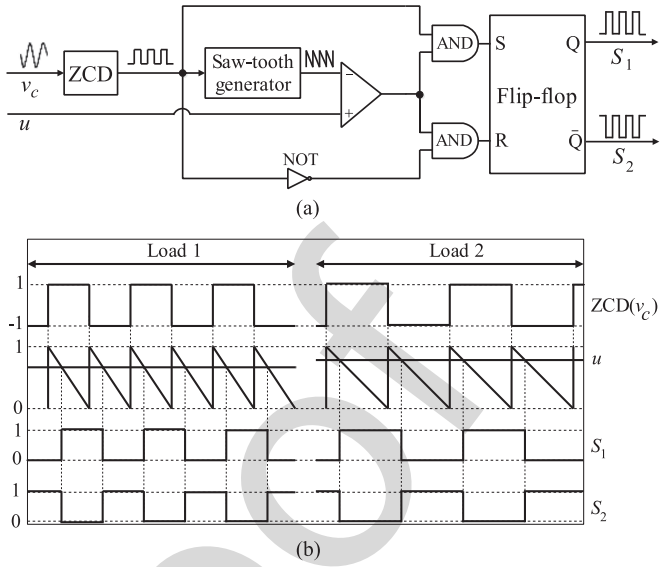

Fig. 5. Proposed FM including a variable slope, fixed amplitude saw-tooth generator: (a) diagram and (b) main waveforms for two different load conditions.

proportional-integral (PI) regulator and provides the signal u to the input of the modulator.

The external voltage loop is responsible to regulate the output voltage. It has two control terms: a feedback term that tries to eliminate the output voltage error using a PI regulator and a feed-forward term of the output current. The feedback term ensures that the output voltage matches the reference voltage in steady state, thus compensating the effects of unmodeled elements such as parasitic resistors and transformer leakage inductances. In the case of load-step changes, the feed-forward term helps the modulator to rapidly find an appropriate switching frequency to ensure a fixed-output voltage, yielding in a fast transient response.

The proposed controller is called here basic configuration when $k_o = 0$ and enhanced configuration when $k_o = I_i/I_o$. In the enhanced controller, the steady-state currents in the feed-forward gain k_o rely on the load condition. However, from (18) and (20) and assuming $V_o = V_{\rm ref}$, the feed-forward gain is independent of the load condition and can be written as

$$k_o = \frac{V_{\rm ref}}{V_i}. \tag{33}$$

The enhanced controller is introduced in order to improve the transient response, i.e, to get a negligible output voltage deviation and lower settling time. This is considered as the benefit of this control configuration. However, an additional measurement i_o is required in this case, slightly increasing the cost of the system.

B. Frequency Modulator

This section proposes an FM for the CSPRC. The modulator is derived from the phase modulator presented in [37] for voltage-source resonant converters. The differences between both modulators are also highlighted below.

Fig. 5(a) shows the proposed FM. It is based on the generation of a saw-tooth waveform synchronized by the zero crossing detection of the resonant capacitor voltage. This waveform is then compared with the output signal of the controller u in order to generate the gate signals (S_1 and S_2) by using an RS flip-flop. Fig. 5(b) shows the main waveforms of the modulator. Note that the switching period depends on the load conditions, as predicted by (21). It is worth mentioning that the ramp amplitude is always one in this modulator in order to modify the switching period as a function of the load condition. The saw-tooth generator produces this distinctive feature by means of a closed-loop control using a PI regulator; see details in [37]. The most promising feature of both modulators is the high robustness to resonant parameter variations. This feature is attributed to the sensing of the resonant tank state, through the measure of a resonant state variable. Thus, changes on resonant components due to temperature, tolerance, age, etc., are perfectly absorbed by the modulator. The main differences between the two modulators are as follows.

1) The resonant capacitor voltage instead of the inductor current is used to provide ZVS conditions.
2) The slope of the ramp signal is reversed to operate below resonance (the voltage-source resonant converter operates above resonance).
3) Only one input signal u is required to regulate the output voltage (the phase modulator needs two signals).

The proposed control scheme is the third contribution of this paper. The novelties of this configuration are: first, the feed-forward term included in the conventional two loop control in order to accelerate the transient response during load step changes; and second, the adaptive modulator used to synchronize the control action with the zero crossing of the resonant capacitor voltage, thus providing ZVS condition. In addition, the modulator provides a robust operation against internal and external disturbances (such as variations in resonant tank parameters and input voltage, respectively).

IV. Control Design

This section presents the design procedure to obtain the gains of the two PI controllers used in the proposed control scheme. A numerical example is also included to illustrate the procedure in detail. This design procedure constitutes the fourth contribution

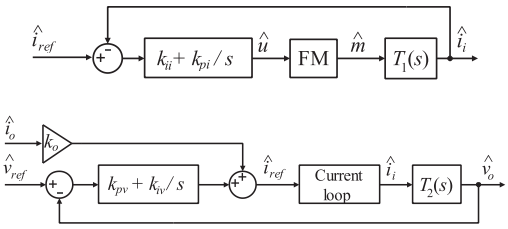

Fig. 6. Small-signal diagram of the (a) internal control loop and (b) external control loop.

of this paper. A numerical example is also included to illustrate the procedure in detail.

A. Design Procedure

The control design proceeds as follows.

1) The closed-loop transfer functions of the system are first obtained by using the derived small-signal model.
2) The frequency-domain specifications of the closed-loop system are fixed in terms of desired control BW and phase margin (PM).
3) The gain values of the PI controllers satisfying the specifications are selected.

To this end, Bode diagrams of different set of gain values are examined until the specifications are met.

B. Closed-Loop Small-Signal Models

Fig. 6 shows the small-signal diagram of the internal and external control loops. Note that the two PI controllers are included in the figure. The other transfer functions involved in the diagram are derived below.

The control to input-current $T_1(s)$ and input-current to output-voltage $T_2(s)$ transfer functions are obtained from the small-signal model expressed in (24). These transfer functions are

$$T_1(s) = \frac{\hat{i}_i(s)}{\hat{m}(s)} = \frac{A_1 s^3 + A_2 s^2 + A_3 s + A_4}{B_1 s^4 + B_2 s^3 + B_3 s^2 + B_4 s + B_5} \quad (34)$$

$$T_2(s) = \frac{\hat{v}_o(s)}{\hat{i}_i(s)} = \frac{C_1 s + C_2}{B_1 s^4 + B_2 s^3 + B_3 s^2 + B_4 s + B_5}. \quad (35)$$

The coefficients of these transfer functions can be found in the Appendix.

The transfer function of the proposed modulator is deduced according to the following points and assumptions.

1) It is well known that the small-signal model of a modulator involving a ramp signal coincides with the inverse of the amplitude of this signal (i.e., $1/V_{\text{ramp}}$) [36].
2) In the proposed modulator, a closed-loop control is used in the saw-tooth generator to fix the amplitude of the ramp signal to one ($V_{\text{ramp}} = 1$).
3) This control loop is fast enough compared to the BW of the internal and external control loops.

Thus, the transfer function of the modulator can be expressed as

$$\frac{\hat{m}}{\hat{u}} = \frac{1}{V_{\text{ramp}}} = 1. \quad (36)$$

TABLE II
FREQUENCY-DOMAIN SPECIFICATIONS

Control loops	BW (kHz)	PM (°)
Current loop	7.467	60
Voltage loop	0.593	60

TABLE III
VALUES OF THE CONTROL GAINS AND PARAMETERS

Symbol	Quantity	Value
k_{pi}	Current-loop proportional gain	0.4 A^{-1}
k_{ii}	Current-loop integral gain	30 Hz/A
k_{pv}	Voltage-loop proportional gain	0.01 Ω^{-1}
k_{iv}	Voltage-loop integral gain	120 Hz/Ω
k_o	Feed-forward gain (basic control)	0
k_o	Feed-forward gain (enhanced control)	2.9
V_{ref}	Reference output voltage	35 V

The design of the PI controllers is based on making the dynamic characteristics meet the control design specifications. Table II lists these specifications for the internal and external control loops. In the internal current loop, the control BW is 1.1 decades below the minimum switching frequency to get a fast current transient response. In the external voltage loop, the control BW is 1.1 decades below the control BW specification of the current loop in order to avoid undesired interactions between these control loops. The PMs are high enough to prevent the converter from going to the instability region.

The dynamic characteristics of the CSPRC can be extracted from the current and voltage loop gains. From Fig. 6, these transfer functions can be written as

$$T_i(s) = \left[k_{pi} + \frac{k_{ii}}{s}\right] T_1(s) \quad (37)$$

$$T_v(s) = \left[k_{pv} + \frac{k_{iv}}{s} - \frac{k_o}{R}\right] T_2(s). \quad (38)$$

Note that the loop gains depend directly on the gains of the two PI controllers, as usual. In the voltage loop gain, a perfect tracking of the reference current is assumed, i.e., $\hat{i}_i(s)/\hat{i}_{\text{ref}}(s) = 1$. This is actually a good approximation due to the reduced control BW of the voltage loop. In addition, the feed-forward term k_o appears in the voltage loop gain, so that the dynamic characteristics will be analyzed for: the current loop, the basic voltage loop ($k_o = 0$), and the enhanced voltage loop ($k_o = V_{\text{ref}}/V_i$). Hence, the impact of k_o on the transient response will be also analyzed considering the closed-loop transfer function shown in (38), derived from the small-signal model.

C. Design of the Internal and External Control Loops

The values of the PI gains are obtained according to the design specifications. Several Bode diagrams are represented with different PI gains until the specifications are met. Once this process is finished, the final values of the PI gains are captured and listed in Table III. The values of the feed-forward

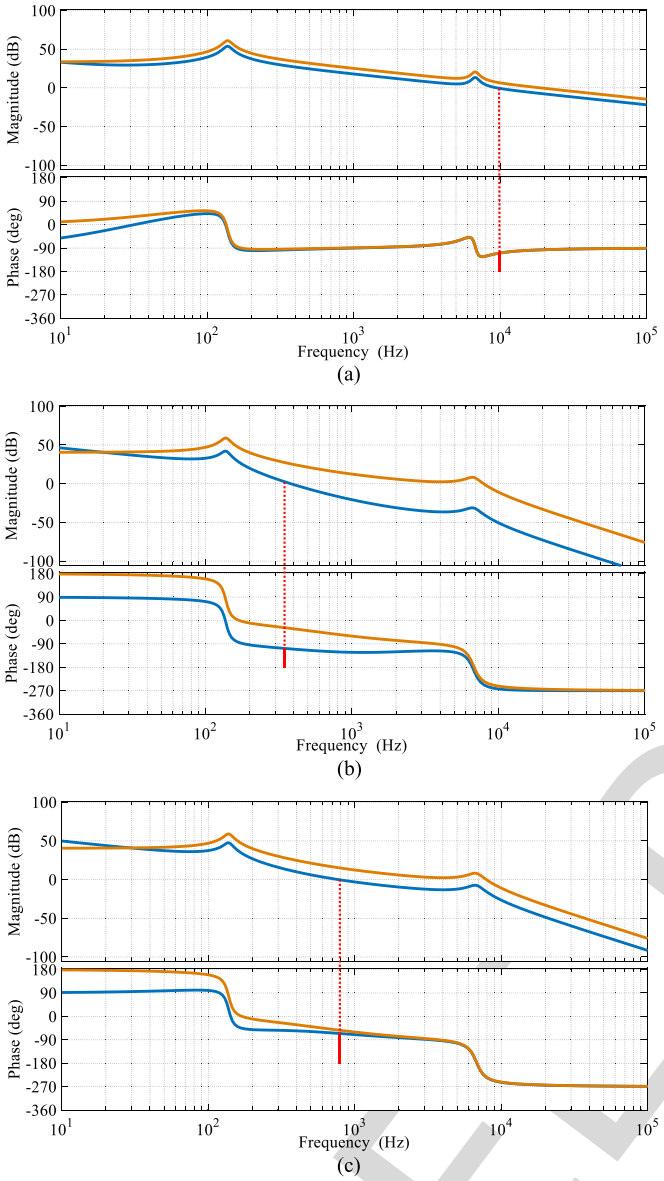

Fig. 7. Bode diagrams of (a) current loop gain, (b) voltage loop gain for the basic control ($k_o = 0$), and (c) voltage loop gain for the enhanced control ($k_o = V_{\rm ref}/V_i$) for FL condition (blue: compensated and orange: uncompensated).

gains for the basic and the enhanced control configurations are also included in the table. Fig. 7 shows the Bode diagram of the loop gains for both compensated and uncompensated system at FL condition. Note that the compensated system reduces the control BW to reach the design specifications, as depicted in Fig. 7.

For the current loop, the control BW is 9.43 kHz and the PM is 67.1°, meeting satisfactorily the design specifications. In the basic voltage loop, although the PM is good enough (70.4°), the control BW (0.35 kHz) is lower than the specification. Thanks to the feed-forward term, the enhanced voltage loop shows superior performance by increasing both the control BW (0.81 kHz) and the PM (116.4°). The design specifications are clearly meet by the enhanced control configuration.

TABLE IV
DYNAMIC CHARACTERISTICS FOR DIFFERENT LOAD CONDITIONS

Control scheme	Load condition	Current loop		Voltage loop	
		BW (kHz)	PM (°)	BW (kHz)	PM (°)
Basic	FL	9.43	67.1	0.35	70.4
($k_o = 0$)	10% of FL	8.52	85.2	0.23	98.2
Enhanced	FL	9.43	67.1	0.81	116.4
($k_o = V_{\rm ref}/V_i$)	10% of FL	8.52	85.2	0.67	153.3

TABLE V
PROTOTYPE COMPONENTS

Component	Model
Diodes	20ETF08S
MOSFETs	IRFR4620
MOSFET driver	MCP14E10
Resonant capacitor	MKT type
Op-amps	MCP6022

Table IV shows the dynamic characteristics for different load conditions. Note that the control BW improves as the load increases for both control loops. Conversely, the PM deteriorates as the load increases. Anyway, the design specifications are meet for the current loop and the enhanced voltage loop. In addition, the enhanced voltage loop improves the dynamic characteristics of the basic voltage loop for all load conditions.

V. EXPERIMENTAL RESULTS

This section validates the proposed control scheme with selected experimental results from a laboratory prototype.

A. Laboratory Prototype

A 60-W laboratory prototype was built including a dc–dc class-D CSPRC with a SPIC33FJ16GS504-I/PT microcontroller as digital control platform. The input and output currents were sensed with current transducers (LTP-15NP). Simple analog circuits including differential amplifiers are used to sense the resonant capacitor and output voltages. Other prototype components are listed in Table V. Fig. 8 shows the top and bottom views of the laboratory prototype.

B. Evaluation of Static Characteristics

In this section, the steady-state operation of the CSPRC is evaluated.

Fig. 9 shows the steady-state voltage across the right leg of the class-D inverter shown in Fig. 1 (including the voltages in MOSFET S2 and blocking diode D2) and its associated current for both FL and 10% of FL. Note that the waveform of the switch voltage is similar in both load conditions. The only notable difference is a change in the switching frequency. However, in the switch current waveform, the change in both switching frequency and in amplitude is observed. These features were theoretically predicted by (18)–(21), as discussed in Section V-C.

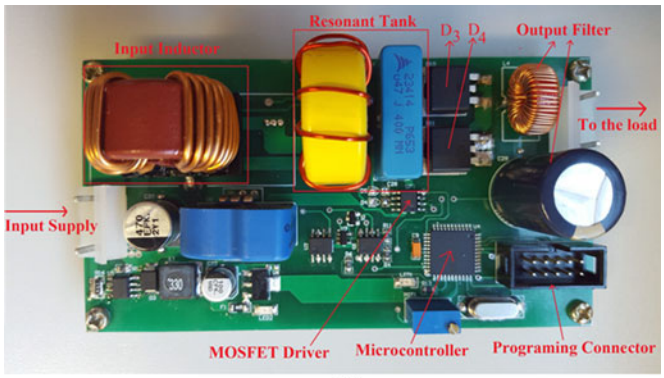

Fig. 8. Experimental dc–dc CSPRC prototype: (a) top view and (b) bottom view.

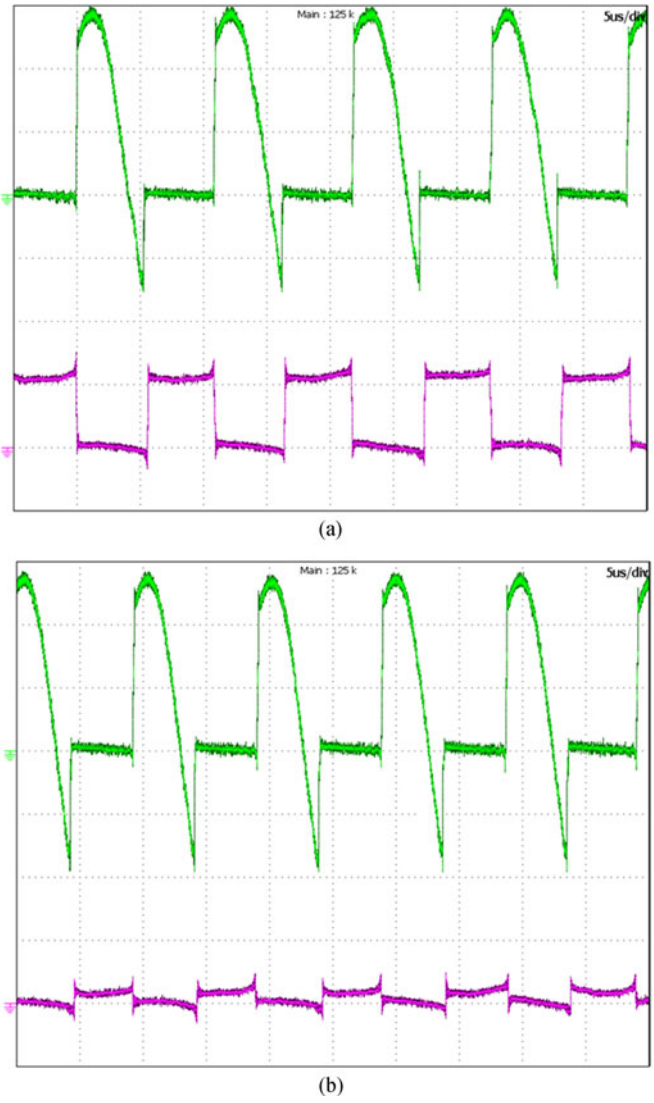

Fig. 9. Steady-state switch voltage (green, 20 V/div, 5 μs/div) and current (pink, 5 A/div) for: (a) FL and (b) 10% of FL.

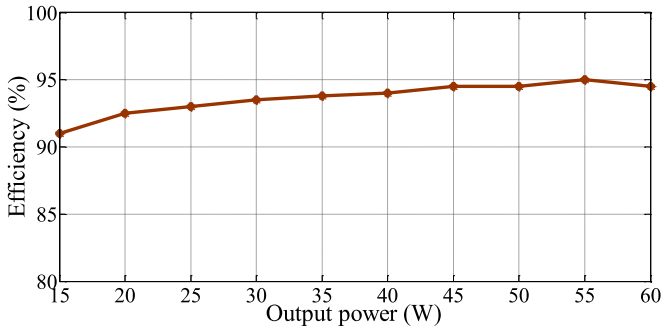

Fig. 10. System efficiency as a function of output power.

Fig. 9 also reveals the ZVS operation of the CSPRC. When the switch is OFF (interval with zero switch current), the switch voltage tracks the resonant capacitor voltage by changing sinusoidally from positive to negative values. In the interval with negative values, the diode D2 is naturally in OFF state and then MOSFET S2 can be driven to ON state. In this case, although S2 is ON, no current flows through the switch due to the blocking diode D2. Thus, the MOSFET S2 is in ON state with zero voltage across before switch current increases during the switch transition from OFF to ON. This mechanism is known as ZVS operation and is characterized by negligible switching losses.

Fig. 10 shows the system efficiency as a function of the output power. The highest efficiency (95%) is obtained at 55 W (90% of full power). As usual, the efficiency deteriorates as output power reduces, being 91.1% the lowest efficiency measured at 15 W (25% of full power).

C. Evaluation of Dynamic Characteristics

Fig. 11(a) shows the transient response of the output voltage during load step changes using the basic control configuration. Note that the load changes produce significant voltage deviations and large settling times. Fig. 11(b) depicts the transient response of the resonant capacitor voltage, showing a similar dynamic. Note that the steady-state amplitude of the resonant capacitor voltage is constant, independent of the load. This fact was predicted theoretically by (18), (20), and (21). The control scheme modifies the switching frequency when the load changes to maintain M constant in steady state; see (21). By this mechanism, the output voltage and the amplitude of the resonant capacitor voltage are constants in steady state, as observed in (18) and (20). Conversely, the input and output currents rely

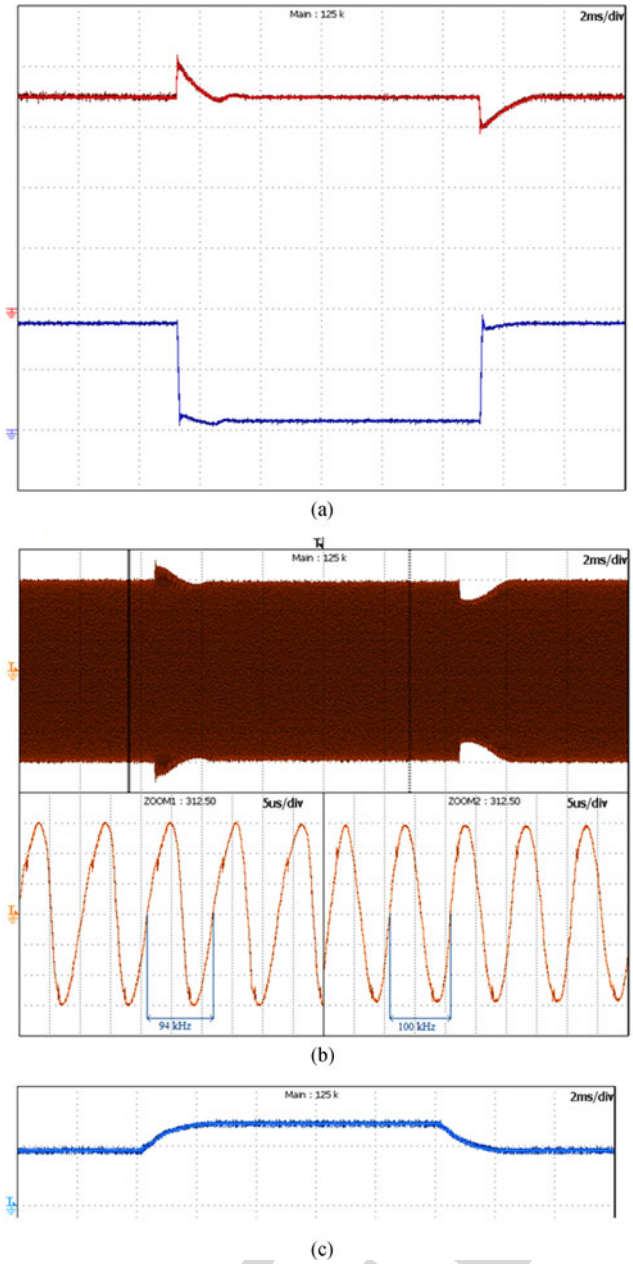

Fig. 11. Load transient response of the basic control configuration ($k_o = 0$): (a) output voltage (red, 10 V/div, 2 ms/div) and current (blue, 1 A/div), (b) resonant capacitor voltage (20 V/div, 2 ms/div), v_c zoom (5 μs/div), and (c) signal u (2 V/div, 2 ms/div).

on the load condition, as predicted by (17) and (19). The areas marked in Fig. 11(b) have been zoomed-in and shown in the lower side of this figure. As it can be seen, the switching frequency increases from 94 to 100 kHz to regulate the output voltage when the load changes from FL to 10% of FL. These experimental measures are well matched with the theoretical results shown in Fig. 2. It is interesting to observe that the quality of the resonant waveforms improves when the switching frequency approaches the resonant frequency. Furthermore, Fig. 11(c) shows the transient response of the input signal of the modulator (u). Note that the basic control has slow dynamics with a settling time around 2 ms.

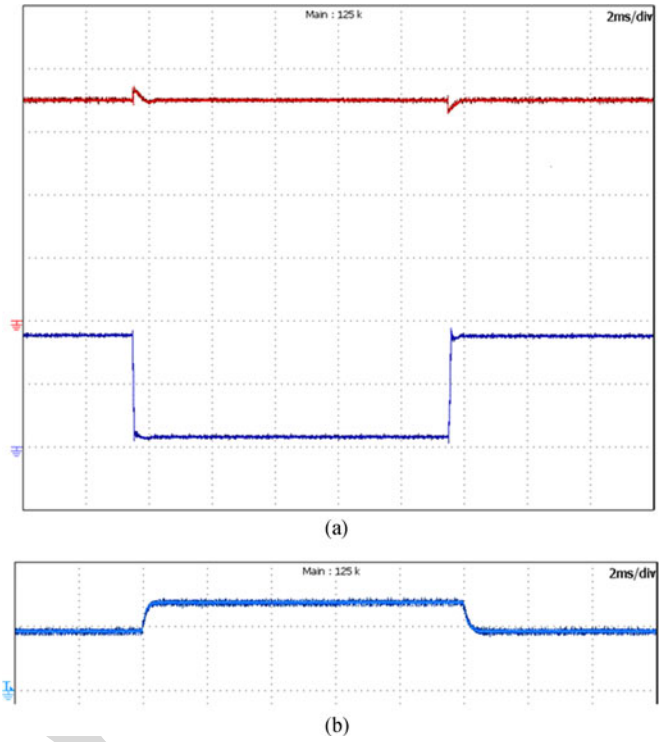

Fig. 12. Load transient response of the enhanced control configuration ($k_o = V_{\rm ref}/V_i$): (a) output voltage (red, 10 V/div, 2 ms/div) and current (blue, 1 A/div), and (b) signal u (2 V/div, 2 ms/div).

Fig. 12(a) shows the transient response of the output voltage during load changes using the enhanced control. As predicted by Fig. 7(c) and Table IV, the transient response is drastically improved. In fact, the voltage overshoots and setting times are clearly reduced from 5 to 1 V and from 1.8 to 0.4 ms, respectively. These enhancements are the consequence of the transient response improvement in the input signal of the modulator (u), as depicted in Fig. 12(b). It means that in the case of load-step changes, the feed-forward term helps the modulator to rapidly find an appropriate switching frequency to ensure a fixed-output voltage.

The load transient response is also evaluated for different values of the input voltage. Fig. 13 shows the results for $V_i = 10$ V and Fig. 14 for $V_i = 14$ V. Note that the voltage deviations during load changes reduce as the input voltage increases (i.e., when the gain of the converter reduces).

In any case, the most important issue is that the dynamic behavior of the enhanced control is still superior than the performance of the basic control for any value of the input voltage; compare Figs. 11–14. In particular, the transient response is faster with lower voltage deviations and settling times (benefit of the enhanced control), as expected from the theoretical analysis.

However, the drawback associated to the enhanced control is the additional measurement (i_o) required to implement the feed-forward term, increasing the overall cost of the system. Therefore, regarding the desired performance and cost, one of the two proposed control configurations should be applied to the converter.

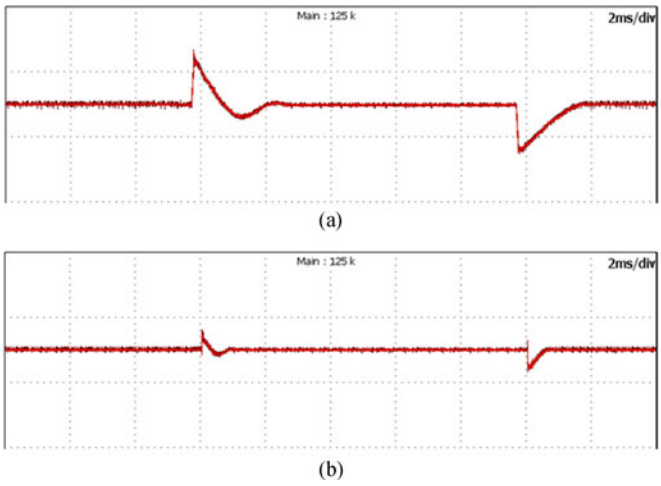

Fig. 13. Load transient response for $V_i = 10\,\text{V}$ and $V_{\text{ref}} = 35\,\text{V}$. (a) Basic control configuration ($k_o = 0$). (b) Enhanced control configuration ($k_o = V_{\text{ref}}/V_i$). 10 V/div, 2 ms/div.

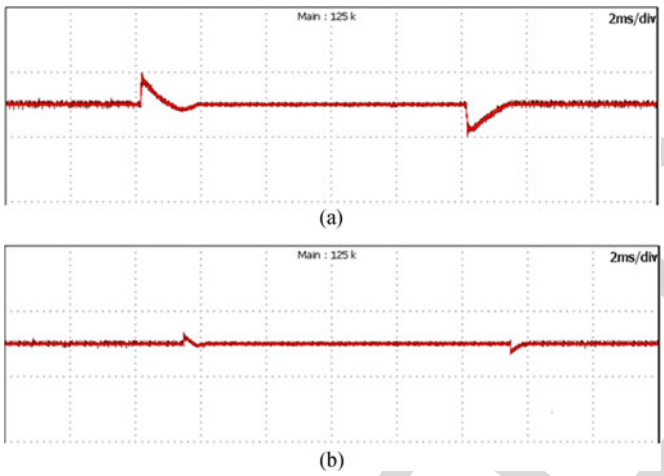

Fig. 14. Load transient response for $V_i = 14\,\text{V}$ and $V_{\text{ref}} = 35\,\text{V}$. (a) Basic control configuration ($k_o = 0$). (b) Enhanced control configuration ($k_o = V_{\text{ref}}/V_i$). 10 V/div, 2 ms/div.

VI. Conclusion

A frequency-modulation control scheme for the class-D CSPRC was proposed in this paper. This control has two possible configurations (basic and enhanced), according to the use or no use of the output-inductor current feed-forward term. The study reveals the superior performance of the enhanced control configuration in terms of fast transient response during load step changes, i.e lower voltage deviations and settling times. The price to pay for this was an increase of cost due to the measure of an extra current. A theoretical study conducting to the design of both control configurations was also proposed in this paper. The study starts with the derivation of proper dynamic models for the converter and the complete closed-loop system. Next, a control design procedure was presented including a design example for illustrative purposes.

The basic and enhanced control configurations can be applied to other current-source parallel resonant topologies including half bridge, full bridge, and other configurations by slightly modifying the logic circuit of the modulator. The proposed control configurations were promising closed-loop control systems to be employed in switching power supplies. The extension to other applications was left for future research work.

Appendix

This Appendix shows the coefficients of the transfer functions expressed in (34) and (35)

$$A_1 = V_c + I_i\ M\ R \tag{A1}$$
$$A_2 = C\ L_o V_c + C_o\ I_i\ L_o M\ R \tag{A2}$$
$$A_3 = I_i\ L_o\ M + C\ R\ V_c + C_o\ R\ V_c \tag{A3}$$
$$A_4 = V_c + I_i\ M\ R \tag{A4}$$
$$B_1 = C\ C_o\ L_i\ L_o\ R \tag{A5}$$
$$B_2 = C\ L_i\ L_o \tag{A6}$$
$$B_3 = C\ L_i\ R + C_o\ L_i\ R + C_o\ L_o\ M^2\ R \tag{A7}$$
$$B_4 = L_i + L_o\ M^2 \tag{A8}$$
$$B_5 = M^2\ R \tag{A9}$$
$$C_1 = I_i\ M\ R\ L_i \tag{A10}$$
$$C_2 = -R\ M\ V_c. \tag{A11}$$

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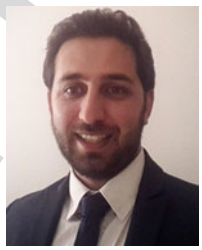

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Queries

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Frequency-Modulation Control of a DC/DC Current-Source Parallel-Resonant Converter

Mohammad Moradi Ghahderijani, Miguel Castilla, Arash Momeneh, Jaume Tomas Miret, *Member, IEEE*, and Luis Garcia de Vicuña

***Abstract*—This paper proposes a frequency-modulation control scheme for a dc/dc current-source parallel-resonant converter with two possible configurations. The basic configuration comprises an external voltage loop, an internal current loop, and a frequency modulator: the voltage loop is responsible for regulating the output voltage, the current loop makes the system controllable and limits the input current, and the modulator provides robustness against variations in resonant component values. The enhanced configuration introduces the output inductor current as a feed-forward term and clearly improves the transient response to fast load changes. The theoretical design of these control schemes is performed systematically by first deriving their small-signal models and second using Bode diagram analysis. The actual performance of the proposed control schemes is experimentally validated by testing on a laboratory prototype.**

***Index Terms*—Control design, control systems, dc–dc power converters, frequency modulation, resonant converters.**

I. Introduction

SINCE the emergence of the resonant technology, major research efforts have been conducted to apply the enhanced features of resonant converters to practical applications [1]–[8]. Induction heating [1], electric vehicle [2], lighting system [3], robotic industry [4], [5], and contactless energy-transfer system [6]–[8] are just a short list of examples. DC–DC conversion category is another industry example of great importance for these converters. Battery charging, electronic air purifiers, and switching power supplies are among these applications, ranging from low to high power [9]–[15]. A great interest has been taken in these converters due to their generated high frequency sinusoidal waveforms, reducing the electromagnetic interference and switching losses [16]. The control strategy has been one of the challenging research keys in this field. For voltage-source series-resonant converters, many control strategies have been analyzed and investigated [17]–[23], turning this into a mature technology nowadays. However, compared to the series-resonant topologies, parallel-resonant converters absorb a continuous smooth current from the input source, offering low current stress to switches [24]. Likewise, the reactive power circulates inside the parallel resonant tank and only the active power is supplied through the switches. This feature provides the capability of generating high current and voltage levels by using low VA-rated switches, reducing conduction losses. In addition, these converters provide more facilities such as short-circuited protection and paralleling capabilities. For the reasons outlined above, the research on the current-source parallel-resonant converters (CSPRC) has recently attracted more interest [25]–[31]. In particular, in [25], a current source topology has been proposed to supply a multireceiver inductive contactless energy transfer system. In this topology, a buck converter has been utilized to obtain an input current source with constant amplitude, supplying the resonant inverter. In [26], a simple modulation technique has been proposed for this type of converter and then applied to an induction heating system [27]. This method is then further developed in [28]. In [29], the modulation technique has been applied to an inductive contactless energy transfer system. A delta–sigma modulator is also applied to a class-D CSPRC in [30]. In all these works, the current-source converters operate in open loop and thus they exhibit a high sensitivity to external disturbances and parameter variations. In [31], a closed-loop control scheme with amplitude modulation has been presented for a dc/dc CSPRC. A robust behavior against load changes was demonstrated in this study by simulation results; however, some drawbacks inherent to the amplitude modulation limit its practical use.

The aim of this paper is to introduce a control scheme for the dc/dc class-D CSPRC intended for switching power supplies. The control scheme has two possible configurations. The basic configuration is responsible for both regulating the output voltage and providing zero voltage switching (ZVS) conditions. A cascaded control scheme is proposed to this end, including an external voltage loop and an internal current loop. ZVS conditions are guaranteed by driving the switches with a robust frequency modulation technique. In addition, an enhanced control configuration is presented in this paper in order to further improve the load transient response of the basic configuration. The design of the control schemes is based on two steps. First,

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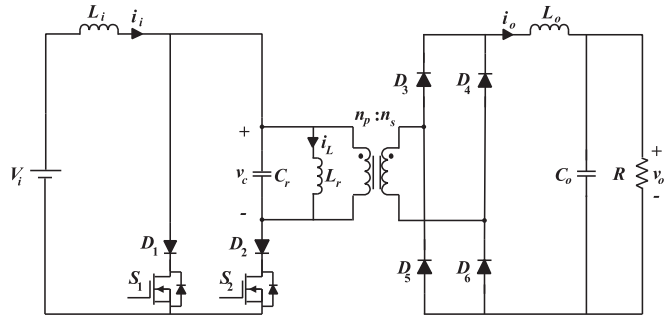


Fig. 1. Power circuit of the class-D CSPRC.

a dynamic model of the open-loop CSPRC is obtained. Afterward, the small-signal characteristics of the obtained averaged model are derived. Second, the dynamic model for the closed-loop system is formulated and a systematic procedure to design the control gains is presented.

The theoretical contributions of this paper are: the large-signal model of the CSPRC operating with frequency modulation; 2) its small-signal model; 3) the control scheme, including the basic and enhanced control-loop configurations and the frequency modulator (FM); and 4) the systematic design procedure for deriving the control gains. As far as authors know, there are no previous studies exploring these four topics together or separately for the considered resonant topology.

This paper is structured as follows. Section II derives the large-signal model of the class-D CSPRC and its averaged small-signal model. Section III introduces the basic and enhanced control configurations, including the FM. Section IV presents the design process of the proposed control scheme intended for dc/dc applications. Section V verifies the theoretical contributions by selected experimental results in a laboratory prototype. Finally, Section VI gives the conclusions.

II. Dynamic Modeling of the Class-D CSPRC

Fig. 1 shows the power circuit of the dc/dc class-D CSPRC. The class-D resonant inverter includes an input inductor (L_i), a second-order parallel-resonant tank (L_r and C_r) and a high-frequency transformer with winding turns ratio $n_p : n_s$. The resonant tank is loaded through a full-bridge diode rectifier and a second-order low-pass filter (L_o and C_o) to get a dc output voltage. The operation principle of this converter using frequency modulation was presented in detail in [24], and thus it is not repeated here.

The first contribution of this paper is the development of an adequate dynamic description of the class-D CSPRC converter for dc switching power supply applications. This model is essential for the control design process. Below is a step-by-step derivation of the dynamic model.

A. State-Space Model

The assumptions to derive the model are: 1) the components are ideal and 2) the circuit is driven by frequency modulation. In this case, the control input is the angular switching frequency ω_s. This variable will be provided by the control system in order to reach the control objectives (i.e., output voltage regulation and operation under ZVS conditions). Under these assumptions and taking into account the equivalent circuits of the converter presented in [24], the differential state-space equations can be expressed as follows:

$$\frac{di_i}{dt} = \frac{1}{L_i}\left[V_i - \left(\frac{1+\operatorname{sgn}(\sin\omega_s t)}{2}\right) v_c\right] \tag{1}$$

$$\frac{dv_c}{dt} = \frac{1}{C_r}\left[\left(\frac{1+\operatorname{sgn}(\sin\omega_s t)}{2}\right) i_i - i_L - \frac{n_s}{n_p}\operatorname{sgn}(v_c)\, i_o\right] \tag{2}$$

$$\frac{di_L}{dt} = \frac{1}{L_r} v_c \tag{3}$$

$$\frac{di_o}{dt} = \frac{1}{L_o}\left[\frac{n_s}{n_p}|v_c| - v_o\right] \tag{4}$$

$$\frac{dv_o}{dt} = \frac{1}{C_o}\left[i_o - \frac{v_o}{R}\right] \tag{5}$$

where i_i stands for the input current variable, v_c and i_L are the resonant state variables, and v_o and i_o are the output filter state variables. According to [32], the state-space variables can be divided in two subgroups: fast and slow variables. The resonant state variables are fast variables and evolve the following sinusoidal waveforms. Input current and output voltage and current are slow variables. They evolve slowly compared to the dynamics of resonant waveforms.

B. Averaged Modeling of the Resonant State Variables

The averaged method presented in [32] is used here to obtain a proper dynamic model. In this method, the resonant state variables are approximated as sinusoidal waveforms including slow time-varying amplitudes and phases, defined as

$$v_c = V_c \sin(\omega_s t - \alpha) \tag{6}$$

$$i_L = I_L \sin(\omega_s t - \beta) \tag{7}$$

where V_c and I_L are the peak values of the resonant state variables, and α and β are the initial phases. These variables are then inserted into (2) and (3). By applying harmonic linearization and harmonic balance to the resulting model, the following equation is derived:

$$\frac{d\bar{v}_c}{dt} = \frac{1}{C_{\text{eq}}}\left[\frac{m}{2}\,\bar{i}_i - \frac{n_s}{n_p}\,\bar{i}_o\right] \tag{8}$$

where the symbol – denotes averaged value over a half-switching cycle, and the equivalent capacitor C_{eq} and the new variable m can be expressed as

$$C_{\text{eq}} = \pi^2 C_r/8 \tag{9}$$

$$m = \sqrt{1 - \left[\frac{\pi^2 Q}{4\,R}\,\frac{\bar{v}_c}{\bar{i}_i}\left(\frac{\omega_s}{\omega_o} - \frac{\omega_o}{\omega_s}\right)\right]^2}. \tag{10}$$

Note that m is a variable that contains information about the system state in an averaged sense (through the variables $\bar{v}_c$ and $\bar{i}_i$) and the control action ω_s. It is used here simply

to compact the final expressions of the models. In (10), the variables Q and ω_o represent the quality factor and angular resonant frequency of the resonant tank. In addition, Z_o is the characteristic impedance. These variables are defined as

$$Q = R/Z_o \tag{11}$$

$$\omega_o = 1/\sqrt{L_r\, C_r} \tag{12}$$

$$Z_o = \sqrt{L_r/C_r}. \tag{13}$$

Further details on model derivation can be found in [33]–[35], where the averaged models of other resonant topologies have been derived. Note that, in this case, the resonant tank is described in an averaged sense because only one differential equation (8) models the dynamics of the averaged resonant capacitor voltage. This equation contains all the necessary information to reproduce the transient and steady-state behavior of the resonant tank in an averaged sense. Also, note that this equation is nonlinear.

C. Averaged Modeling of Slow Variables

The averaged dynamics of the slow variables, including the input and output state variables, are derived by using the time-varying averaging over a half-switching cycle, resulting in

$$\frac{d\overline{i_i}}{dt} = \frac{1}{L_i}.\left[V_i - \frac{m}{2}\,\overline{v}_c\right] \tag{14}$$

$$\frac{d\overline{i}_o}{dt} = \frac{1}{L_o}\left[\frac{n_s}{n_p}\overline{v}_c - \overline{v}_o\right] \tag{15}$$

$$\frac{d\overline{v}_o}{dt} = \frac{1}{C_o}.\left[\overline{i}_o - \frac{\overline{v}_o}{R}\right]. \tag{16}$$

Therefore, the complete averaged large-signal model of the class-D CSPRC is expressed by (8) and (14)–(16).

As far as authors know, the large signal model for the frequency-modulated CSPRC has not been previously studied. Hence, this model constitutes the first contribution of this paper. The accuracy of this model is validated in Section II-E by selected simulation results.

D. Equilibrium Point

In steady-state conditions, all the averaged variables reach their equilibrium point. By considering $d\overline{i_i}/dt = 0$, $d\overline{v_c}/dt = 0$, $d\overline{i_o}/dt = 0$, and $d\overline{v_o}/dt = 0$, the equilibrium point of the model (8) and (14)–(16) can be expressed as

$$I_i = \frac{V_0^2}{R\,V_i} \tag{17}$$

$$V_c = \frac{2V_i}{M} \tag{18}$$

$$I_o = \frac{V_o}{R} \tag{19}$$

$$V_o = \frac{n_s}{n_p}\frac{2V_i}{M} \tag{20}$$

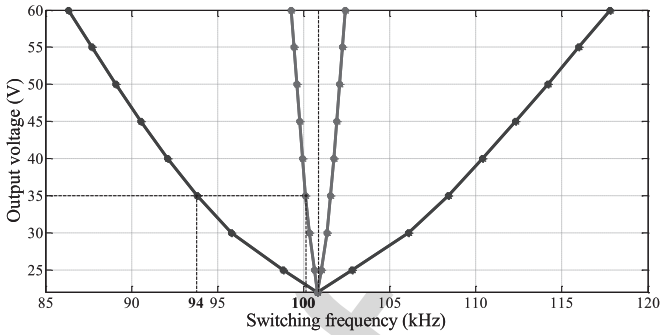


Fig. 2. Output voltage as a function of the switching frequency (FL in blue and 10% of FL in red).

TABLE I
VALUES OF THE POWER COMPONENTS

Symbol	Quantity	Value
V_i	Input voltage	12 V
L_i	Input filter inductor	300 μH
C_r	Resonant capacitor	470 nF
L_r	Resonant inductor	5.3 μH
$n_p : n_s$	Transformer turns ratio	1:1
L_o	Output filter inductor	100 μH
C_o	Output filter capacitor	470 μF
V_o	Output voltage	35 V
R	Full-load resistor	20 Ω

where M is the steady-state value of m (i.e., the equilibrium point of m), which can be written as

$$\frac{1}{M} = \sqrt{1 + \left[\frac{\pi^2}{8}\,Q\left(\frac{n_s}{n_p}\right)^2\left(\frac{\omega_s}{\omega_o} - \frac{\omega_o}{\omega_s}\right)\right]^2}. \tag{21}$$

Note that the equilibrium point depends on the control input ω_s, the resonant circuit parameters, the input voltage, and the load.

The output voltage in steady state can be easily determined from (20) and (21). Fig. 2 depicts this voltage as a function of the switching frequency for two load conditions: full load (FL) in blue and 10% of FL in red. The nominal values of the power components listed in Table I are used to draw the figure. Note that the output voltage can be maintained constant in steady state by adjusting conveniently the switching frequency. In fact, Fig. 2 also shows the theoretical values of the switching frequency that provides the nominal output voltage for the two considered load conditions.

E. Validation of the Averaged Large-Signal Model

The validity of the derived large-signal model expressed in (8) and (14)–(16) is evaluated by comparing selected simulation results with those obtained by the state-space model expressed in (1)–(5). Both models are implemented in MATLAB–Simulink, and the obtained results are shown in Fig. 3. Two different switching frequencies are considered to validate the averaged model in different operating points. During the first interval, the switching frequency is fixed at 91 kHz. At $t = 10$ ms, the

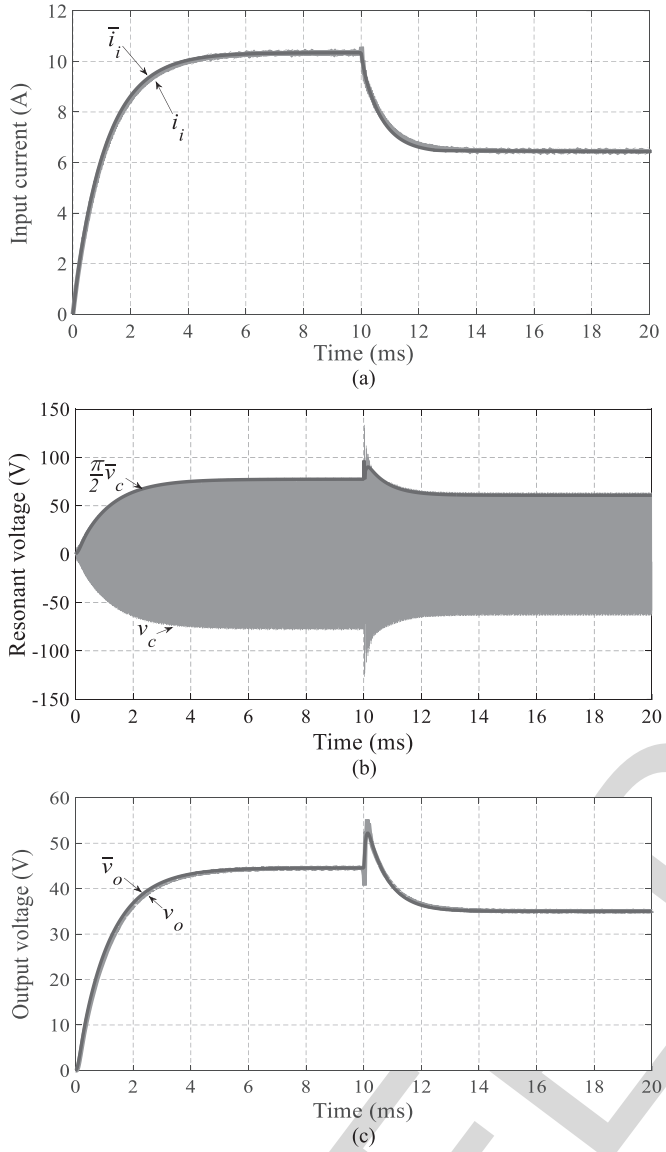


Fig. 3. Comparison of waveforms generated by the state-space model and the averaged large-signal model for two different switching frequencies ($0 < t < 10$ ms: 91 kHz, 10 ms $< t < 20$ ms: 94 kHz) and FL condition: (a) input current, (b) resonant capacitor voltage, and (c) output voltage.

switching frequency is changed to 94 kHz. This frequency is maintained to the end of the test. The results show good agreement between the models, although some small differences appear when the switching frequency is abruptly changed at $t = 10$ ms. These mismatches are clearly caused by the assumptions made in the large-signal model derivation. However, for control design purposes, the observed high-frequency transients are not important due to the limited control bandwidth (BW).

F. Small-Signal Model

The small-signal model of the converter is derived by following the conventional approach based on perturbing and linearizing the large-signal model [36]. The systematic procedure is presented below. First, the state variables are decomposed in dc (I_i, V_c, I_o, V_o and M, all defined in [17]–[20]) and ac ($\widehat{\mathrm{i}_i}$, $\widehat{\mathrm{v}_c}$, $\widehat{\mathrm{i}_o}$, $\widehat{\mathrm{v}_o}$, and $\widehat{m}$) terms, given as follows:

$$\bar{i}_i = I_i + \widehat{i_i} \tag{22}$$

$$\bar{v}_c = V_c + \widehat{v_c} \tag{23}$$

$$\overline{i_o} = I_o + \widehat{i_o} \tag{24}$$

$$\bar{v}_o = V_o + \widehat{v_o} \tag{25}$$

$$m = M + \hat{m}. \tag{26}$$

Second, the amplitudes of the ac terms are considered small in comparison to the dc quantities (obtained equilibrium values), i.e.,

$$\widehat{i_i} \ll I_i \tag{27}$$

$$\widehat{v_c} \ll V_c \tag{28}$$

$$\widehat{i_o} \ll I_o \tag{29}$$

$$\widehat{v_o} \ll V_o \tag{30}$$

$$\hat{m} \ll M. \tag{31}$$

Third, by substituting (22)–(26) in (8) and (14)–(16), and taking into account that the products of two ac terms are negligible, the small-signal model is derived. It can be written in matrix form as follows:

$$\begin{bmatrix} sL_i & M & 0 & 0 \\ -M & sC_{\mathrm{eq}} & n_s/n_p & 0 \\ 0 & -n_s/n_p & sL_o & 1 \\ 0 & 0 & -1 & sC_o + (1/R) \end{bmatrix} \begin{bmatrix} \hat{i}_i(s) \\ \hat{v}_c(s) \\ \hat{i}_o(s) \\ \hat{v}_o(s) \end{bmatrix} = \begin{bmatrix} -V_c \\ I_i \\ 0 \\ 0 \end{bmatrix} \cdot \hat{m}(s) \tag{32}$$

where s is the Laplace operator. Note that all the transfer functions that characterize the behavior of the converter in small signal can be derived from (32).

The obtained small-signal model constitutes the second contribution of this paper. This model is then utilized for control design as explained in Section IV.

III. Proposed Control Scheme

This section introduces a control scheme for the parallel-resonant converter with two possible configurations for the external voltage loop. The internal current loop and the FM are also presented in detail.

A. Voltage and Current Control Loops

Fig. 4 shows the diagram of the proposed control scheme. It is based on two control loops and an FM. The internal control loop makes the system controllable and limits the input current. To this end, it processes the input current error using a

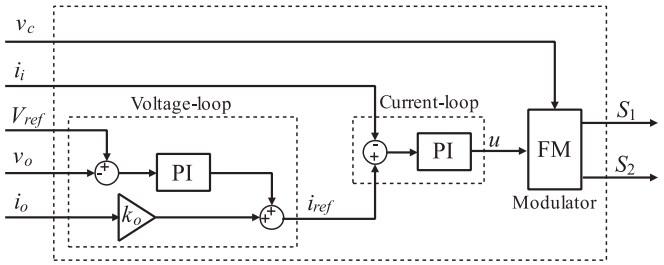


Fig. 4. Diagram of the two proposed control schemes. Basic configuration (i_o is not measured in this case and $k_o = 0$) and enhanced configuration (i_o is measured in this case and $k_o = V_{\rm ref}/V_i$).

proportional-integral (PI) regulator and provides the signal u to the input of the modulator.

The external voltage loop is responsible to regulate the output voltage. It has two control terms: a feedback term that tries to eliminate the output voltage error using a PI regulator and a feed-forward term of the output current. The feedback term ensures that the output voltage matches the reference voltage in steady state, thus compensating the effects of unmodeled elements such as parasitic resistors and transformer leakage inductances. In the case of load-step changes, the feed-forward term helps the modulator to rapidly find an appropriate switching frequency to ensure a fixed-output voltage, yielding in a fast transient response.

The proposed controller is called here basic configuration when $k_o = 0$ and enhanced configuration when $k_o = I_i/I_o$. In the enhanced controller, the steady-state currents in the feed-forward gain k_o rely on the load condition. However, from (18) and (20) and assuming $V_o = V_{\rm ref}$, the feed-forward gain is independent of the load condition and can be written as

$$k_o = \frac{V_{\rm ref}}{V_i}. \tag{33}$$

The enhanced controller is introduced in order to improve the transient response, i.e, to get a negligible output voltage deviation and lower settling time. This is considered as the benefit of this control configuration. However, an additional measurement i_o is required in this case, slightly increasing the cost of the system.

B. Frequency Modulator

This section proposes an FM for the CSPRC. The modulator is derived from the phase modulator presented in [37] for voltage-source resonant converters. The differences between both modulators are also highlighted below.

Fig. 5(a) shows the proposed FM. It is based on the generation of a saw-tooth waveform synchronized by the zero crossing detection of the resonant capacitor voltage. This waveform is then compared with the output signal of the controller u in order to generate the gate signals (S_1 and S_2) by using an RS flip-flop. Fig. 5(b) shows the main waveforms of the modulator. Note that the switching period depends on the load conditions, as predicted by (21). It is worth mentioning that the ramp amplitude is always one in this modulator in order to modify the

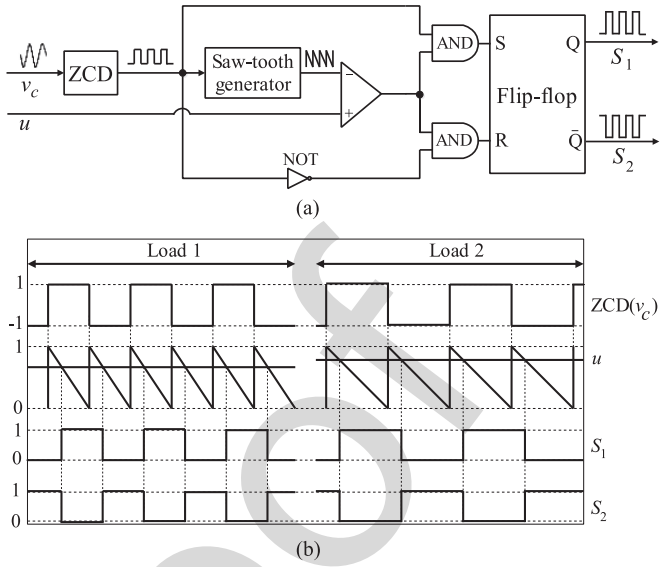


Fig. 5. Proposed FM including a variable slope, fixed amplitude saw-tooth generator: (a) diagram and (b) main waveforms for two different load conditions.

switching period as a function of the load condition. The saw-tooth generator produces this distinctive feature by means of a closed-loop control using a PI regulator; see details in [37]. The most promising feature of both modulators is the high robustness to resonant parameter variations. This feature is attributed to the sensing of the resonant tank state, through the measure of a resonant state variable. Thus, changes on resonant components due to temperature, tolerance, age, etc., are perfectly absorbed by the modulator. The main differences between the two modulators are as follows.

1) The resonant capacitor voltage instead of the inductor current is used to provide ZVS conditions.
2) The slope of the ramp signal is reversed to operate below resonance (the voltage-source resonant converter operates above resonance).
3) Only one input signal u is required to regulate the output voltage (the phase modulator needs two signals).

The proposed control scheme is the third contribution of this paper. The novelties of this configuration are: first, the feed-forward term included in the conventional two loop control in order to accelerate the transient response during load step changes; and second, the adaptive modulator used to synchronize the control action with the zero crossing of the resonant capacitor voltage, thus providing ZVS condition. In addition, the modulator provides a robust operation against internal and external disturbances (such as variations in resonant tank parameters and input voltage, respectively).

IV. Control Design

This section presents the design procedure to obtain the gains of the two PI controllers used in the proposed control scheme. A numerical example is also included to illustrate the procedure in detail. This design procedure constitutes the fourth contribution

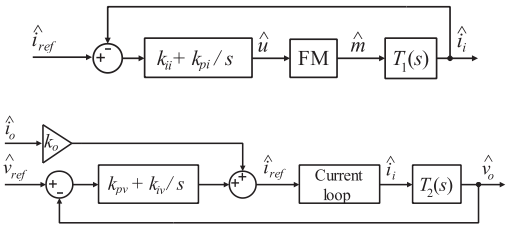


Fig. 6. Small-signal diagram of the (a) internal control loop and (b) external control loop.

of this paper. A numerical example is also included to illustrate the procedure in detail.

A. Design Procedure

The control design proceeds as follows.

1) The closed-loop transfer functions of the system are first obtained by using the derived small-signal model.
2) The frequency-domain specifications of the closed-loop system are fixed in terms of desired control BW and phase margin (PM).
3) The gain values of the PI controllers satisfying the specifications are selected.

To this end, Bode diagrams of different set of gain values are examined until the specifications are met.

B. Closed-Loop Small-Signal Models

Fig. 6 shows the small-signal diagram of the internal and external control loops. Note that the two PI controllers are included in the figure. The other transfer functions involved in the diagram are derived below.

The control to input-current $T_1(s)$ and input-current to output-voltage $T_2(s)$ transfer functions are obtained from the small-signal model expressed in (24). These transfer functions are

$$T_1(s) = \frac{\hat{i}_i(s)}{\hat{m}(s)} = \frac{A_1\ s^3 + A_2\ s^2 + A_3\ s + A_4}{B_1 s^4 + B_2 s^3 + B_3 s^2 + B_4 s + B_5} \quad (34)$$

$$T_2(s) = \frac{\hat{v}_o(s)}{\hat{i}_i(s)} = \frac{C_1\ s + C_2}{B_1 s^4 + B_2 s^3 + B_3 s^2 + B_4 s + B_5}. \quad (35)$$

The coefficients of these transfer functions can be found in the Appendix.

The transfer function of the proposed modulator is deduced according to the following points and assumptions.

1) It is well known that the small-signal model of a modulator involving a ramp signal coincides with the inverse of the amplitude of this signal (i.e., $1/V_{\rm ramp}$) [36].
2) In the proposed modulator, a closed-loop control is used in the saw-tooth generator to fix the amplitude of the ramp signal to one ($V_{\rm ramp} = 1$).
3) This control loop is fast enough compared to the BW of the internal and external control loops.

Thus, the transfer function of the modulator can be expressed as

$$\frac{\hat{m}}{\hat{u}} = \frac{1}{V_{\rm ramp}} = 1. \quad (36)$$

TABLE II
FREQUENCY-DOMAIN SPECIFICATIONS

Control loops	BW (kHz)	PM (°)
Current loop	7.467	60
Voltage loop	0.593	60

TABLE III
VALUES OF THE CONTROL GAINS AND PARAMETERS

Symbol	Quantity	Value
k_{pi}	Current-loop proportional gain	0.4 A^{-1}
k_{ii}	Current-loop integral gain	30 Hz/A
k_{pv}	Voltage-loop proportional gain	0.01 Ω^{-1}
k_{iv}	Voltage-loop integral gain	120 Hz/Ω
k_o	Feed-forward gain (basic control)	0
k_o	Feed-forward gain (enhanced control)	2.9
$V_{\rm ref}$	Reference output voltage	35 V

The design of the PI controllers is based on making the dynamic characteristics meet the control design specifications.

Table II lists these specifications for the internal and external control loops. In the internal current loop, the control BW is 1.1 decades below the minimum switching frequency to get a fast current transient response. In the external voltage loop, the control BW is 1.1 decades below the control BW specification of the current loop in order to avoid undesired interactions between these control loops. The PMs are high enough to prevent the converter from going to the instability region.

The dynamic characteristics of the CSPRC can be extracted from the current and voltage loop gains. From Fig. 6, these transfer functions can be written as

$$T_i(s) = \left[k_{pi} + \frac{k_{ii}}{s}\right] T_1(s) \quad (37)$$

$$T_v(s) = \left[k_{pv} + \frac{k_{iv}}{s} - \frac{k_o}{R}\right] T_2(s). \quad (38)$$

Note that the loop gains depend directly on the gains of the two PI controllers, as usual. In the voltage loop gain, a perfect tracking of the reference current is assumed, i.e., $\hat{i}_i(s)/\hat{i}_{\rm ref}(s) = 1$. This is actually a good approximation due to the reduced control BW of the voltage loop. In addition, the feed-forward term k_o appears in the voltage loop gain, so that the dynamic characteristics will be analyzed for: the current loop, the basic voltage loop ($k_o = 0$), and the enhanced voltage loop ($k_o = V_{\rm ref}/V_i$). Hence, the impact of k_o on the transient response will be also analyzed considering the closed-loop transfer function shown in (38), derived from the small-signal model.

C. Design of the Internal and External Control Loops

The values of the PI gains are obtained according to the design specifications. Several Bode diagrams are represented with different PI gains until the specifications are met. Once this process is finished, the final values of the PI gains are captured and listed in Table III. The values of the feed-forward

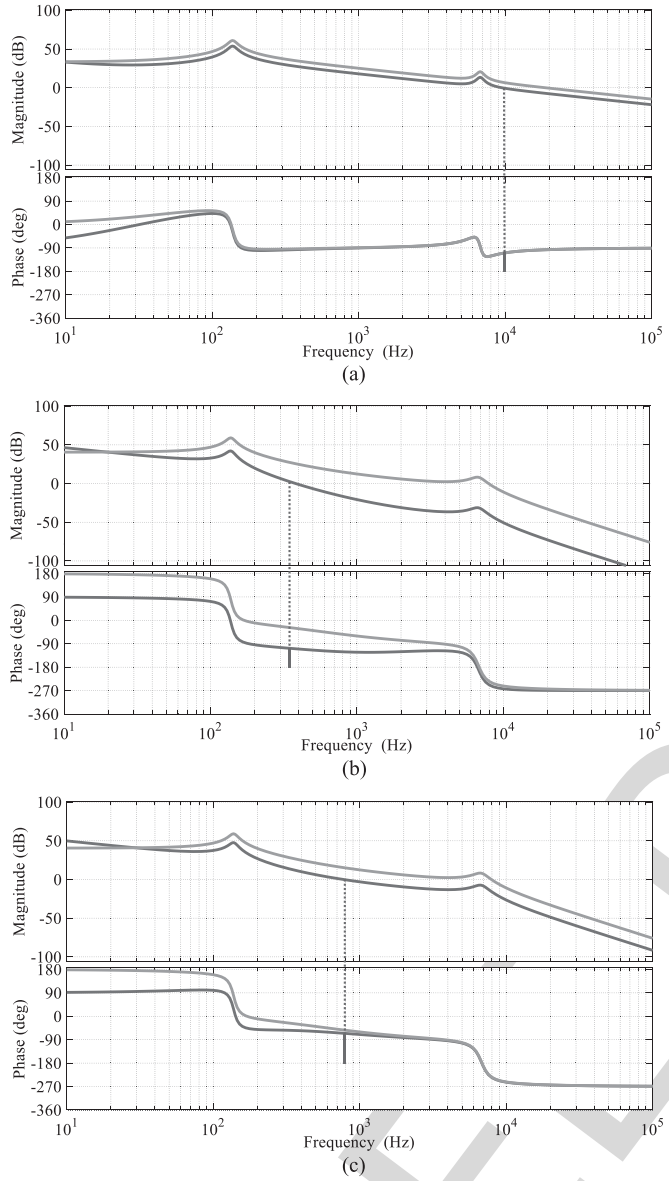


Fig. 7. Bode diagrams of (a) current loop gain, (b) voltage loop gain for the basic control ($k_o = 0$), and (c) voltage loop gain for the enhanced control ($k_o = V_{\rm ref}/V_i$) for FL condition (blue: compensated and orange: uncompensated).

gains for the basic and the enhanced control configurations are also included in the table. Fig. 7 shows the Bode diagram of the loop gains for both compensated and uncompensated system at FL condition. Note that the compensated system reduces the control BW to reach the design specifications, as depicted in Fig. 7.

For the current loop, the control BW is 9.43 kHz and the PM is 67.1°, meeting satisfactorily the design specifications. In the basic voltage loop, although the PM is good enough (70.4°), the control BW (0.35 kHz) is lower than the specification. Thanks to the feed-forward term, the enhanced voltage loop shows superior performance by increasing both the control BW (0.81 kHz) and the PM (116.4°). The design specifications are clearly meet by the enhanced control configuration.

TABLE IV
DYNAMIC CHARACTERISTICS FOR DIFFERENT LOAD CONDITIONS

Control scheme	Load condition	Current loop		Voltage loop	
		BW (kHz)	PM (°)	BW (kHz)	PM (°)
Basic	FL	9.43	67.1	0.35	70.4
($k_o = 0$)	10% of FL	8.52	85.2	0.23	98.2
Enhanced	FL	9.43	67.1	0.81	116.4
($k_o = V_{\rm ref}/V_i$)	10% of FL	8.52	85.2	0.67	153.3

TABLE V
PROTOTYPE COMPONENTS

Component	Model
Diodes	20ETF08S
MOSFETs	IRFR4620
MOSFET driver	MCP14E10
Resonant capacitor	MKT type
Op-amps	MCP6022

Table IV shows the dynamic characteristics for different load conditions. Note that the control BW improves as the load increases for both control loops. Conversely, the PM deteriorates as the load increases. Anyway, the design specifications are meet for the current loop and the enhanced voltage loop. In addition, the enhanced voltage loop improves the dynamic characteristics of the basic voltage loop for all load conditions.

V. EXPERIMENTAL RESULTS

This section validates the proposed control scheme with selected experimental results from a laboratory prototype.

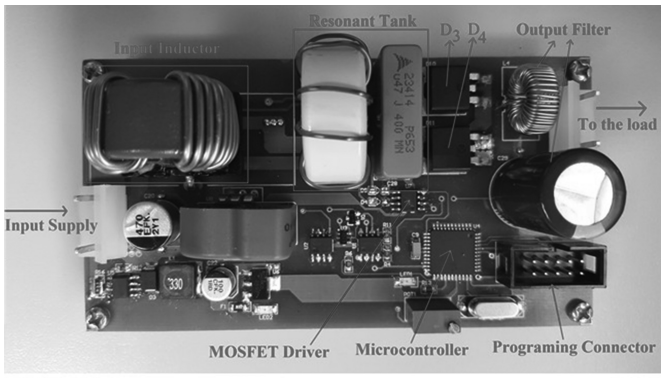
A. Laboratory Prototype

A 60-W laboratory prototype was built including a dc–dc class-D CSPRC with a SPIC33FJ16GS504-I/PT microcontroller as digital control platform. The input and output currents were sensed with current transducers (LTP-15NP). Simple analog circuits including differential amplifiers are used to sense the resonant capacitor and output voltages. Other prototype components are listed in Table V. Fig. 8 shows the top and bottom views of the laboratory prototype.

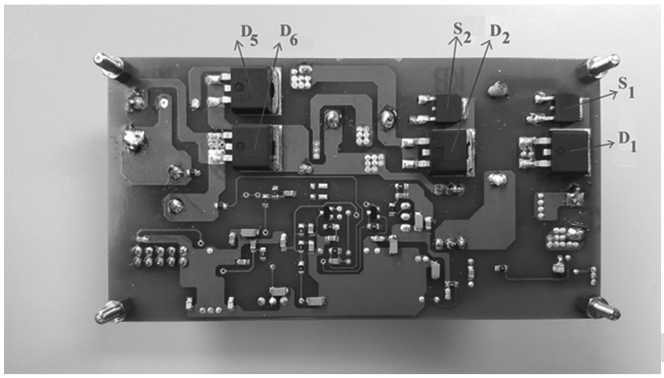
B. Evaluation of Static Characteristics

In this section, the steady-state operation of the CSPRC is evaluated.

Fig. 9 shows the steady-state voltage across the right leg of the class-D inverter shown in Fig. 1 (including the voltages in MOSFET S2 and blocking diode D2) and its associated current for both FL and 10% of FL. Note that the waveform of the switch voltage is similar in both load conditions. The only notable difference is a change in the switching frequency. However, in the switch current waveform, the change in both switching frequency and in amplitude is observed. These features were theoretically predicted by (18)–(21), as discussed in Section V-C.

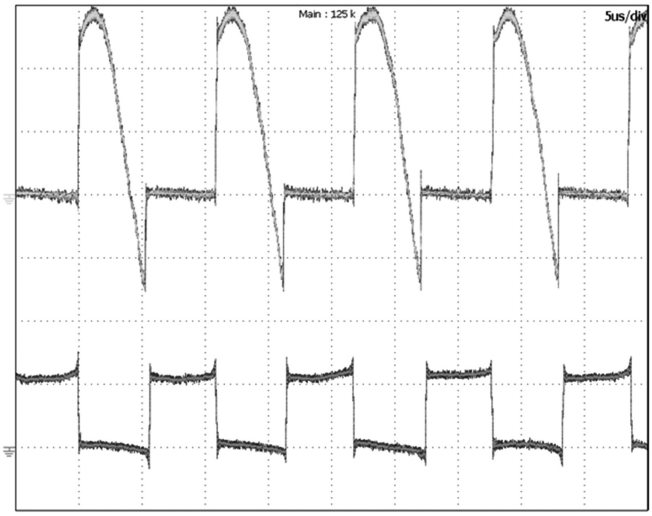


(a)

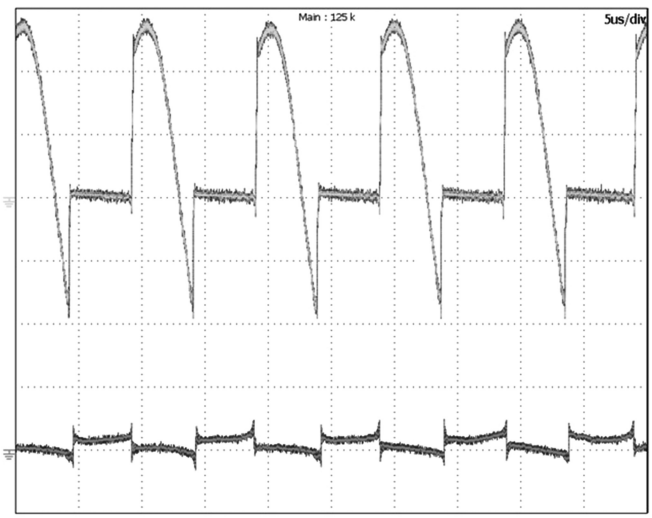


(b)

Fig. 8. Experimental dc–dc CSPRC prototype: (a) top view and (b) bottom view.



(a)



(b)

Fig. 9. Steady-state switch voltage (green, 20 V/div, 5 μs/div) and current (pink, 5 A/div) for: (a) FL and (b) 10% of FL.

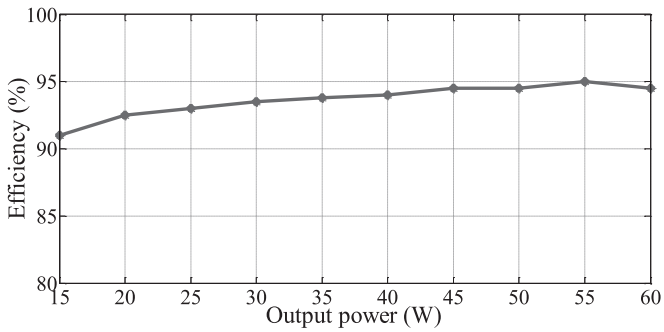


Fig. 10. System efficiency as a function of output power.

Fig. 9 also reveals the ZVS operation of the CSPRC. When the switch is OFF (interval with zero switch current), the switch voltage tracks the resonant capacitor voltage by changing sinusoidally from positive to negative values. In the interval with negative values, the diode D2 is naturally in OFF state and then MOSFET S2 can be driven to ON state. In this case, although S2 is ON, no current flows through the switch due to the blocking diode D2. Thus, the MOSFET S2 is in ON state with zero voltage across before switch current increases during the switch transition from OFF to ON. This mechanism is known as ZVS operation and is characterized by negligible switching losses.

Fig. 10 shows the system efficiency as a function of the output power. The highest efficiency (95%) is obtained at 55 W (90% of full power). As usual, the efficiency deteriorates as output power reduces, being 91.1% the lowest efficiency measured at 15 W (25% of full power).

C. Evaluation of Dynamic Characteristics

Fig. 11(a) shows the transient response of the output voltage during load step changes using the basic control configuration. Note that the load changes produce significant voltage deviations and large settling times. Fig. 11(b) depicts the transient response of the resonant capacitor voltage, showing a similar dynamic. Note that the steady-state amplitude of the resonant capacitor voltage is constant, independent of the load. This fact was predicted theoretically by (18), (20), and (21). The control scheme modifies the switching frequency when the load changes to maintain M constant in steady state; see (21). By this mechanism, the output voltage and the amplitude of the resonant capacitor voltage are constants in steady state, as observed in (18) and (20). Conversely, the input and output currents rely

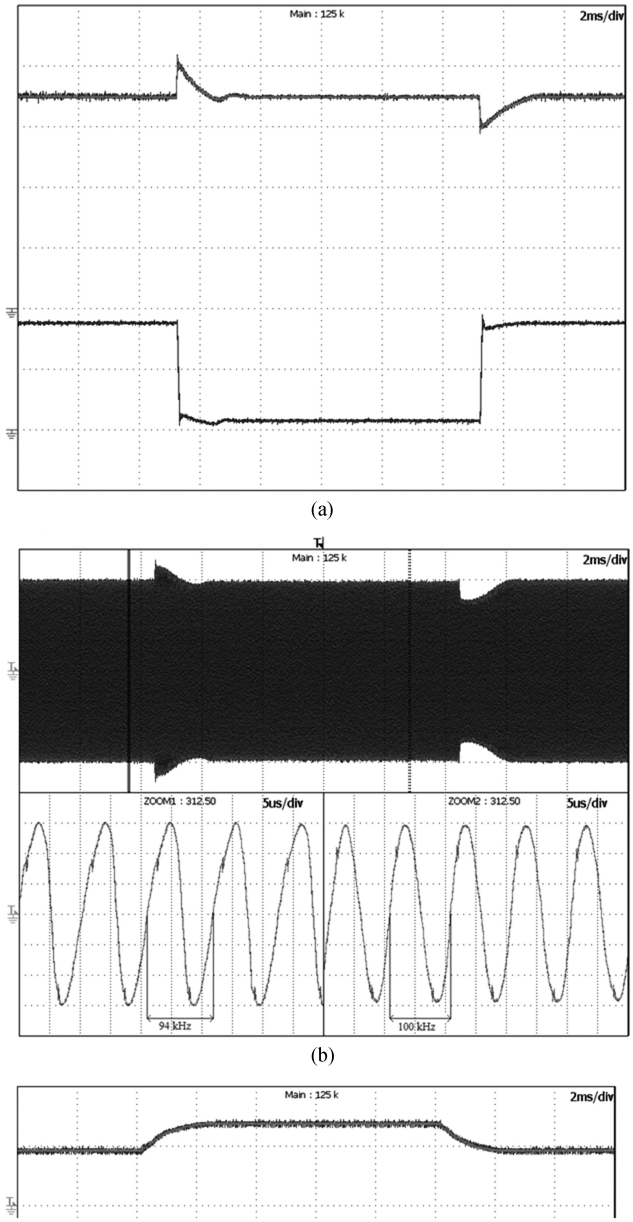


Fig. 11. Load transient response of the basic control configuration ($k_o = 0$): (a) output voltage (red, 10 V/div, 2 ms/div) and current (blue, 1 A/div), (b) resonant capacitor voltage (20 V/div, 2 ms/div), v_c zoom (5 μs/div), and (c) signal *u* (2 V/div, 2 ms/div).

on the load condition, as predicted by (17) and (19). The areas marked in Fig. 11(b) have been zoomed-in and shown in the lower side of this figure. As it can be seen, the switching frequency increases from 94 to 100 kHz to regulate the output voltage when the load changes from FL to 10% of FL. These experimental measures are well matched with the theoretical results shown in Fig. 2. It is interesting to observe that the quality of the resonant waveforms improves when the switching frequency approaches the resonant frequency. Furthermore, Fig. 11(c) shows the transient response of the input signal of the modulator (u). Note that the basic control has slow dynamics with a settling time around 2 ms.

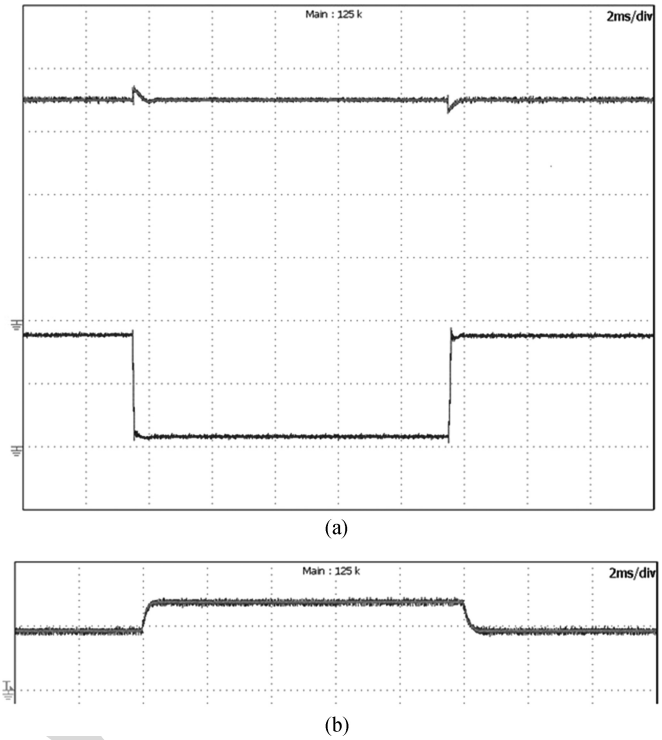


Fig. 12. Load transient response of the enhanced control configuration ($k_o = V_{\rm ref}/V_i$): (a) output voltage (red, 10 V/div, 2 ms/div) and current (blue, 1 A/div), and (b) signal *u* (2 V/div, 2 ms/div).

Fig. 12(a) shows the transient response of the output voltage during load changes using the enhanced control. As predicted by Fig. 7(c) and Table IV, the transient response is drastically improved. In fact, the voltage overshoots and setting times are clearly reduced from 5 to 1 V and from 1.8 to 0.4 ms, respectively. These enhancements are the consequence of the transient response improvement in the input signal of the modulator (u), as depicted in Fig. 12(b). It means that in the case of load-step changes, the feed-forward term helps the modulator to rapidly find an appropriate switching frequency to ensure a fixed-output voltage.

The load transient response is also evaluated for different values of the input voltage. Fig. 13 shows the results for $V_i = 10$ V and Fig. 14 for $V_i = 14$ V. Note that the voltage deviations during load changes reduce as the input voltage increases (i.e., when the gain of the converter reduces).

In any case, the most important issue is that the dynamic behavior of the enhanced control is still superior than the performance of the basic control for any value of the input voltage; compare Figs. 11–14. In particular, the transient response is faster with lower voltage deviations and settling times (benefit of the enhanced control), as expected from the theoretical analysis.

However, the drawback associated to the enhanced control is the additional measurement (i_o) required to implement the feed-forward term, increasing the overall cost of the system. Therefore, regarding the desired performance and cost, one of the two proposed control configurations should be applied to the converter.

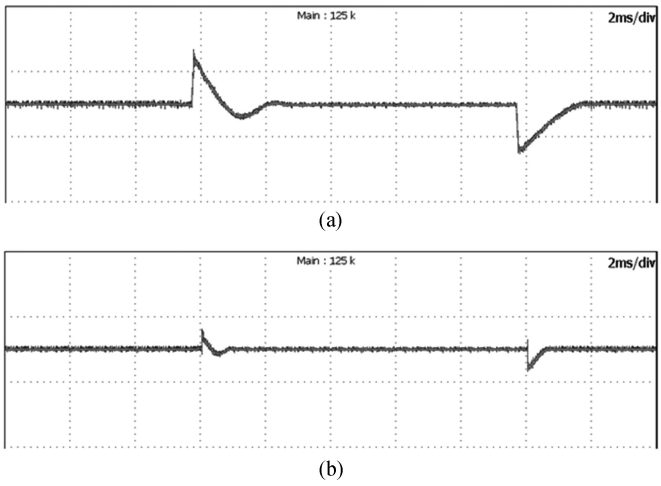


Fig. 13. Load transient response for $V_i = 10\,\text{V}$ and $V_{\text{ref}} = 35\,\text{V}$. (a) Basic control configuration ($k_o = 0$). (b) Enhanced control configuration ($k_o = V_{\text{ref}}/V_i$). 10 V/div, 2 ms/div.

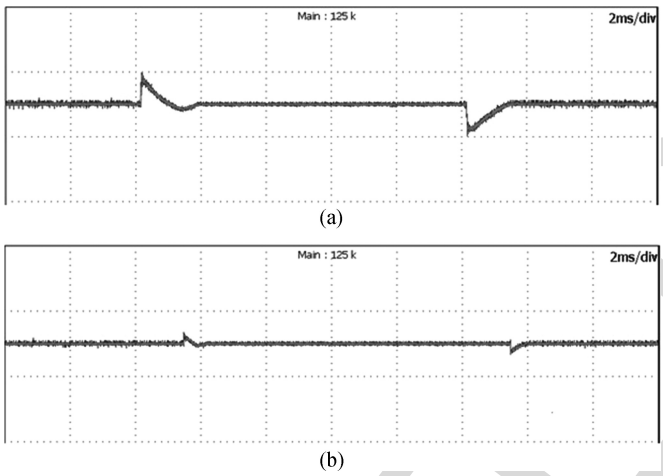


Fig. 14. Load transient response for $V_i = 14\,\text{V}$ and $V_{\text{ref}} = 35\,\text{V}$. (a) Basic control configuration ($k_o = 0$). (b) Enhanced control configuration ($k_o = V_{\text{ref}}/V_i$). 10 V/div, 2 ms/div.

VI. Conclusion

A frequency-modulation control scheme for the class-D CSPRC was proposed in this paper. This control has two possible configurations (basic and enhanced), according to the use or no use of the output-inductor current feed-forward term. The study reveals the superior performance of the enhanced control configuration in terms of fast transient response during load step changes, i.e lower voltage deviations and settling times. The price to pay for this was an increase of cost due to the measure of an extra current. A theoretical study conducting to the design of both control configurations was also proposed in this paper. The study starts with the derivation of proper dynamic models for the converter and the complete closed-loop system. Next, a control design procedure was presented including a design example for illustrative purposes.

The basic and enhanced control configurations can be applied to other current-source parallel resonant topologies including half bridge, full bridge, and other configurations by slightly modifying the logic circuit of the modulator. The proposed control configurations were promising closed-loop control systems to be employed in switching power supplies. The extension to other applications was left for future research work.

Appendix

This Appendix shows the coefficients of the transfer functions expressed in (34) and (35)

$$A_1 = V_c + I_i\ M\ R \tag{A1}$$
$$A_2 = C\ L_o V_c + C_o\ I_i\ L_o M\ R \tag{A2}$$
$$A_3 = I_i\ L_o\ M + C\ R\ V_c + C_o\ R\ V_c \tag{A3}$$
$$A_4 = V_c + I_i\ M\ R \tag{A4}$$
$$B_1 = C\ C_o\ L_i\ L_o\ R \tag{A5}$$
$$B_2 = C\ L_i\ L_o \tag{A6}$$
$$B_3 = C\ L_i\ R + C_o\ L_i\ R + C_o\ L_o\ M^2\ R \tag{A7}$$
$$B_4 = L_i + L_o\ M^2 \tag{A8}$$
$$B_5 = M^2\ R \tag{A9}$$
$$C_1 = I_i\ M\ R\ L_i \tag{A10}$$
$$C_2 = -R\ M\ V_c. \tag{A11}$$

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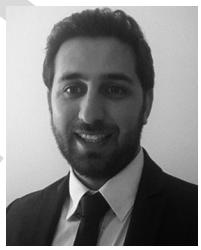

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Queries

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