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Generalized PWM-Based Method for Multiphase Neutral-Point-Clamped Converters with Capacitor Voltage Balance Capability

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Abstract

This paper presents a generalized PWM-based control algorithm for multiphase neutral-point-clamped (NPC) converters. The proposed algorithm provides a zero-sequence to be added to the reference voltages that contributes to improve the performance of the converter by: *i*) regulating the neutral-point (NP) current to eliminate/attenuate the low-frequency NP voltage ripples, *ii*) reducing the switching losses of the power semiconductors and *iii*) maximizing the range of modulation indices for linear operation mode. The control method is formulated following a carrier-based PWM approach. Hence, dealing with complex space-vector diagrams to solve the modulation problem for multiphase converters is avoided. The recursive approach means that it can be easily extended to *n*-phase converters without increasing the complexity and computational burden, making it especially attractive for digital implementation. The proposed method allows regulating the NP voltage without the need for external controllers; therefore, no parameter tuning is required. The algorithm has been tested in a four-leg NPC converter prototype performing as a three- and four-phase system and operating with balanced and unbalanced loads.

Index Terms

Carrier-based pulse-width modulation, multiphase multilevel converter, neutral-point-clamped converter, capacitor voltage balance.

I. Introduction

The recent developments in power electronics and control systems have increased practical interest on multiphase machines. These machines present several advantages with regard to their three-phase counterparts [1]–[3], such as:

- Fault tolerance and improved reliability: Multiphase machines can operate with several faulty phases, as long as there are at least three healthy phases.
- Increased efficiency: The stator excitation in a multiphase machine produces a field with lower harmonic content and less losses [1]–[3].
- Lower power handling requirements per phase. Consequently, power semicondutors with lower rated current can be used without the need to include additional hardware to balance the current among the devices [3].

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These advantages have positioned multiphase machines as a good alternative in applications including ship propulsion [4]–[6], wind turbines [7]–[9], electric traction (including electric and hybrid vehicles) [10], [11], multiphase active filters [12] and aerospace industry [13], [14]. In [15], a comprehensive review of this technology is presented.

At the same time, multilevel conversion is nowadays an industrially accepted technology for medium- and high-voltage applications [16]–[22]. Several multilevel converter topologies have been developed in the last three decades. Detailed comparisons between these topologies in terms of structure, modularity, losses and power quality are performed in [16], [21], [23], [24]. The three-level neutral-point-clamped (NPC) converter [25] is the most commonly used due to, among other characteristics, its simple structure and reduced number of capacitors.

Several modulation algorithms for multilevel multiphase drives have been proposed in the technical literature. Some of them address the modulation problem following a space-vector PWM (SVPWM) approach [26]–[30]. When the converter has more than three phases, the number of vectors increases exponentially, according to the rule l^n (where l is the number of converter levels, and n is the number of phases). In addition, the space-vector diagram changes from a 2-D plane for three-phase converters, to a (n-1)-D vector diagram for converters with more than three phases [26]. Consequently, an increase in the number of phases implies dealing with a high number of switching vectors and sophisticated vector diagrams. This complicates the implementation of SVPWM algorithms for multilevel multiphase converters and increases the calculation requirements of digital controllers.

Several alternatives have been introduced to simplify the implementation of multiphase SVPWM algorithms. In [27], a space-vector strategy for a three-level five-phase converter is proposed, where a decomposition of the variables into 2-D orthogonal planes is conducted. In [28], a similar methodology is reported for a three-level seven-phase NPC converter. SVPWM formulation is also used in [29] and [30], where a methodology to solve the multiphase modulation problem is derived using a two-level approach. This approach uses a matrix formulation to calculate the duty cycles. The computation time required to solve the problem is not significantly affected by the number of levels of the converter, but the matrix size increases with the number of phases and therefore the complexity and processing time required for the modulation algorithm increase as well.

Carrier-based PWM (CBPWM) methods for multilevel converters have also been widely reported in the technical literature [31]–[34]. These modulation approaches are well-stablished for three-phase systems and, unlike the SVPWM approach, their implementation complexity does not increase with the number of phases.

The comparison of SVM and CBPWM for three-level, multiphase systems presented in [35] demonstrates that CBPWM techniques are less complex, easier to expand to converters with multiple phases and require less computing time than SVPWM. Consequently, they are better suited to operate multiphase converters.

However, none of the CBPWM methods for multiphase converters described in [35] includes NP voltage balancing control. This feature is crucial for NPC converters [36], [37], especially when they operate as active filters or connected to unbalanced electrical systems [38]. Multiple control methods to regulate the NP voltage in three-phase NPC converters following a CBPWM approach have been proposed in the technical literature. These methods can be classified into three categories. Firstly, there are those methods that use an external linear or nonlinear controller to determine the zero-sequence voltage used to balance the NP voltage [31]. Secondly, there are those methods in which the zero-sequence voltage calculation is embedded into the modulation method [34]. In particular [34] establishes a correlation between SVPWM and CBPWM, and based on that correlation, a method to directly determine the zero-sequence voltage injection is proposed. Thirdly, there are those methods where some phases of the converter are forced to commutate between multiple voltage levels in each modulation period to achieve NP voltage balance [39]–[41]. These methods are able to completely cancel the low-frequency NP voltage oscillations; however, this is achieved at the cost of decreasing the efficiency of the converter and the quality of the output voltage waveforms.

Despite the great number of publications addresing NP voltage balance in three-phase NPC converters little attention has been paid to their multiphase counteparts. Some of the modulation methods initially presented for three-phase systems, as for instance that introduced in [31], can also be used with multiphase NPC converters. However, it ususally implies dealing with external controllers that it is necessary to tune to balance the NP voltage. In addition, the dynamics of these methods are usually slow and they are barely able to reduce the amplitude of the low-frequency NP voltage oscillations. A few specific CBPWM methods for multiphase NPC converters have also been developed recently [42]–[44]. These methods are able to cancel completely the low-frequency NP voltage oscillations and regulate the NP voltage in multiphase NPC converters but they increase the power losses of the converter and degrade the quality of the output voltages.

In this paper, a new method to calculate the zero-sequence that can regulate the NP voltage, eliminate or attenuate the low-frequency NP voltage oscillations and reduce the switching losses of the power semiconductors in multiphase NPC converters (Fig. 1) is introduced. The main contribution of the proposed algorithm with regard to existing methods in the technical literature is the generalised formulation that makes it applicable to NPC converters with any number of phases. It enhances the existing CBPWM methods by:

- Providing a recursive, generalised formulation that makes it expandable to n-phase converters,
- Being completely based on a CBPWM approach and, unlike [34], it does not need to establish a duality between the SVPWM and CBPWM to solve the modulation problem. Hence, it is not necessary to deal with sophisticated vector diagrams with many vectors when the number of phases increases.
- Controlling the NP voltage autonomously using a closed-loop algorithm embedded in the modulation method.
- Not requiring the use of external linear or nonlinear controllers used in other modulation algorithms to balance the NP voltage, thus making the NP voltage control simpler.
- Reducing the switching power losses.

This paper is an extension of the work presented in [45]. The control method is improved at low modulation indices, and extended NP voltage analysis, power quality studies and power losses evaluations are provided. The paper also includes new experimental results and further discussions.

The paper is organized as follows. The basis of the control algorithm is analyzed in Section II. Section III presents experimental results for three- and four-phase NPC converters under balanced and unbalanced loading conditions. Section IV benchmarks the performance of the proposed algorithm against other modulation methods in terms of voltage balancing capability, efficiency and power quality. It also shows the operation of the proposed algorithm when applied to closed-loop drives. Finally, Section V concludes the paper.

II. Fundamentals of the Proposed Control Method

The proposed control method uses a CBPWM approach where each phase is controlled by means of a modulation signal. A zero-sequence voltage is injected aiming to: (*i*) minimize the switching losses, (*ii*) control the current flowing through the NP to regulate the NP voltage, and (*iii*) extend the linear modulation region. To fulfill the first requirement, the number of switching events has to be kept as low as possible. This is achieved maintaining one of the converter phases continuously clamped during each switching period. There are several zero-sequence voltage combinations that clamp one phase of the converter to a fixed level.

When the modulation index is high, i.e. v_{max}-v_{min} is larger than one, where v_{max} and v_{min} are the maximum and minimum normalized reference voltages ranging in the interval [-1,1], respectively, there are at least two zero-sequence voltage sets that clamp one of the converter phases. One of them clamps the phase with the highest output voltage reference to the positive rail of the *dc*-bus. The required zero-sequence voltage to clamp this phase is calculated as:

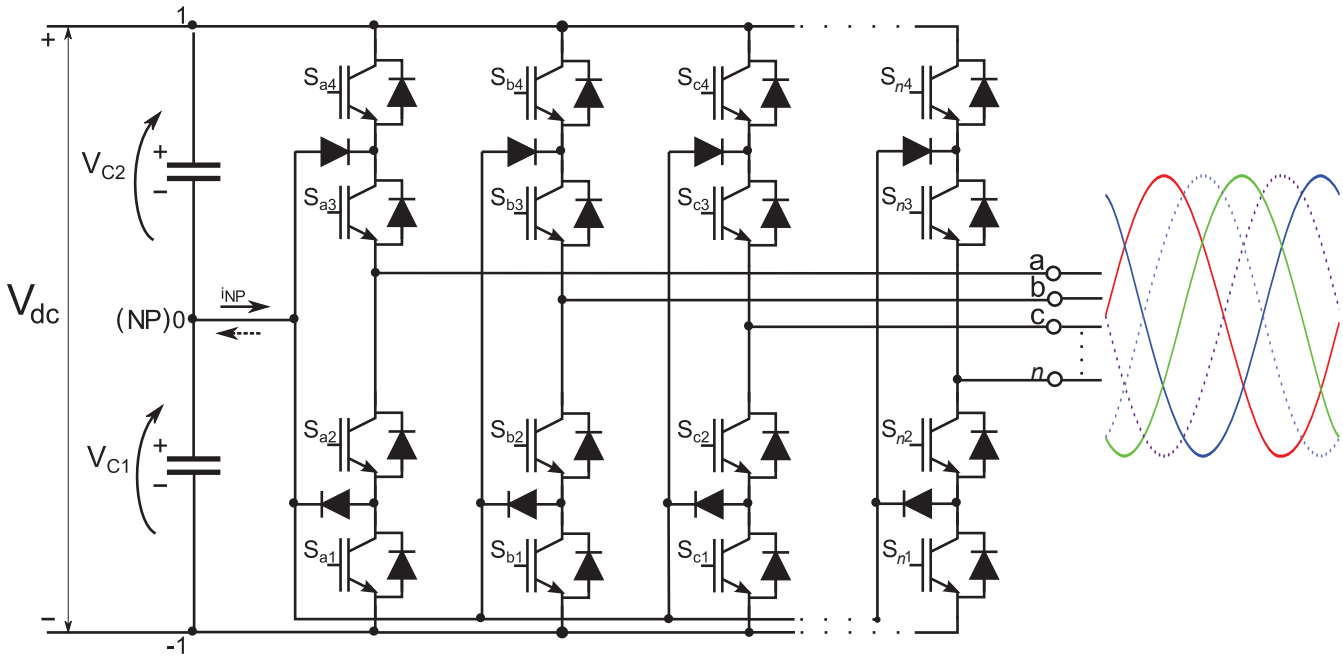


Fig. 1. n-phase three-level NPC converter.

$$v_{off_{max}} = 1 - v_{max}. \tag{1}$$

Alternatively, it is also possible to clamp the phase with the lowest output voltage reference to the negative *dc*-bus rail. The required zero-sequence voltage is calculated as follows:

$$v_{off_{min}} = -1 - v_{min}. \tag{2}$$

In addition, depending on the operating point, some of the remaining phases may be connected to the NP *dc*-bus rail, provided that the saturation limit of the PWM is not exceeded. The offset required to clamp one of the remaining output phases to the NP dc rail is given by:

$$v_{off_{med}} = -v_i, \tag{3}$$

where v_i represents the reference signals of those phases that are not generating the maximum nor the minimum output voltages.

Expressions (1) and (2) are also applicable when the converter is working in the low modulation index region. However, when the modulation index is low, i.e. $v_{max} - v_{min} < 1$, the zero-sequence voltage of (1) and (2) produce unnecessary switching events that increase the switching losses.

A better solution that also provides NP voltage controllability, but reduces the number of switching transitions, is found if the zero-sequence voltage given by (3) is applied to all the phases, including those that generate the maximum and minimum output voltages. This is equivalent to saying that any phase can be clamped to the NP *dc*-bus rail. Obviously, this can only be applied if the modulation index is low.

The effect of the zero-sequence voltage on the locally-averaged current that flows through the NP ($\bar{i}_{NP}$) during a switching period can be assessed by:

$$\bar{i}_{NP} = (1 - |v'_a|)i_a + (1 - |v'_b|)i_b + ... + (1 - |v'_n|)i_n, \tag{4}$$

where i_a, i_b, i_c, ..., i_n are the output currents of an n-phase converter, and v'_a, v'_b, v'_c, ..., v'_n are the normalized output voltages with the addition of the corresponding zero-sequence voltage, i.e.:

$$v'_i = v_i + v_{off}, \tag{5}$$

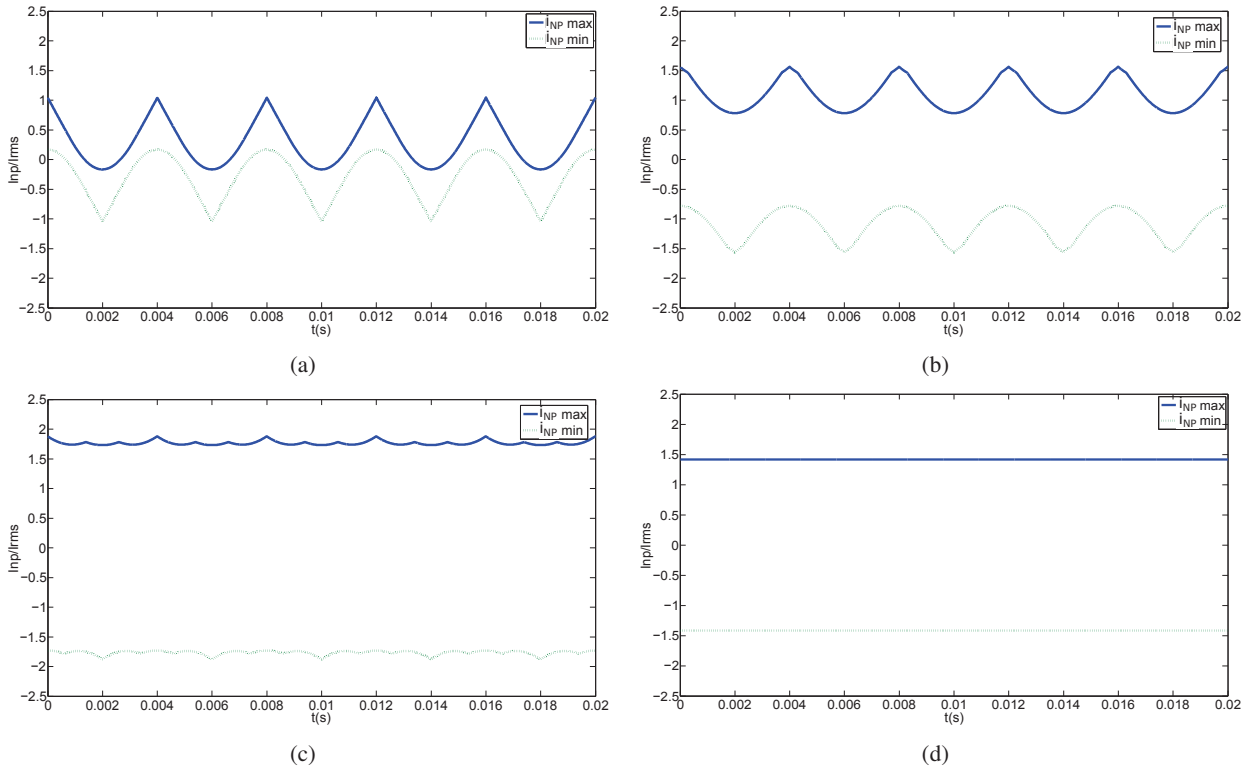


Fig. 2. Normalized maximum and minimum NP current waveforms obtained when the power factor is 1: (a) *m*=1, (b) *m*=0.8, (c) *m*=0.6 and (d) *m*=0.4.

for *i*={*a*, *b*,..., *n*}, and v_{off} being the zero-sequence voltages given by (1)-(3).

For the sake of simplicity, the locally-average notation in $\bar{i}_{NP}$ will be eliminated and presented as i_{NP} henceforth. According to (4), it is possible to modulate the NP current selecting the appropiate zero-sequence voltage. To illustrate the effect of the zero-sequence voltage on the NP current Fig. 2 is provided. It shows the maximum and minimum values of the NP current that can be achieved by selecting the appropiate zero-sequence voltage for different modulation indexes. Results in Fig. 2 are obtained for a five-phase NPC converter working at unit power factor, but similar results can be obtained for converters with different number of phases and different working conditions. The values in Fig. 2 are normalized against the RMS value of the output current. It can be observed that the maximum NP current takes mostly positive values while the minimum takes negative values. The proposed algorithm takes advantage of this degree of freedom and selects the most suitable NP current to balance the NP voltage. This is accomplished by selecting, among all the feasible zero-sequence voltage options given by (1)-(3), the one that minimizes (6).

$$E = \mid i_{NP} - i^*_{NP} \mid \tag{6}$$

where E represents the error between the NP current given by (4) and the required NP current i^*_{NP} to regulate the NP voltage to $\frac{V_{dc}}{2}$. i^*_{NP} is calculated using (7).

$$i^*_{NP} = \frac{\triangle v_{NP}}{T_s} 2C, \tag{7}$$

being C the *dc*-bus capacitor and T_s the switching period.

In those time intervals where the maximum and minimum currents take positive and negative values respectively, it is possible to make (6) very close to zero by selecting the appropiate zero-sequence voltage. Consequently, the NP voltage is perfectly balanced. However, there are some operating conditions where

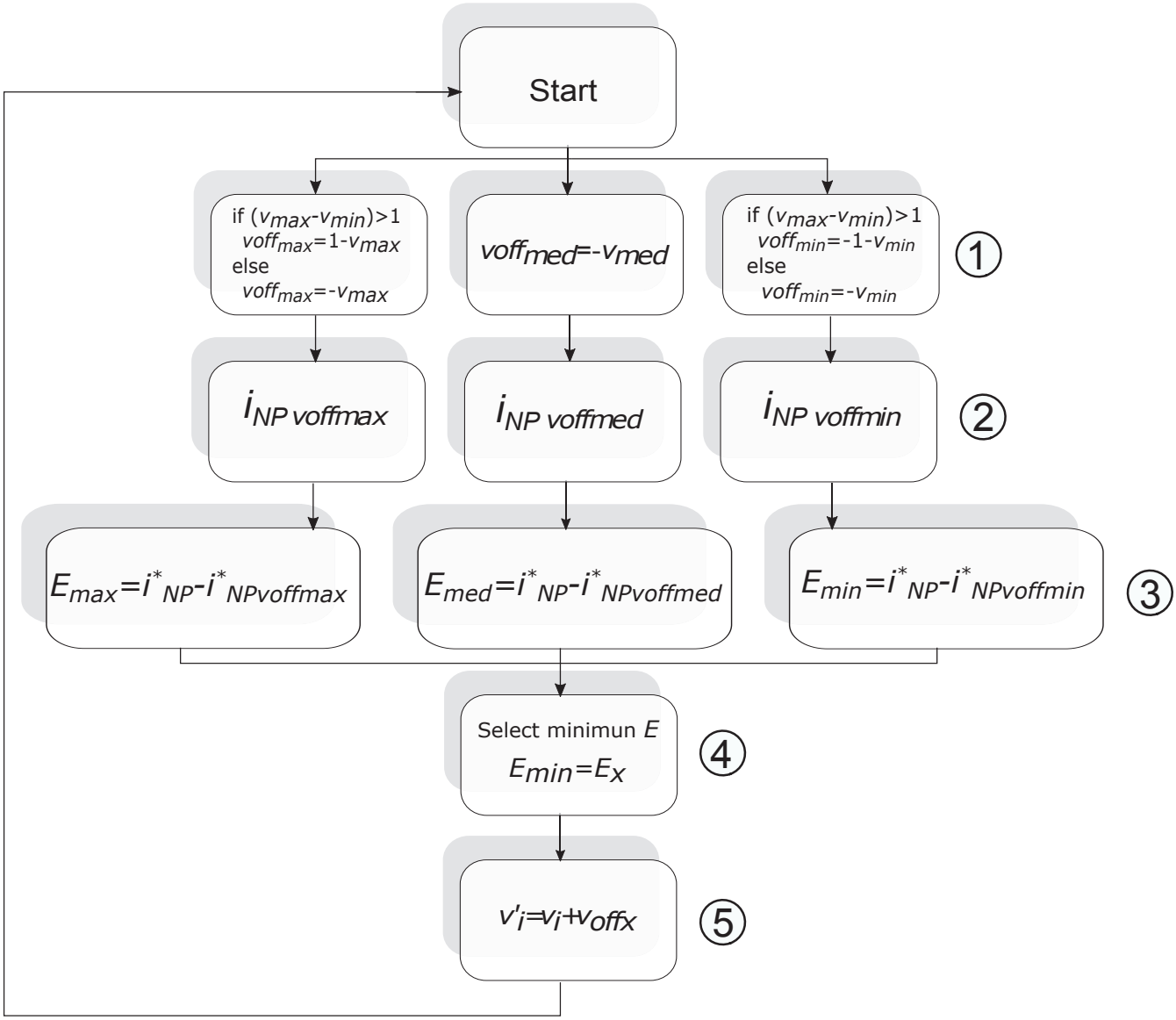


Fig. 3. Modulation method flowchart for a n-phase three-level NPC converter.

the maximum and minimum currents take simultaneouly positive or negative values during some time intervals (see Fig. 2(a)). In this case, it is not possible to make (6) equal to zero and the algorithm losses its capacity to regulate the NP voltage. Nevertheless, it is still able to select the zero-sequence voltage that minimizes (6) producing the least harmful NP current. Therefore, the NP voltage oscillates but the amplitude of the oscillations is reduced.

Once the selection of the most suitable zero-sequence voltage is made, (5) is applied to calculate the modulation signals. These modulation signals are used as inputs in a PWM modulator. Fig. 3 shows a flowchart that summarizes the main steps of the proposed control algorithm.

III. Experimental Results

To validate the proposed method a set of experimental tests have been conducted in the four-phase NPC prototype shown in Fig 4. The parameters of the test-platform are summarized in Table I. The control algorithm is tested with the platform configured as a three- or four-phase NPC converter under balanced

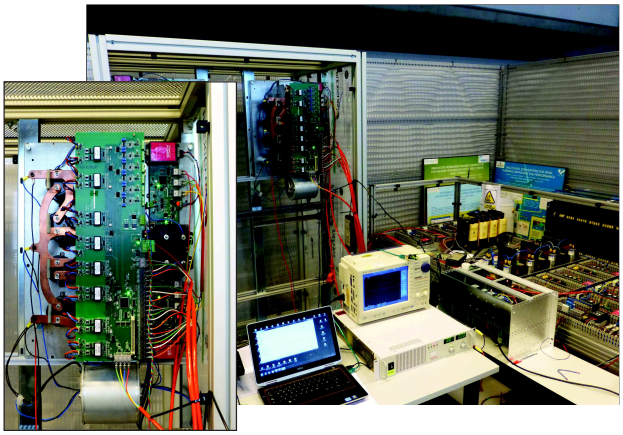


Fig. 4. Experimental platform.

Table I
SYSTEM FEATURES

Three-Level Multiphase NPC Converter	
Rated power (kW)	20
Output rated voltage (V_{rms})	400
dc-link capacitors (mF)	1.1
dc-bus maximum voltage (V)	700
Switching frequency (kHz)	2.5

and unbalanced load conditions and under a large NP voltage imbalance. The fundamental frequency of the output voltages has been set to 20 Hz, low enough to emphasize the amplitude of the low-frequency NP voltage ripples. The *dc*-bus voltage used in the tests is 300V unless otherwise noted.

A. Three-Level Three-Phase NPC Converter

1) Balanced Load Conditions: Fig. 5 shows the line-to-line output voltage (v_{ab}), dc-link capacitor voltages (v_{C1} and v_{C2}), and the ac output currents obtained for different modulation indices (m=1, m=0.6 and m=0.4) operating with the proposed control method. These results are obtained with a three-phase balanced star-connected R-L load (R=5 Ω, L=10 mH).

Fig. 6 shows equivalent results when the standard CBPWM technique with a zero-sequence voltage injection according to the min-max principle is used. For the sake of simplicity, this modulation technique will be referred as standard CBPWM henceforth.

One can observe the ability of the proposed algorithm to regulate the NP voltage and to cancel the low-frequency NP voltage ripples for some modulation indices. However, the proposed algorithm causes some undesirable voltage spikes in the voltage waveforms, which can be appreciated in Figs. 5(b) and 5(c). These spikes are caused by the dead times of the transistors during certain additional commutations that take place at the beginning of certain switching periods as a consequence of the added zero-sequence voltage. These extra commutations are not produced with standard CBPWM. Consequently, the proposed algorithm produces higher harmonic distortion in the voltage and current waveforms at high frequencies. Nevertheless, as it is high frequency distortion, it can be easily filtered, leading to the sinusoidal current waveforms of Fig. 5 with very low harmonic distortion.

2) Unbalanced Load Conditions: Fig. 7 shows the results obtained when the proposed algorithm is applied to a three-phase NPC converter connected to an unbalanced R-L load ($R_{a,b}$=5 Ω, $L_{a,b}$=10 mH, and

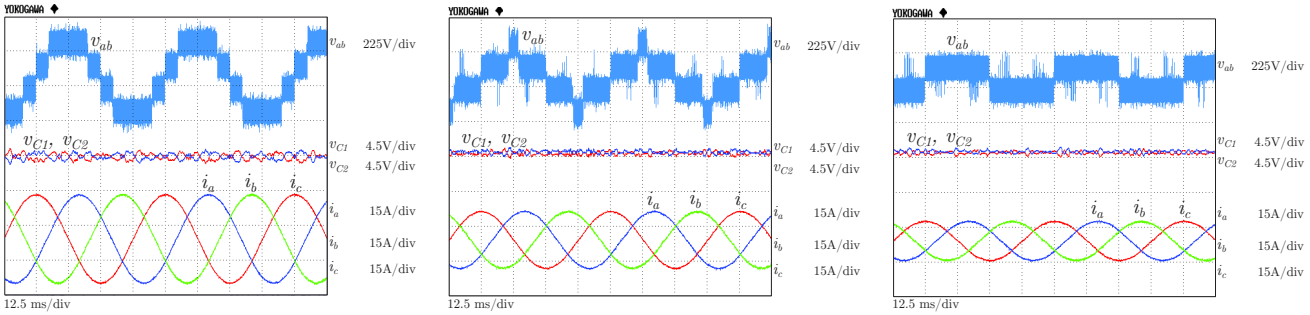


Fig. 5. Three-level three-phase NPC converter with the proposed control algorithm and $v_{dc} = 300V$: (a) m=1, (b) m=0.6, and (c) m=0.4.

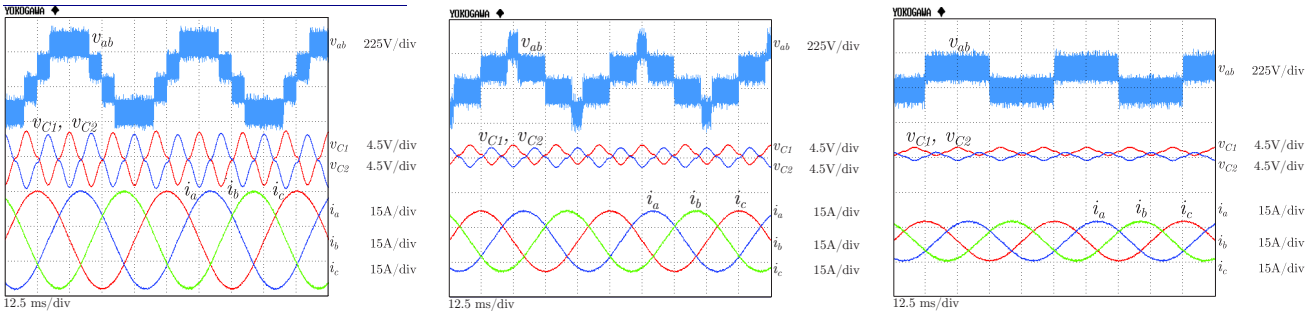


Fig. 6. Three-level three-phase NPC converter with standard CBPWM and $v_{dc} = 300V$: (a) m=1, (b) m=0.6, and (c) m=0.4.

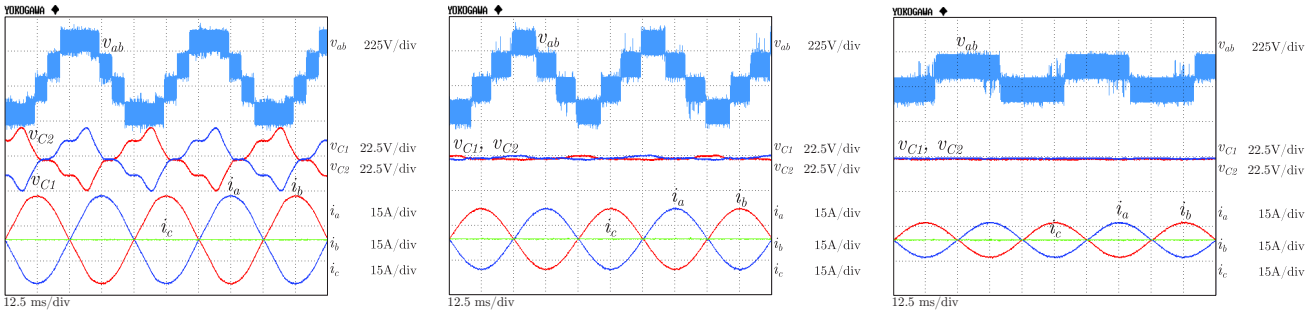


Fig. 7. Three-level three-phase NPC converter with the proposed algorithm operating with an asymmetrical load and $v_{dc} = 300V$: (a) m=1, (b) m=0.7, and (c) m=0.4.

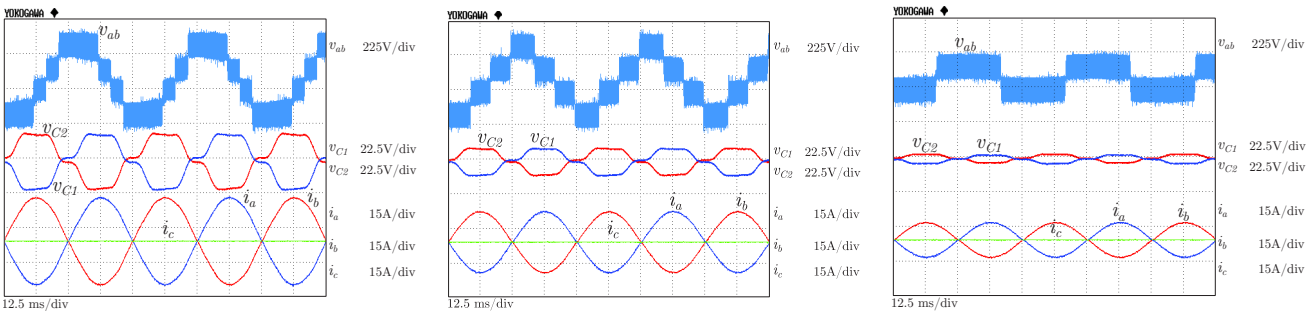


Fig. 8. Three-level three-phase NPC converter with standard CBPWM operating with an asymmetrical load and $v_{dc} = 300V$: (a) m=1, (b) m=0.7, and (c) m=0.4.

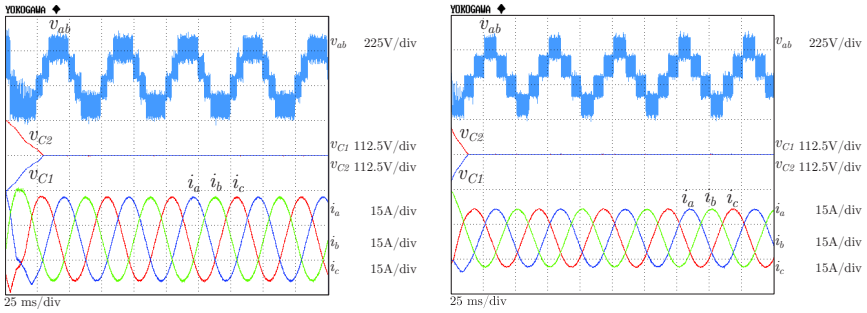


Fig. 9. Three-level three-phase NPC converter with *dc*-bus imbalance applying the proposed algorithm with $v_{dc} = 250V$: (a) *m*=1 and (b) *m*=0.7.

phase c is left open). Fig. 8 shows equivalent results when standard CBPWM is applied. These figures illustrate the line-to-line voltage (v_{ab}), *dc*-bus capacitor voltages (v_{C1} and v_{C2}) and the output currents for m=1, m=0.7 and m=0.4.

The amplitudes of the low-frequency NP voltage ripples increase when the converter is connected to an unbalanced load with both modulation methods. When the modulation index is *m*=1, the proposed algorithm exhibits similar voltage ripples than the standard CBPWM. This is caused by the intrinsic lack of NP voltage controllability of the NPC converters at high modulation indices and by the bang-bang behavior of the proposed method. However, when the modulation index is slightly lower than 1, the proposed algorithm has the capacity to reduce drastically the low-frequency NP voltage ripples. This is shown in Fig. 7(b) operating with a modulation index *m*=0.7, where the low-frequency NP voltage ripples are practically eliminated with the proposed control method.

3) Unbalanced NP Voltage: In this test, the *dc*-bus capacitors are forced to have an initial voltage imbalance. The upper capacitor voltage v_{C2} is forced to 250 V (the total *dc*-bus voltage), while the lower capacitor voltage v_{C1} is forced to 0 V.

Fig. 9 shows the dynamic of the capacitor voltages under the above circumstances for m=1 and m=0.7 when the proposed method is applied. The figures show how the voltage of the *dc*-bus capacitors (v_{C1} and v_{C2}) evolve towards the reference value (v_{dc}/2=125 V) eliminating the initial imbalance completely. As it can be observed, the lower the modulation index, the faster the balancing dynamic. The reason for this is the better degree of controllability of the NP current that the proposed method exhibits with low modulation indices. These results demonstrate the capacity of the proposed method to balance the NP voltage. Standard CBPWM has also the ability to naturally balance the NP voltage. However, the dynamic response achieved with the proposed method is improved considerably. For most usual operating conditions, involving high modulation indexes and high power factors, the time required to balance the NP voltage when the proposed method is used is about four times lower than the time required by the standard CBPWM.

B. Three-Level Four-Phase NPC Converter

This section validates the proposed algorithm for multiphase NPC converters. Ideally, it would have been interesting to test the algorithm with a five-phase converter since it has a marked practical interest. However, due to the non-availability of a five-phase converter in our laboratory, we have used a four-phase converter.

1) Unbalanced Load Conditions: Due to the inherent symmetry of a balanced four-phase electrical system, no low-frequency NP voltage ripples are present in a four-phase NPC converter connected to a balanced load. However, this does not happen if the four-phase system is unbalanced. Fig. 10 and 11 show the performance of the proposed control method and standard CBPWM, respectively, for *m*=1, *m*=0.7 and *m*=0.4. The four-phase NPC converter is connected to an unbalanced R-L load (R_a=10 Ω, $R_{b,c}$=5 Ω, L_a=

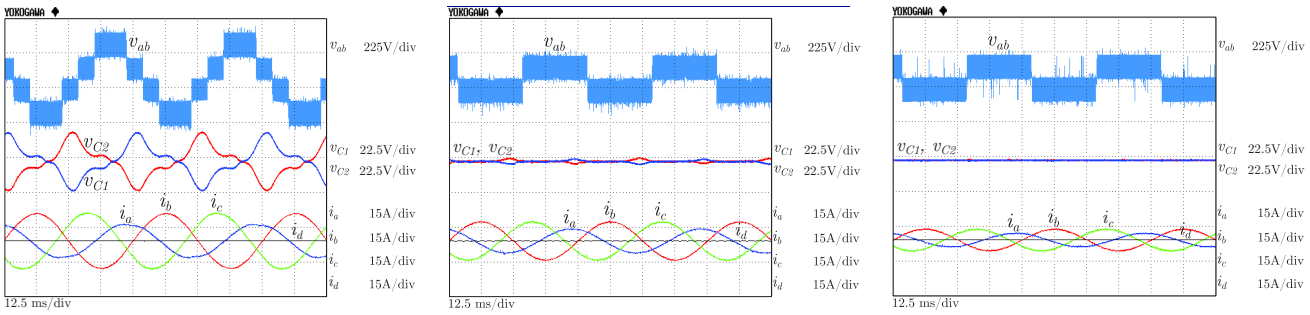


Fig. 10. Three-level four-phase NPC converter applying the proposed algorithm with an asymmetrical load and $v_{dc} = 300V$: (a) m=1, (b) m=0.7, and (c) m=0.4.

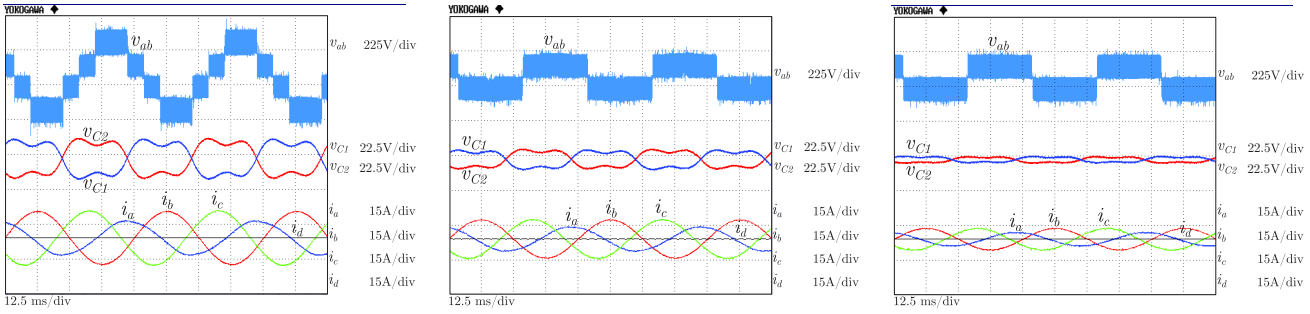


Fig. 11. Three-level four-phase NPC converter applying standard CBPWM with an asymmetrical load and $v_{dc} = 300V$: (a) m=1, (b) m=0.7, and (c) m=0.4.

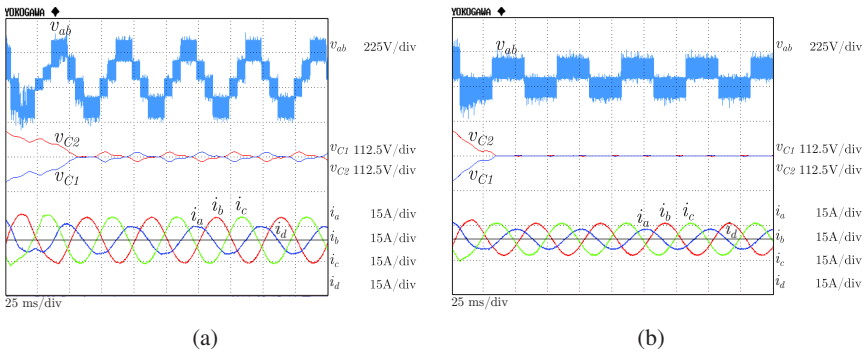


Fig. 12. Three-level four-phase NPC converter with *dc*-bus imbalance applying the proposed algorithm with $v_{dc} = 250V$: (a) m=1 and (b) m=0.7.

5 mH, $L_{b,c}$=10 mH and phase *d* is left open). The four reference voltage signals have a phase difference of 90 degrees. These results show once again the ability of the proposed method to reduce the amplitudes of the low-frequency NP voltage ripples when the modulation index is below 1.

2) Unbalanced NP Voltage: Fig. 12 shows the results when an initial imbalance is forced in the dc-link capacitor voltages. The upper capacitor voltage v_{C2} is forced to 250 V (the total *dc*-bus voltage), while the lower capacitor voltage v_{C1} is forced to 0 V. In addition, the four-phase NPC converter is connected to the same unbalanced R-L load used in the previous experiment. Even under these extreme operating conditions, the proposed control algorithm is able to compensate the initial voltage imbalance in a fast and accurate way.

IV. Additional Considerations

This section makes some additional considerations on the proposed algorithm regarding its capability to attenuate the low-frequency NP voltage ripples and also to achieve higher converter efficiency. In addition, power quality analysis is also carried out and proper performance of the proposed algorithm under closed-loop operating conditions is demonstrated.

A. NP Voltage Ripples

The previous experimental results demonstrate the capability of the proposed algorithm to attenuate or even eliminate the NP voltage ripples for some specific operating conditions. To extend this study, the amplitude of the voltage ripple for any operating condition of the converter has been determined using MATLAB/Simulink. Figs. 13(a) to 13(d) show the normalized amplitude of the low-frequency NP voltage ripples for all modulation indices and power factors of a three-phase NPC converter operating under a balanced load for different modulation methods.

The normalized NP voltage amplitude is defined as [36]:

$$\frac{\Delta V_{NPn}}{2} = \frac{\Delta V_{NP}/2}{I_{RMS}/fC} \tag{8}$$

where I_{RMS} is the RMS (root mean square) value of the output currents, f is the output frequency, C is the value of the dc-link capacitors and ΔV_{NPn} the peak-to-peak value of the low-frequency voltage ripples.

These figures are used to benchmark the NP voltage regulation capacity of the proposed algorithm (Fig. 13(a)) against the CBPWM with zero sequence voltage injection according to the max-min principle (Fig. 13(b)) and two modern modulation methods for NPC converters introduced in [34] (Fig. 13(c)) and [44] (Fig. 13(d)).

The modulation methods shown in Figs. 13(a) to 13(c) exhibit the largest amplitude of the NP voltage ripple when the modulation index is the maximum and the converter is operating with a power factor close to zero. Under these circumstances the three of them have similar low-frequency NP voltage ripples. However, when the modulation index is not the maximum, the proposed algorithm and the one introduced in [34] exhibit better NP current regulation capacity than the CBPWM. Hence, the NP voltage ripples are reduced accordingly.

The main difference between the proposed algorithm and the modulation presented in [34] is observed at low modulation indices and power factors. Under these conditions, the proposed method offers an improved performance with better NP voltage regulation capability. Fig. 13(d) shows the normalized NP voltage amplitude for the modulation method introduced in [44]. This modulation is able to cancel the NP voltage ripple for any working condition. Therefore, the surface displayed in Fig. 13(d) is equal to zero. In this sense, the modulation presented in [44] achieves optimal capacitor voltage balance for all the operating conditions, which cannot be achieved with the proposed modulation. However, as it is demonstrated in the following sections, the superior NP voltage regulation capability of [44] is achieved at the cost of degrading the efficiency of the converter and the power quality. In this sense, the proposed algorithm offers an optimum compromise between NP voltage regulation capability, power quality and efficiency.

Fig. 14 shows the normalized amplitude of the low-frequency NP voltage ripples in a five-phase converter with the proposed method. A significant reduction in the capacitor voltage ripples in the five-phase NPC converter compared with the three-phase one can be observed. The maximum ripple is reduced by a factor of three. The reason for this is that the proposed control method offers better utilization of the phases for NP voltage control.

The higher the number of phases, the more choices the control method has to compute the most suitable zero-sequence voltage to balance the NP voltage. Consequently, the amplitude of the low-frequency NP voltage ripples are reduced.

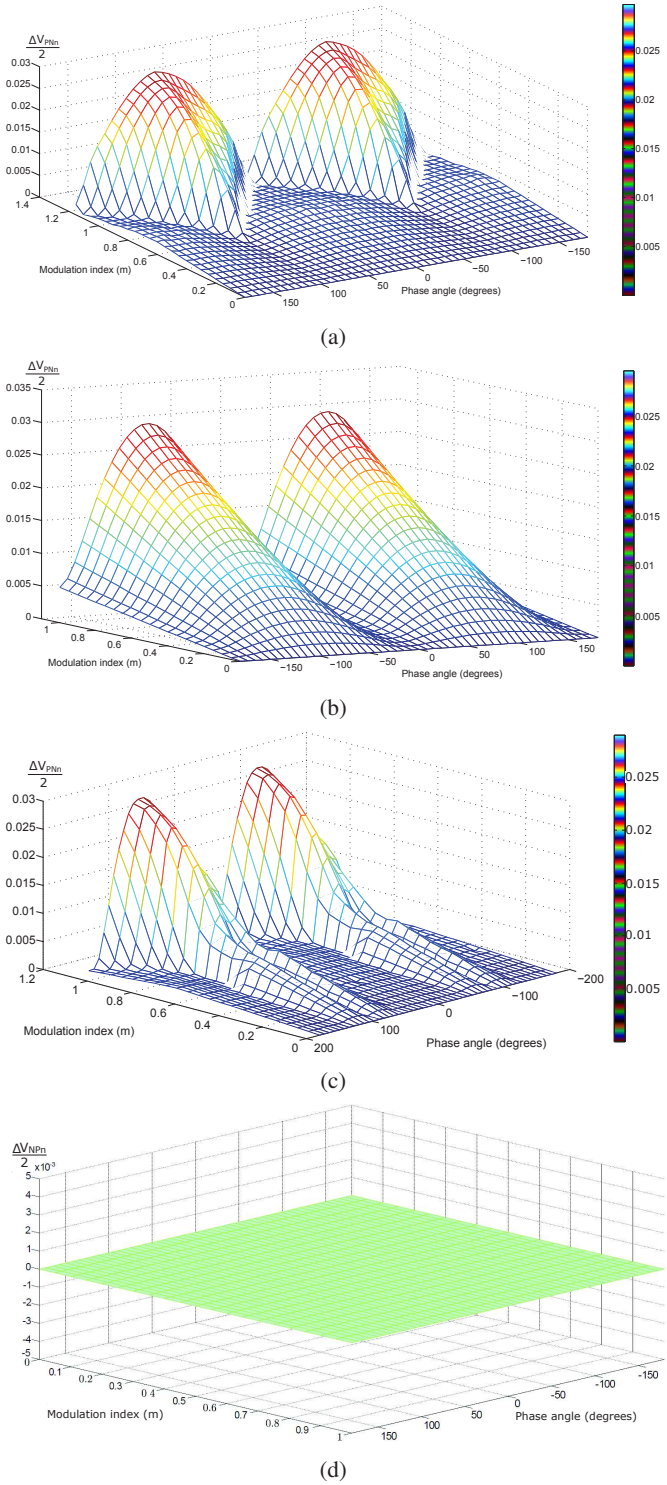


Fig. 13. Normalized amplitude of the low-frequency NP voltage ripples of a three-phase NPC converter with: (a) proposed algorithm; (b) CBPWM; (c) algorithm introduced in [34], and (d) algorithm introduced in [44].

B. Efficiency Analysis

This section benchmarks the efficiency of the proposed method against the standard CBPWM. considering the insulated-gate bipolar transistor (IGBT) DIM1200NSM17-E000 for the calculations. This IGBT has a collector-emitter voltage of 1700 V and a continuous collector current of 1200 A. The IGBT losses

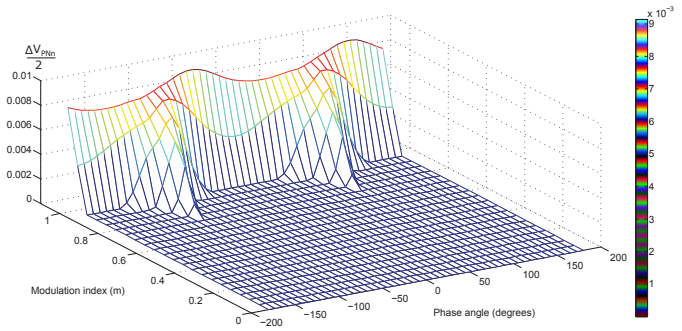


Fig. 14. Normalized amplitude of the low-frequency NP voltage ripples of a five-phase NPC converter with the proposed modulation.

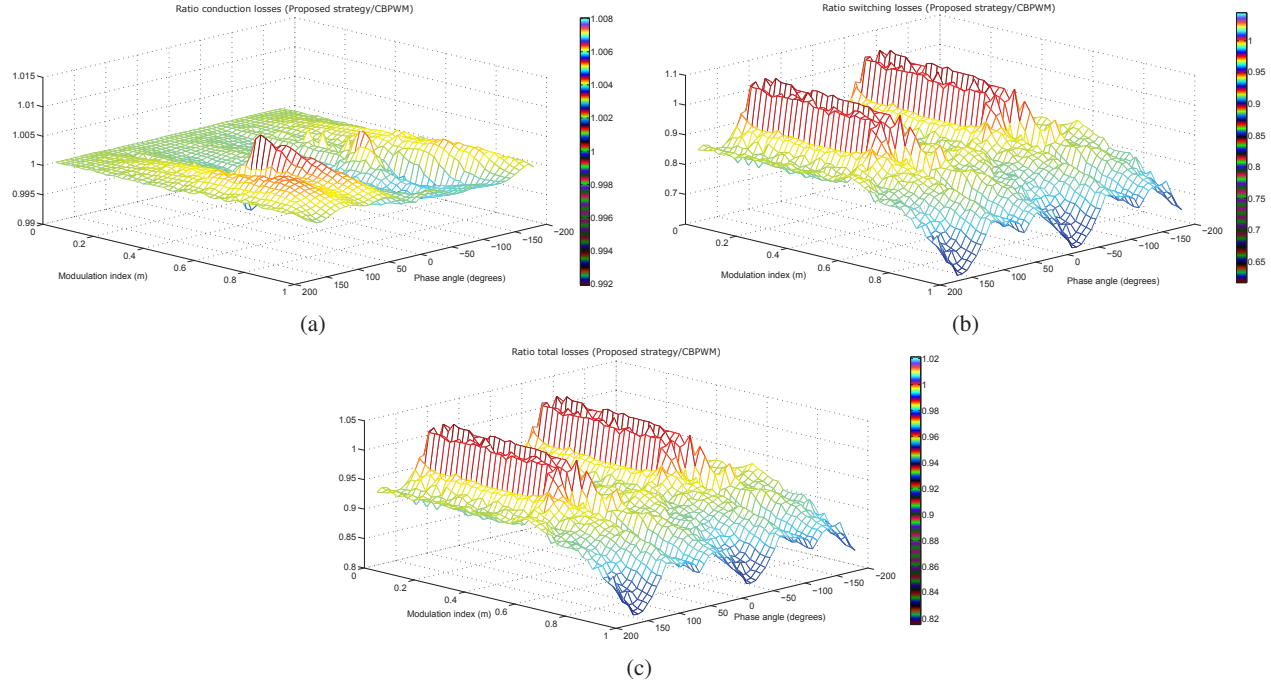


Fig. 15. Losses study of the proposed method over the conduction losses of the standard CBPWM: (a) Conduction losses ratio, (b) switching losses and (c) total losses.

have been estimated using the conduction and switching characteristic curves shown in the datasheet of the manufacturer. A switching frequency of 2.5 kHz has been considered.

Fig. 15(a) shows the ratio of conduction losses of the proposed modulation method over the standard CBPWM for all modulation indices and power factors. As the only difference between both modulations is the type of semiconductor that is conducting at any instant, i.e. IGBT or diode, the ratio of conduction losses are close to one for all the operating conditions. Consequently, both methods exhibit similar conduction losses.

Fig. 14(b) shows the ratio between the switching losses of the two algorithms. The proposed algorithm exhibits lower switching losses than standard CBPWM for all the operating conditions, except when the modulation index is below 0.5 and the power factor is within a narrow area close to 0. Under these circumstances the switching losses are around 3% higher when the proposed method is used. This is attributed to the additional commutations that take place at the beginning of some switching periods because of the added zero-sequence voltage that increase the switching power losses. On the contrary, when the modulation index is higher than 0.5 (which is quite common in many applications) the switching losses are considerably lower with the proposed algorithm. This is especially noticeable at high modulation

Table II
NORMALIZED LOSSES

	Proposed Algorithm	CBPWM	Modulation in[34]	Modulation in [44]
Normalized Switching Losses	1	1.17	∼1	1.56
Normalized Total Losses	1	1.09	∼1	1.27

Table III
THD AND WTHD FOR DIFFERENT MODULATION METHODS FOR A MODULATION INDEX OF 0.9 AND $\varphi = 30^{o}$

	Proposed Algorithm	CBPWM	Modulation in[34]	Modulation in [44]
THD	35.15%	34.36%	35.26%	50.75%
WTHD	0.5670%	0.3923%	0.5683%	0.7468%

indices, where a significant reduction of the switching losses is obtained (see Fig. 14(b)). The average value of the surface displayed in Fig. 14(b) is 0.85, meaning than an averaged reduction on the switching losses of 15% is achieved with the proposed control algorithm.

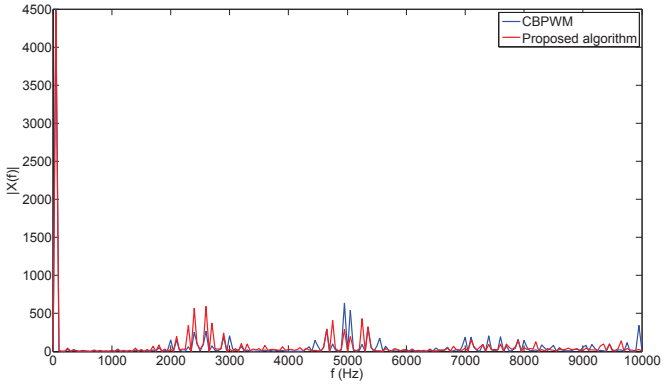
Fig. 15(c) shows the ratio of total power losses. Similar conclusions to those highlighted for the switching losses can be derived. In this case, since the conduction losses are similar in both algorithms, an averaged reduction of around 8% in the total losses is obtained if the new control algorithm is used. A similar procedure has been followed to evaluate the losses of the rest of the methods used in the previous section. Table II shows the ratio of the averaged switching and total losses for different algorithms. These values are calculated averaging the converter losses for the complete range of operating conditions (power factors and modulation indices). The data shown in Table II is normalized with regard to the averaged losses of the proposed control algorithm. The modulation strategy introduced in [34] presents similar losses to the proposed control algorithm. However, the strategy in [44] presents an increase of around 56% in the switching losses and of around 27% in the total losses.

C. Harmonic Distortion Analysis

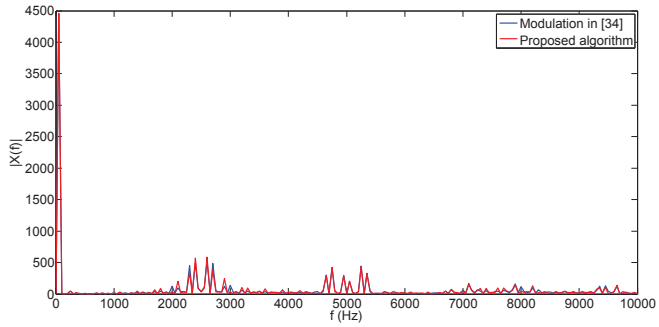
This section benchmarks the harmonic distortion of the proposed method against the modulation methods used in previous sections. To quantify the quality of the voltage waveforms, the total harmonic distortion (THD) and the weighted THD (WTHD) have been computed. These two magnitudes are shown in Table III for the different modulation methods when *m*=0.9, the phase of the current respect to the voltage is $\varphi = 30^{o}$ and the switching frequency is 2.5 kHz.

The spectral energy generated by the proposed algorithm, the standard CBPWM and the modulation introduced in [34] are equivalent. Therefore, the resulting THD values are almost equal. However, the amplitude of the first set of harmonics centered around the switching frequency is lower in the standard CBPWM compared to both the proposed method and the modulation introduced in [34]. This is shown in Figs. 16(a) and 16(b). Consequently, the WTHD of the CBPWM is lower or, equivalently, the CBPWM generates voltage waveforms with better quality. The decrease on the power quality caused by the proposed algorithm is due to a combination of two factors; the decrease of the averaged switching frequency that the proposed modulation features and the voltage spikes in the voltage waveforms explained in Section III.

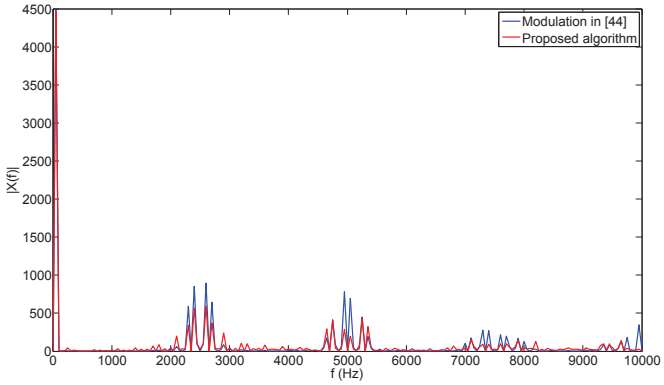
Fig. 16(c) shows the harmonic spectra of the voltage waveforms from the modulation method introduced in [44]. In this case, the harmonic components are larger than the rest of algorithms resulting in higher values of both THD and WTHD.



(a)



(b)



(c)

Fig. 16. Harmonic distortion analysis.

D. Closed Loop Operation

Previous results have shown the operation of the proposed algorithm in open-loop. This section demonstrates its operation in closed-loop. A model of a 5 MW, 3.3 kV synchronous machine with 3 pairs of poles has been developed. The nominal speed of the machine is 1000 rpm and the value of the machine inductors has been set to 0.1 pu. The machine is controlled by a three-phase NPC converter with a *dc*-bus voltage of 5000V and a *dc*-bus capacitance of 5 mF. The rotational speed is regulated by means of a field-oriented controller (FOC). Fig. 17 shows a diagram of the closed-loop controller that has been implemented.

Fig. 18 shows the simulation results obtained when the proposed control algorithm is used. In particular, Fig. 18(a) shows the line-to-line voltage, the phase currents and the voltage of the *dc*-bus capacitors of the NPC drive. Fig. 18(b) shows the rotational speed of the machine. Initially, the machine is working

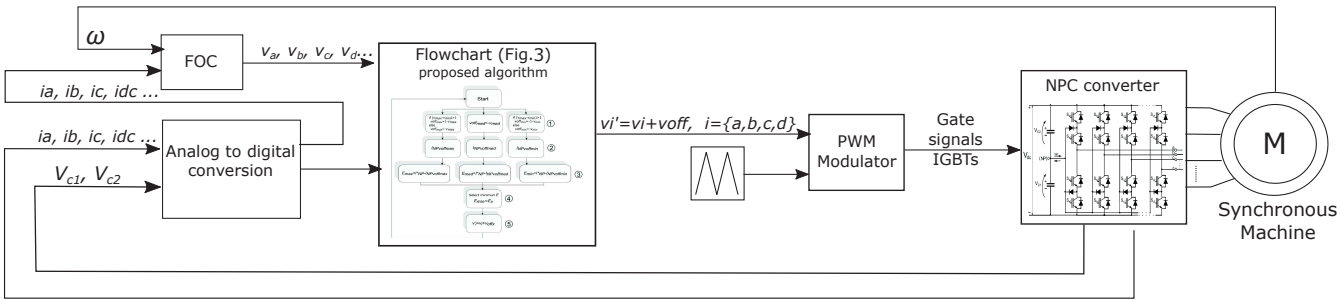
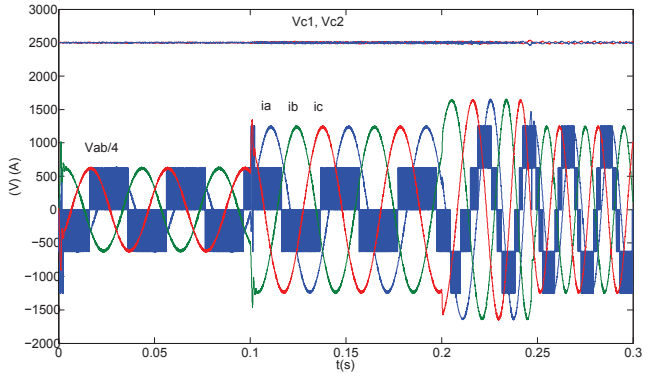
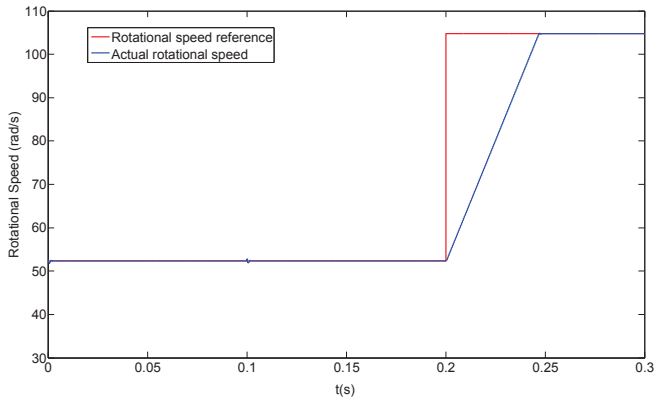


Fig. 17. The implemented closed-loop controller.



(a)



(b)

Fig. 18. Closed loop operation: (a) line-to-line voltage, phase currents and voltage of the *dc*-bus capacitors of the NPC drive, and (b) rotational speed of the machine.

at half the nominal torque and half of the nominal speed. At t=0.1 s the torque demand is increased up to the nominal torque. It can be observed that the current increases accordingly. At t=0.2 s the rotational speed reference is increased up to the nominal speed. This requires an increase of the frequency and the amplitude of the voltage waveforms to control the machine. The drive is able to track the speed reference correctly. The proposed algorithm regulates accurately the NP voltage at its reference value (2500 V). There are no NP voltage deviations in the steady state and during the transient.

V. Conclusion

This paper has proposed a generalised PWM method based on the calculation of the proper zero-sequence voltage that has to be injected into the reference signals to help for capacitor voltage balance in multiphase three-level NPC converters. All the feasible zero sequences that achieve the clamping of one of the normalized reference voltages to $+1$, 0 and -1 are considered and evaluated, and the one that achieves optimal capacitor voltage balance is selected. The proposed algorithm matches or even improves slightly the performance of some of the modern modulation techniques for three-phase NPC converters [34] in terms of NP voltage regulation capability, efficiency and power quality. Furthermore, it is not only limited to three-phase NPC converters. Its main novelty lies on the fact that it is formulated following a generalized approach that makes it applicable to NPC converters with any number of phases. In addition to that, it also features the following characteristics:

- It is able to regulate the NP voltage and to mitigate the low-frequency NPC voltage ripples for balanced and unbalanced load conditions.
- It exhibits low switching losses for most of the working conditions. On average, a reduction of 15% on the switching losses and 8% on the total losses is obtained with regard to the standard CBPWM.
- It does not rely on the use of external controllers to regulate the NP voltage. Consequently, no controller tuning is needed and it performs optimally for any operating conditions.

All in all, the proposed algorithm represents an interesting alternative to regulate the NP voltage in multiphase NPC converters. It achieves optimal trade-off in terms of NP voltage controllability, power losses and efficiency with regards to other modulation methods and exhibits very low computational burden facilitating its implementation in a digital controller.

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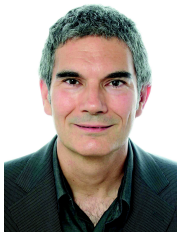

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