National Semiconductor

PRELIMINARY
November 1996

LMX2301
PLLatinum™ 160 MHz Frequency Synthesizer for RF Personal Communications

General Description

The LMX2301 is a high performance frequency synthesizer designed for RF operation up to 160 MHz. It is fabricated using National's ABiC IV BiCMOS process.

LMX2301, which employs the digital phase lock loop technique, combined with a high quality reference oscillator and a loop filter, provides the tuning voltage for the voltage controlled oscillator to generate a very stable, low noise local oscillator signal.

Serial data is transferred into the LMX2301 via a three line MICROWIRE™ interface (Data, Enable, Clock). Supply voltage can range from 2.7V to 5.5V.

The LMX2301 features very low current consumption, typically 2 mA at 3V.

The LMX2301 is available in a TSSOP 20-pin surface mount plastic package.

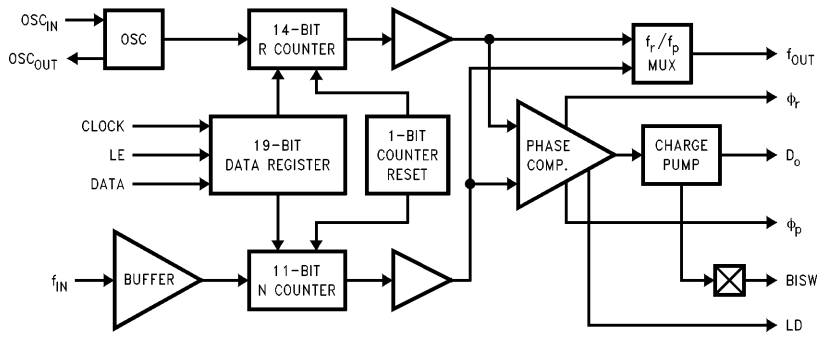
Features

- RF operation up to 160 MHz
- 2.7V to 5.5V operation
- Low current consumption:
  I_{CC} = 2 mA (typ) at V_{CC} = 3V
- Internal balanced, low leakage charge pump
- Small-outline, plastic, surface mount TSSOP, 0.173″ wide package

Applications

- Analog Cellular telephone systems (AMPS, ETACS, NMT)
- Portable wireless communications (PCS/PCN, cordless)
- Other wireless communication systems

Block Diagram



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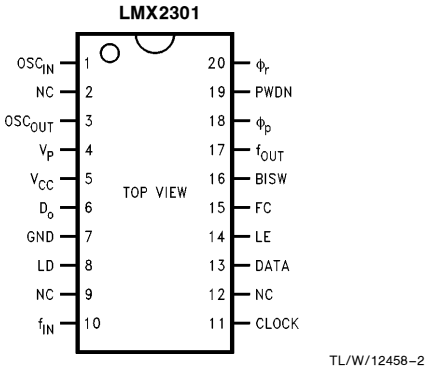
Connection Diagram



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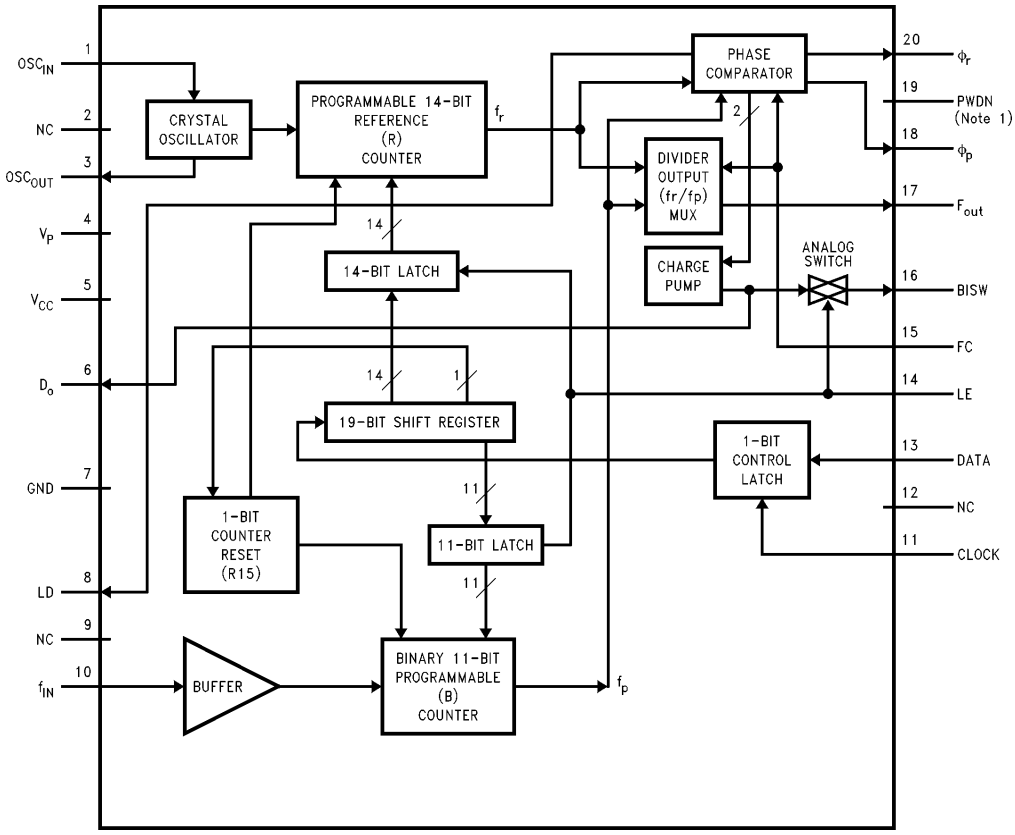
20-Lead (0.173″ Wide) Thin Shrink Small Outline Package (TM)
Order Number LMX2301TM or LMX2301TMX
See NS Package Number MTC20

Pin Descriptions

Pin No.	Pin Name	I/O	Description
1	OSC_{IN}	I	Oscillator input. A CMOS inverting gate input intended for connection to a crystal resonator for operation as an oscillator. The input has a $V_{CC}/2$ input threshold and can be driven from an external CMOS or TTL logic gate. May also be from a reference oscillator.
3	OSC_{OUT}	O	Oscillator output.
4	V_P		Power supply for charge pump. Must be $\geq V_{CC}$.
5	V_{CC}		Power supply voltage input. Input may range from 2.7V to 5.5V. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane.
6	D_o	O	Internal charge pump output. For connection to a loop filter for driving the input of an external VCO.
7	GND		Ground.
8	LD	O	Lock detect. Output provided to indicate when the VCO frequency is in ''lock''. When the loop is locked, the pin's output is HIGH with narrow low pulses.
10	f_{IN}	I	RF buffer input. Small signal input from the VCO.
11	CLOCK	I	High impedance CMOS Clock input. Data is clocked in on the rising edge, into the various counters and registers.
13	DATA	I	Binary serial data input. Data entered MSB first. LSB is control bit. High impedance CMOS input.
14	LE	I	Load enable input (with internal pull-up resistor). When LE transitions HIGH, data stored in the shift registers is loaded into the appropriate latch (control bit dependent). Clock must be low when LE toggles high or low. See Serial Data Input Timing Diagram.
15	FC	I	Phase control select (with internal pull-up resistor). When FC is LOW, the polarity of the phase comparator and charge pump combination is reversed.
16	BISW	O	Analog switch output. When LE is HIGH, the analog switch is ON, routing the internal charge pump output through BISW (as well as through D_o).
17	f_{OUT}	O	Monitor pin of phase comparator input. CMOS output.
18	ϕ_p	O	Output for external charge pump. ϕ_p is an open drain N-channel transistor and requires a pull-up resistor.
19	PWDN	I	Power Down (with internal pull-up resistor). PWDN = HIGH for normal operation. PWDN = LOW for power saving. Power down function is gated by the return of the charge pump to a TRI-STATE condition.
20	ϕ_r	O	Output for external charge pump. ϕ_r is a CMOS logic output.
2,9,12	NC		No connect.

Functional Block Diagram



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Note 1: The power down function is gated by the charge pump to prevent any unwanted frequency jumps. Once the power down pin is brought low the part will go into power down mode when the charge pump reaches a TRI-STATE condition.

Absolute Maximum Ratings (Notes 1 and 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Power Supply Voltage
- V_{CC} −0.3V to +6.5V
- V_P −0.3V to +6.5V

Voltage on Any Pin with GND = 0V (V_I) −0.3V to V_{CC} +0.3V

Storage Temperature Range (T_S) −65°C to +150°C

Lead Temperature (T_L) (solder, 4 sec.) +260°C

Recommended Operating Conditions

Power Supply Voltage
- V_{CC} 2.7V to 5.5V
- V_P V_{CC} to +5.5V

Operating Temperature (T_A) −40°C to +85°C

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: This device is a high performance RF integrated circuit with an ESD rating < 2 keV and is ESD sensitive. Handling and assembly of this device should only be done at ESD workstations.

Electrical Characteristics V_{CC} = 5V, V_P = 5V; −40°C < T_A < 85°C, except as specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{CC}	Power Supply Current	V_{CC} = 3.0V		2.0	5	mA
		V_{CC} = 5.0V		3.0		mA
$I_{CC-PWDN}$	Power Down Current	V_{CC} = 3.0V		30	180	μA
		V_{CC} = 5.0V		60	350	μA
f_{IN}	RF Input Operating Frequency		45		160	MHz
f_{OSC}	Oscillator Input Operating Frequency		5		20	MHz
f_ϕ	Phase Detector Frequency				10	MHz
Pf_{IN}	Input Sensitivity	V_{CC} = 2.7V to 5.5V	−10		+6	dBm
V_{OSC}	Oscillator Sensitivity	OSC_{IN}	0.5			V_{PP}
V_{IH}	High-Level Input Voltage	*	0.7 V_{CC}			V
V_{IL}	Low-Level Input Voltage	*			0.3 V_{CC}	V
I_{IH}	High-Level Input Current (Clock, Data)	V_{IH} = V_{CC} = 5.5V	−1.0		1.0	μA
I_{IL}	Low-Level Input Current (Clock, Data)	V_{IL} = 0V, V_{CC} = 5.5V	−1.0		1.0	μA
I_{IH}	Oscillator Input Current	V_{IH} = V_{CC} = 5.5V			100	μA
I_{IL}		V_{IL} = 0V, V_{CC} = 5.5V	−100			μA
I_{IH}	High-Level Input Current (LE, FC)	V_{IH} = V_{CC} = 5.5V	−1.0		1.0	μA
I_{IL}	Low-Level Input Current (LE, FC)	V_{IL} = 0V, V_{CC} = 5.5V	−100		1.0	μA

*Except f_{IN} and OSC_{IN}

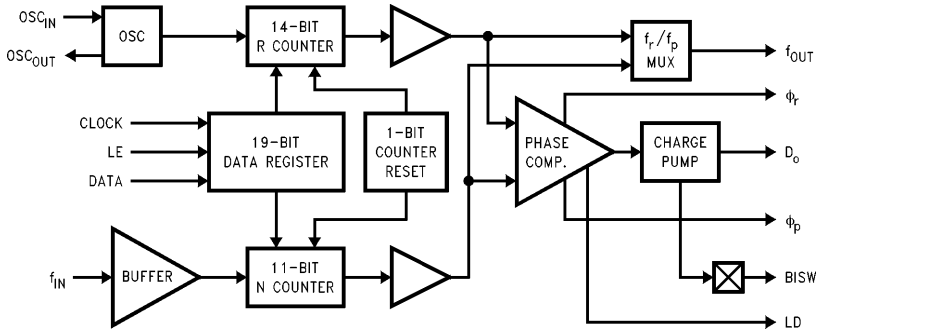
Electrical Characteristics $V_{CC} = 5.0V$, $V_P = 5.0V$; $-40°C < T_A < 85°C$, except as specified (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$I_{D_o\text{-source}}$	Charge Pump Output Current	$V_{D_o} = V_P/2$		−5.0		mA
$I_{D_o\text{-sink}}$		$V_{D_o} = V_P/2$		5.0		mA
$I_{D_o\text{-Tri}}$	Charge Pump TRI-STATE® Current	$0.5V \leq V_{D_o} \leq V_P - 0.5V$ $T_A = 25°C$	−5.0		5.0	nA
V_{OH}	High-Level Output Voltage	$I_{OH} = -1.0$ mA**	$V_{CC} - 0.8$			V
V_{OL}	Low-Level Output Voltage	$I_{OL} = 1.0$ mA**			0.4	V
V_{OH}	High-Level Output Voltage (OSC_{OUT})	$I_{OH} = -200\ \mu A$	$V_{CC} - 0.8$			V
V_{OL}	Low-Level Output Voltage (OSC_{OUT})	$I_{OL} = 200\ \mu A$			0.4	V
I_{OL}	Open Drain Output Current (ϕ_P)	$V_{CC} = 5.0V$, $V_{OL} = 0.4V$	1.0			mA
I_{OH}	Open Drain Output Current (ϕ_P)	$V_{OH} = 5.5V$			100	μA
R_{ON}	Analog Switch ON Resistance			100		Ω
t_{CS}	Data to Clock Set Up Time	See Data Input Timing	50			ns
t_{CH}	Data to Clock Hold Time	See Data Input Timing	10			ns
t_{CWH}	Clock Pulse Width High	See Data Input Timing	50			ns
t_{CWL}	Clock Pulse Width Low	See Data Input Timing	50			ns
t_{ES}	Clock to Enable Set Up Time	See Data Input Timing	50			ns
t_{EW}	Enable Pulse Width	See Data Input Timing	50			ns

**Except OSC_{OUT}

Functional Description

The simplified block diagram below shows the 19-bit data register, the 14-bit R Counter and the R15 Latch, and the 11-bit N Counter (intermediate latches are not shown). The data stream is clocked (on the rising edge) into the DATA input, MSB first. If the Control Bit (last bit input) is HIGH, the DATA is transferred into the R Counter (programmable reference divider) and the S Latch (power up counter reset). If the Control Bit (LSB) is LOW, the DATA is transferred into the N Counter (programmable divider).



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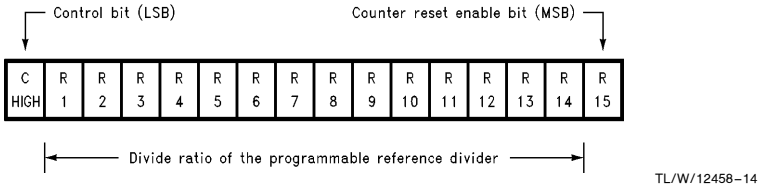
PROGRAMMABLE REFERENCE DIVIDER (R COUNTER) AND COUNTER RESET (R15 LATCH)

If the Control Bit (last bit shifted into the Data Register) is HIGH, data is transferred from the 19-bit shift register into a 14-bit latch (which sets the 14-bit R Counter) and the 1-bit R15 Latch, which can be used to force an immediate load of the R and N counters during a cold power up condition. Serial data format is shown below.



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14-BIT PROGRAMMABLE REFERENCE DIVIDER RATIO (R COUNTER)

Divide Ratio R	R 14	R 13	R 12	R 11	R 10	R 9	R 8	R 7	R 6	R 5	R 4	R 3	R 2	R 1
3	0	0	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Notes: Divide ratios less than 3 are prohibited.

Divide ratio: 3 to 16383

R1 to R14: These bits select the divide ratio of the programmable reference divider.

C: Control bit (set to HIGH level to load R counter and R15 Latch)

Data is shifted in MSB first.

1-BIT COUNTER RESET (R15 LATCH)

Counter Reset	R 15
Remove Forced Load	0
Force Load State	1

The 1-bit counter reset latch controls whether the R and N counters are immediately forced to load conditions upon power up. If R[15] = HIGH, the N and R latch states are immediately read into the respective counters.

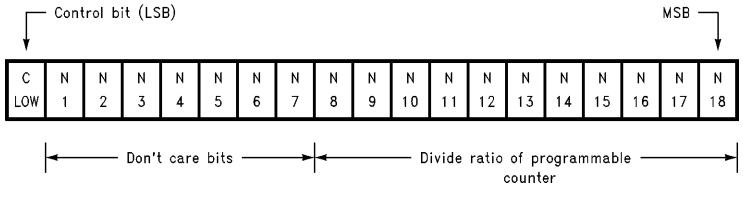
SUGGESTED PROGRAMMING SEQUENCE AFTER COLD POWER-UP

1. Program N counter with desired divide ratio.
2. Program R counter with R15 = 1 and desired divide ratio. (N and R counters hold at load state.)
3. Program R counter with R15 = 0 and desired divide ratio. (N and R counters start counting.)

Functional Description (Continued)

PROGRAMMABLE DIVIDER (N COUNTER)

The N counter consists of the 11-bit programmable counter. If the Control Bit (last bit shifted into the Data Register) is LOW, data is transferred from the 19-bit shift register into an 11-bit latch, which sets the 11-bit programmable Counter. Serial data format is shown below.



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Note: R8 to R18: Programmable counter divide ratio control bits (3 to 2047)

7 LSB BITS OF N REGISTER

Divide Ratio	N 7	N 6	N 5	N 4	N 3	N 2	N 1
X	X	X	X	X	X	X	X

Note: X = Don't care state

11-BIT PROGRAMMABLE COUNTER DIVIDE RATIO

Divide Ratio N	N 18	N 17	N 16	N 15	N 14	N 13	N 12	N 11	N 10	N 9	N 8
3	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

Note: Divide ratio: 3 to 2047 (Divide ratios less than 3 are prohibited)

EQUATION FOR OUTPUT FREQUENCY DETERMINATION

$f_{VCO} = [N] \times f_{OSC}/R$

f_{VCO}: Output frequency of external voltage controlled oscillator (VCO)

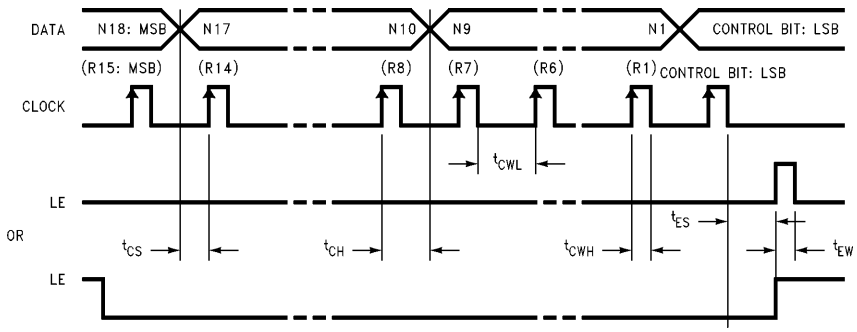
N: Preset divide ratio of binary 11-bit programmable counter (3 to 2047)

f_{OSC}: Output frequency of the external reference frequency oscillator

R: Preset divide ratio of binary 14-bit programmable reference counter (3 to 16383)

Functional Description (Continued)

SERIAL DATA INPUT TIMING



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Notes: Parenthesis data indicates programmable reference divider data.

Data shifted into register on clock rising edge.

Data is shifted in MSB first.

Test Conditions: The Serial Data Input Timing is tested using a symmetrical waveform around $V_{CC}/2$. The test waveform has an edge rate of 0.6 V/ns with amplitudes of 2.2V @ V_{CC} = 2.7V and 2.6V @ V_{CC} = 5.5V.

Phase Characteristics

In normal operation, the FC pin is used to reverse the polarity of the phase detector. Both the internal and any external charge pump are affected.

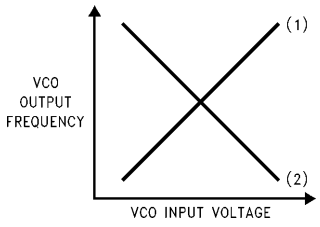
Depending upon VCO characteristics, FC pin should be set accordingly:

When VCO characteristics are like (1), FC should be set HIGH or OPEN CIRCUIT;

When VCO characteristics are like (2), FC should be set LOW.

When FC is set HIGH or OPEN CIRCUIT, the monitor pin of the phase comparator input, f_{out}, is set to the reference divider output, f_r. When FC is set LOW, f_{out} is set to the programmable divider output, f_p.

VCO Characteristics



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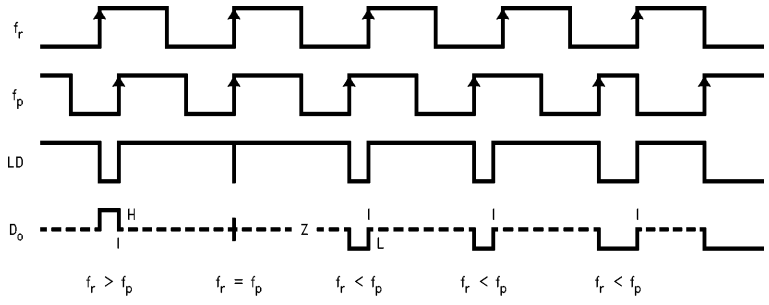
PHASE COMPARATOR AND INTERNAL CHARGE PUMP CHARACTERISTICS



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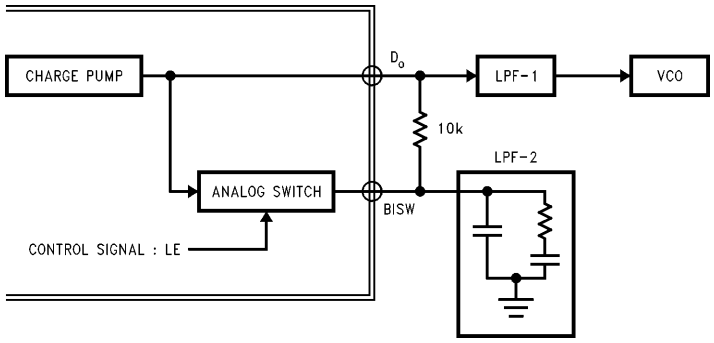
Notes: Phase difference detection range: -2π to $+2\pi$

The minimum width pump up and pump down current pulses occur at the D_o pin when the loop is locked.

FC = HIGH

Analog Switch

The analog switch is useful for radio systems that utilize a frequency scanning mode and a narrow band mode. The purpose of the analog switch is to decrease the loop filter time constant, allowing the VCO to adjust to its new frequency in a shorter amount of time. This is achieved by adding another filter stage in parallel. The output of the charge pump is normally through the D_O pin, but when LE is set HIGH, the charge pump output also becomes available at BISW. A typical circuit is shown below. The second filter stage (LPF-2) is effective only when the switch is closed (in the scanning mode).



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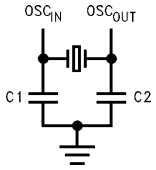
Typical Crystal Oscillator Circuit

A typical circuit which can be used to implement a crystal oscillator is shown below.



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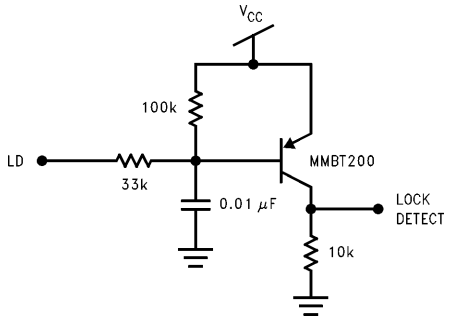
Typical Lock Detect Circuit

A lock detect circuit is needed in order to provide a steady LOW signal when the PLL is in the locked state. A typical circuit is shown below.



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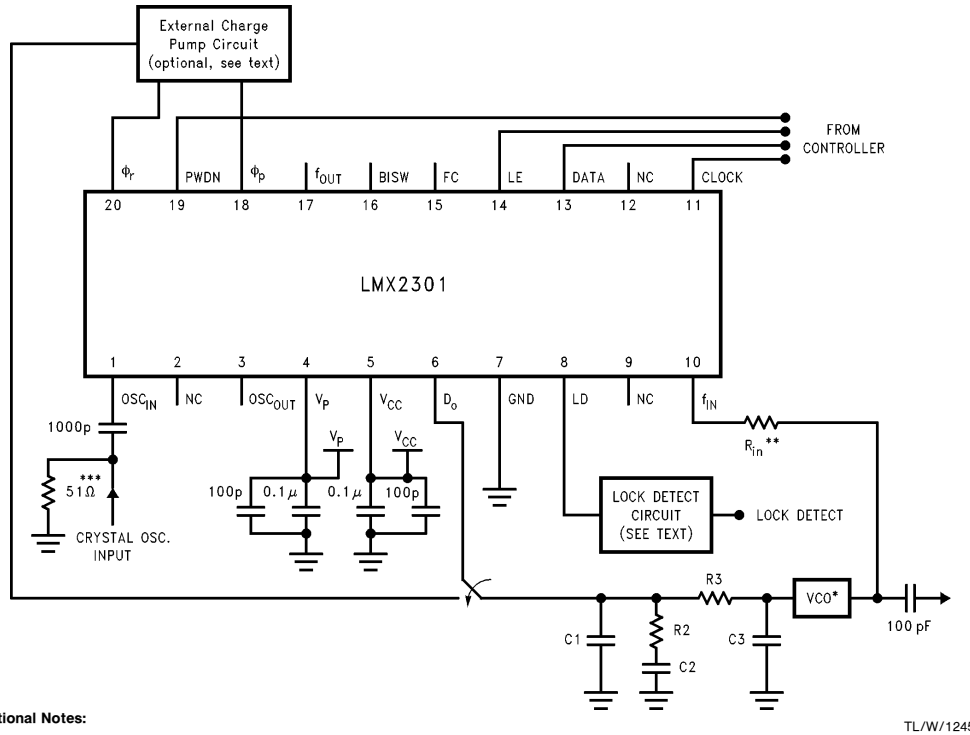
Typical Application Example



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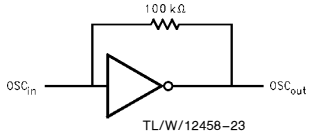
Operational Notes:

* VCO is assumed AC coupled.

** R_{IN} increases impedance so that VCO output power is provided to the load rather than the PLL. Typical values are 10Ω to 200Ω depending on the VCO power level. f_{IN} RF impedance ranges from 40Ω to 100Ω.

*** 50Ω termination is often used on test boards to allow use of external reference oscillator. For most typical products a CMOS clock is used and no terminating resistor is required. OSC_{IN} may be AC or DC coupled. AC coupling is recommended because the input circuit provides its own bias. (See *Figure* below)



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Application Hints:

Proper use of grounds and bypass capacitors is essential to achieve a high level of performance.

Crosstalk between pins can be reduced by careful board layout.

This is an electrostatic sensitive device. It should be handled only at static free work stations.

Application Information

LOOP FILTER DESIGN

A block diagram of the basic phase locked loop is shown.

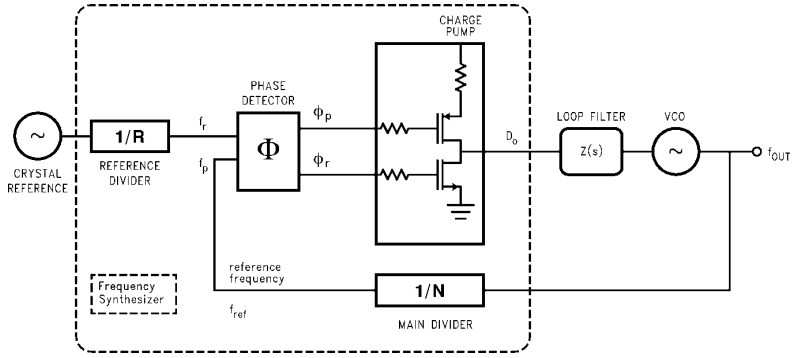

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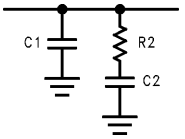
FIGURE 1. Basic Charge Pump Phase Locked Loop

An example of a passive loop filter configuration, including the transfer function of the loop filter, is shown in *Figure 2*.



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$$Z(s) = \frac{s\,(C2 \bullet R2) + 1}{s^2\,(C1 \bullet C2 \bullet R2) + sC1 + sC2}$$

FIGURE 2. 2nd Order Passive Filter

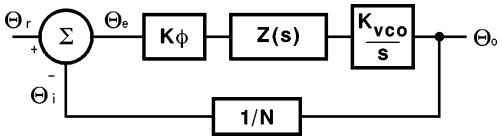
Define the time constants which determine the pole and zero frequencies of the filter transfer function by letting

$$T2 = R2 \bullet C2 \quad (1a)$$

and

$$T1 = R2 \bullet \frac{C1 \bullet C2}{C1 + C2} \quad (1b)$$

The PLL linear model control circuit is shown along with the open loop transfer function in *Figure 3*. Using the phase detector and VCO gain constants [$K\phi$ and K_{VCO}] and the loop filter transfer function [Z(s)], the open loop Bode plot can be calculated. The loop bandwidth is shown on the Bode plot (ωp) as the point of unity gain. The phase margin is shown to be the difference between the phase at the unity gain point and $-180°$.



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Open Loop Gain $= \theta_i/\theta_e = H(s)\,G(s)$
$= K\phi\,Z(s)\,K_{VCO}/Ns$

Closed Loop Gain $= \theta_o/\theta_i = G(s)/[1 + H(s)\,G(s)]$

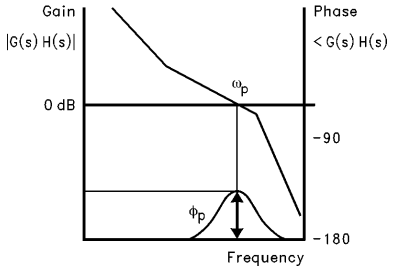

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FIGURE 3. Open Loop Transfer Function

Thus we can calculate the 3rd order PLL Open Loop Gain in terms of frequency

$$G(s) \bullet H(s)|_{s\,=\,j\,\bullet\,\omega} = \frac{-K\phi \bullet K_{VCO}\,(1 + j\omega \bullet T2)}{\omega^2 C1 \bullet N(1 + j\omega \bullet T1)} \bullet \frac{T1}{T2} \quad (2)$$

From equation 2 we can see that the phase term will be dependent on the single pole and zero such that

$$\phi(\omega) = \tan^{-1}(\omega \bullet T2) - \tan^{-1}(\omega \bullet T1) + 180° \quad (3)$$

By setting

$$\frac{d\phi}{d\omega} = \frac{T2}{1 + (\omega \bullet T2)^2} - \frac{T1}{1 + (\omega \bullet T1)^2} = 0 \quad (4)$$

we find the frequency point corresponding to the phase inflection point in terms of the filter time constants T1 and T2. This relationship is given in equation 5.

$$\omega_p = 1/\sqrt{T2 \bullet T1} \quad (5)$$

For the loop to be stable the unity gain point must occur before the phase reaches -180 degrees. We therefore want the phase margin to be at a maximum when the magnitude of the open loop gain equals 1. Equation 2 then gives

$$C1 = \frac{K\phi \bullet K_{VCO} \bullet T1}{\omega_p{}^2 \bullet N \bullet T2} \left\| \frac{(1 + j\omega_p \bullet T2)}{(1 + j\omega_p \bullet T1)} \right\| \quad (6)$$

Application Information (Continued)

Therefore, if we specify the loop bandwidth, ω_p, and the phase margin, ϕ_p, Equations 1 through 6 allow us to calculate the two time constants, T1 and T2, as shown in equations 7 and 8. A common rule of thumb is to begin your design with a 45° phase margin.

$$T1 = \frac{\sec\phi_p - \tan\phi_p}{\omega_p} \quad (7)$$

$$T2 = \frac{1}{\omega_p^2 \bullet T1} \quad (8)$$

From the time constants T1, and T2, and the loop bandwidth, ω_p, the values for C1, R2, and C2 are obtained in equations 9 to 11.

$$C1 = \frac{T1}{T2} \bullet \frac{K\phi \bullet K_{VCO}}{\omega_p^2 \bullet N} \sqrt{\frac{1 + (\omega_p \bullet T2)^2}{1 + (\omega_p \bullet T1)^2}} \quad (9)$$

$$C2 = C1 \bullet \left(\frac{T2}{T1} - 1\right) \quad (10)$$

$$R2 = \frac{T2}{C2} \quad (11)$$

K_{VCO} (MHz/V) — Voltage Controlled Oscillator (VCO) Tuning Voltage constant. The frequency vs voltage tuning ratio.

$K\phi$ (mA) — Phase detector/charge pump gain constant. The ratio of the current output to the input phase differential.

N — Main divider ratio. Equal to RF_{opt}/f_{ref}

RF_{opt} (MHz) — Radio Frequency output of the VCO at which the loop filter is optimized.

f_{ref} (kHz) — Frequency of the phase detector inputs. Usually equivalent to the RF channel spacing.

In choosing the loop filter components a trade off must be made between lock time, noise, stability, and reference spurs. The greater the loop bandwidth the faster the lock time will be, but a large loop bandwidth could result in higher reference spurs. Wider loop bandwidths generally improve close in phase noise but may increase integrated phase noise depending on the reference input, VCO and division ratios used. The reference spurs can be reduced by reducing the loop bandwidth or by adding more low pass filter stages but the lock time will increase and stability will decrease as a result.

THIRD ORDER FILTER

A low pass filter section may be needed for some applications that require additional rejection of the reference sidebands, or spurs. This configuration is given in *Figure 4*. In order to compensate for the added low pass section, the component values are recalculated using the new open loop unity gain frequency. The degradation of phase margin caused by the added low pass is then mitigated by slightly increasing C1 and C2 while slightly decreasing R2.

The added attenuation from the low pass filter is:

$$ATTEN = 20 \log[(2\pi f_{ref} \bullet R3 \bullet C3)^2 + 1] \quad (12)$$

Defining the additional time constant as

$$T3 = R3 \bullet C3 \quad (13)$$

Then in terms of the attenuation of the reference spurs added by the low pass pole we have

$$T3 = \sqrt{\frac{10^{ATTEN/20} - 1}{(2\pi \bullet f_{ref})^2}} \quad (14)$$

We then use the calculated value for loop bandwidth ω_c in equation 11, to determine the loop filter component values in equations 15–17. ω_c is slightly less than ω_p, therefore the frequency jump lock time will increase.

$$T2 = \frac{1}{\omega_c^2 \bullet (T1 + T3)} \quad (15)$$

$$\omega_c = \frac{\tan\phi \bullet (T1 + T3)}{[(T1 + T3)^2 + T1 \bullet T3]} \bullet \left[\sqrt{1 + \frac{(T1 + T3)^2 + T1 \bullet T3}{[\tan\phi \bullet (T1 + T3)]^2}} - 1\right] \quad (16)$$

$$C1 = \frac{T1}{T2} \bullet \frac{K\phi \bullet K_{VCO}}{\omega_c^2 \bullet N} \bullet \left[\frac{(1 + \omega_c^2 \bullet T2^2)}{(1 + \omega_c^2 \bullet T1^2)\,(1 + \omega_c^2 \bullet T3^2)}\right]^{1/2} \quad (17)$$

Application Information (Continued)

EXTERNAL CHARGE PUMP

The LMX PLLatinum series of frequency synthesizers are equipped with an internal balanced charge pump as well as outputs for driving an external charge pump. Although the superior performance of NSC's on board charge pump eliminates the need for an external charge pump in most applications, certain system requirements are more stringent. In these cases, using an external charge pump allows the designer to take direct control of such parameters as charge pump voltage swing, current magnitude, TRI-STATE leakage, and temperature compensation.

One possible architecture for an external charge pump current source is shown in *Figure 9*. The signals ϕ_p and ϕ_r in the diagram, correspond to the phase detector outputs of the LMX2301 frequency synthesizer. These logic signals are converted into current pulses, using the circuitry shown in *Figure 9*, to enable either charging or discharging of the loop filter components to control the output frequency of the PLL.

Referring to *Figure 9*, the design goal is to generate a 5 mA current which is relatively constant to within 0.5V of the power supply rail. To accomplish this, it is important to establish as large of a voltage drop across R5, R8 as possible without saturating Q2, Q4. A voltage of approximately 300 mV provides a good compromise. This allows the current source reference being generated to be relatively repeatable in the absence of good Q1, Q2/Q3, Q4 matching. (Matched transistor pairs is recommended.) The ϕp and ϕr outputs are rated for a maximum output load current of 1 mA while 5 mA current sources are desired. The voltages developed across R4, 9 will consequently be approximately 258 mV, or 42 mV $<$ R8, 5, due to the current density differences {0.026*1n (5 mA/1 mA)} through the Q1, Q2/Q3, Q4 pairs.

In order to calculate the value of R7 it is necessary to first estimate the forward base to emitter voltage drop (Vfn,p) of the transistors used, the V_{OL} drop of ϕp, and the V_{OH} drop of ϕr's under 1 mA loads. (ϕp's V_{OL} $<$ 0.1V and ϕr's V_{OH} $<$ 0.1V.)

Knowing these parameters along with the desired current allow us to design a simple external charge pump. Separating the pump up and pump down circuits facilitates the nodal analysis and give the following equations.

$$R_4 = \frac{V_{R5} - V_T \bullet \ln\left(\frac{i_{source}}{i_{p\,max}}\right)}{i_{source}}$$

$$R_9 = \frac{V_{R8} - V_T \bullet \ln\left(\frac{i_{sink}}{i_{n\,max}}\right)}{i_{sink}}$$

$$R_5 = \frac{V_{R5}}{i_{p\,max}}$$

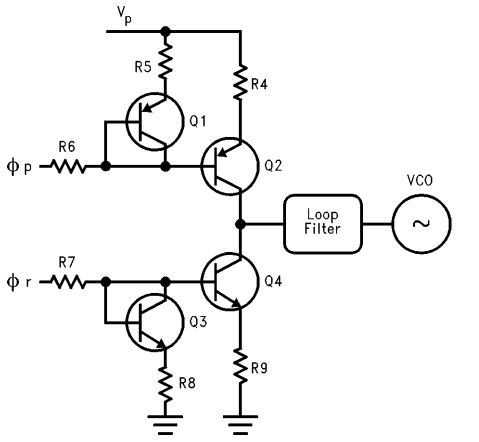
$$R_8 = \frac{V_{R8}}{i_{r\,max}}$$

$$R_6 = \frac{(V_p - V_{VOL\phi p}) - (V_{R5} + Vfp)}{i_{p\,max}}$$

$$R_7 = \frac{(V_P - V_{VOH\phi r}) - (V_{R8} + Vfn)}{i_{max}}$$

EXAMPLE

Typical Device Parameters	$\beta_n = 100$, $\beta_p = 50$
Typical System Parameters	$V_P = 5.0V$;
	$V_{cntl} = 0.5V - 4.5V$;
	$V_{\phi p} = 0.0V$; $V_{\phi r} = 5.0V$
Design Parameters	$I_{SINK} = I_{SOURCE} = 5.0$ mA;
	$V_{fn} = V_{fp} = 0.8V$
	$I_{rmax} = I_{pmax} = 1$ mA
	$V_{R8} = V_{R5} = 0.3V$
	$V_{OL\phi p} = V_{OH\phi r} = 100$ mV



TL/W/12458–28

FIGURE 9

Therefore select

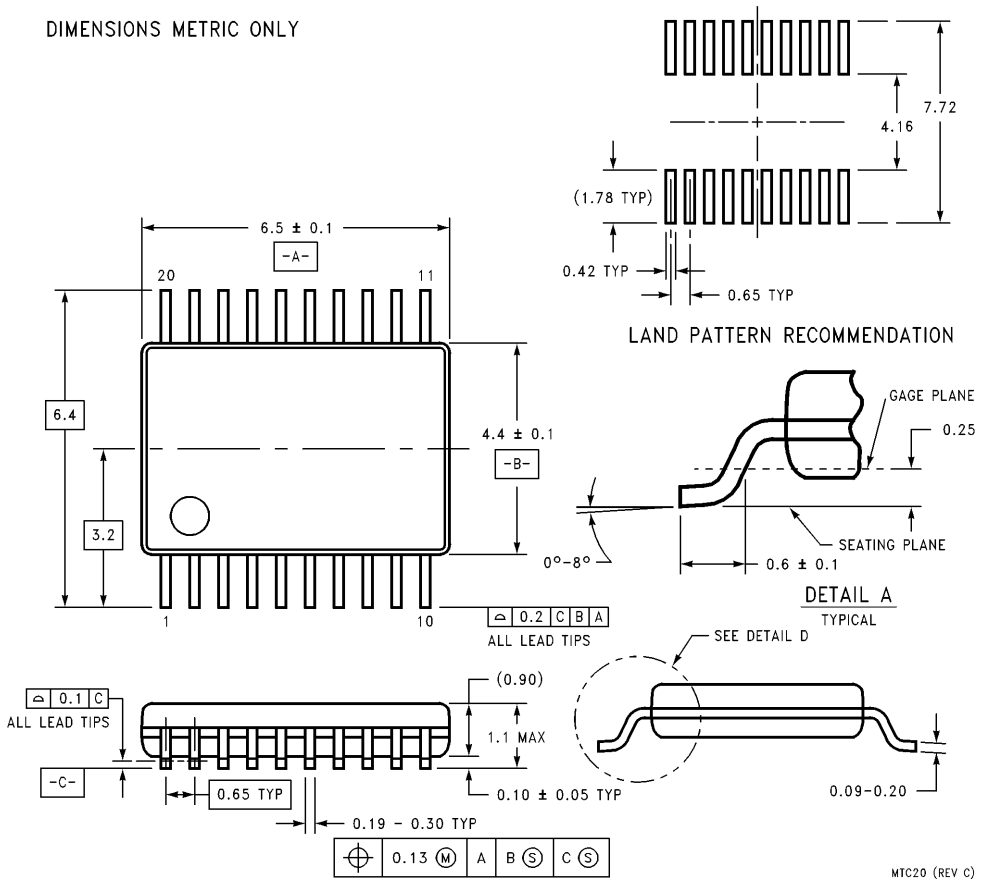
$$R_4 = R_9 = \frac{0.3V - 0.026 \bullet 1n(5.0\text{ mA}/1.0\text{ mA})}{5\text{ mA}} = 51.6\Omega$$

$$R_5 = \frac{0.3V}{1.0\text{ mA}} = 300\Omega$$

$$R_8 = \frac{0.3V}{1.0\text{ mA}} = 300\Omega$$

$$R_6 = R_7 = \frac{(5V - 0.1V) - (0.3V + 0.8V)}{1.0\text{ mA}} = 3.8\text{ k}\Omega$$

Physical Dimensions inches (millimeters) unless otherwise noted



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