c-Si photovoltaic arrays

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Abstract— Crystalline silicon small photovoltaic arrays are shown. Electrical isolation of individual cells and series connection between them to integrate series arrays are discussed. High open circuit voltage values in the range of 100 V and power densities of 7.2 mW/cm^2 have been achieved.
Keywords; photovoltaic; arrays; silicon;

I. INTRODUCTION

An increasing number of applications call for totally or almost totally autonomous electrical powering to drive ubiquitous systems such as distributed sensors or actuators including some devices requiring substantially higher voltage than the mainstream power supply voltages for integrated electronics. One way of achieving high voltages-on-system is by means of photovoltaic arrays delivering electrical power converted from the incoming light. It is well known that a single silicon solar cell can barely provide more than 0.7V output. It becomes then mandatory to connect in series a number of individual cells to scale up the output voltage[1-3]. However the search for single crystal monolithic silicon technology is boosted by the appealing compatibility with mainstream CMOS integrated circuit technology.

II. FABRICATION PROCESSES

Figure 1 shows a cross section of the main devices discussed in this paper.

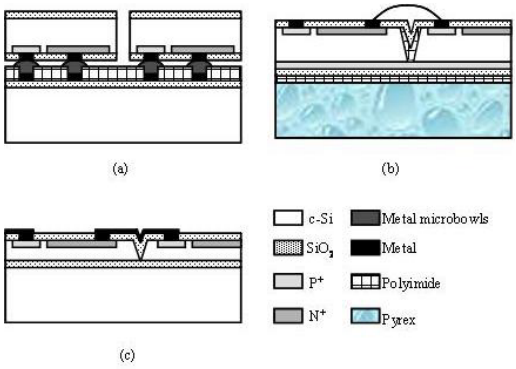

Figure 1. Cross sections of the devices discussed in this paper

A. *High density packaging (Flip-chip) (Figure 1(a))*

This technique requires the separate processing and dicing of the solar cells of suitable size for the subsequent flip-chip and assembly processes. We have used a process using a single crystal silicon substrate which is independently processed. Solar cells are batch processed using sequential diffusions through oxide windows to create the emitter and the base contact area. After another oxidation, contact windows are opened, metal is deposited and patterned. The wafer is diced. The handle wafer is processed by depositing and patterning metal layer on top of an oxidized silicon wafer. The patterning of the metal delineates the interconnections of the solar cells. A layer of polyimide is deposited on top and windows opened to provide access to the contact points. After that, a thin layer of solder paste is deposited on top. Once the two wafers have been fully processed, the assembly is performed, by a pick and flip-chip technique which places the solar cells upside down on top of the solder paste. A subsequent thermal treatment transforms the solder past into balls just at the windows opened in the polyimide [4].

B. *Pyrex bonding (Figure 1(b))*

In this process solar cells are not diced but isolated to each other by means of trenches made by anisotropic etching of silicon. In order to provide mechanical support and substrate isolation we have used a pyrex handle wafer. The silicon wafer is processed by performing selective diffusion processes to create the emitter and the base contacts. The isolation trenches are first defined into the covering oxide photolithographically, the pyrex wafer is adhesively bonded to the silicon wafer and a TMAH anisotropic etching is performed until the pyrex wafer is reached at the bottom. The trenches are then filled with polyimide to planarize the surface and, at the same time, preserving the electrical isolation. PECVD silicon oxide is the deposited, contact windows opened and finally metal deposited and patterned. The bonding of the several devices in series is performed by wire bonding [5].

C. *Monolithic and Fusion bonding (Figure 1(c))*

The advantage of silicon wafer fusion bonding is that this technique is easy to implement and has a good yield withstanding the high temperatures required by the fabrication process. One of the silicon wafers act as a handle wafer and the second as the device wafer. The isolation trenches are

performed in the device wafer until they reach the substrate wafer. Some changes have been introduced in this fabrication process mainly in order to avoid photolitography steps once the isolation grooves are formed. The process starts with the fusion bonding of two silicon wafers. Patterning of the boron diffusion follows the bonding process. After the drive in, phosphorous windows are opened. Then there is an oxide etching of the front side of the wafer and after that, a Si_3N_4 layer is deposited. The Si_3N_4 regions are then patterned and a new oxide is grown to define the grooves that will isolate the individual cells. The grooves are formed by TMAH etching. Another final layer of oxide is then grown to passivate the surface of the grooves. The patterned nitride is then removed so contact windows are opened. The process ends with the evaporation of a thick layer of metal through a shadow mask.

D. Monolithic with SOI wafer processing (Figure 1(c))

This technology is quite similar in concept to the fusion bonding, but now a SOI (Silicon on Insulator) c-Si wafers are used, consisting on an active thin layer, (5 to10 μm), on top of a handle wafer (400 μm),isolated by a buried oxide layer[6]. Similarly to the technologies described above, the top active layer (the previously called device wafer)is where individual solar cells are fabricated and they are isolated from each other by means of trenches made by anisotropic etching. Emitter and base contacts are both in the front side of the wafer, performing the series interconnection of cells by metallization and patterning. The fabrication process starts with a thermal dry oxidation followed by anisotropic etching using TMAH to form isolation trenches. Then SiO_2 is patterned and emitter diffusion is performed. Front and rear SiO_2 is removed and we make a selective isotropic wet etching using to smooth the corners and etch emitter under the metallization path between cells. A thermal oxidation is then made to passivate emitter and to create the antireflective coating film. Boron diffusion ensures ohmic base contacts. And finally metallization of Ti/Pd/Ag and lift-off technique creates the contacts

III. RESULTS

The results we have obtained are summarized in Table I

Table I Summary of the main results

	Flip-chip	Pyrex bonding	Fusion bonding	SOI
nr.of cells in series	9	16	9	169
Cell area(cm^2)	0,089	0,068	0,155	0,00248
Array area(cm^2)	0,79	1,1	1,4	0,42
Cell Voc (V)	0,56	0,53	0,47	0,61
Array Voc (V)	5,05	7,5	4,11	103
Array current Isc (mA)	1,31	0,385	2,45	0,039
Array current density (mA/cm^2)	25,8	12	24,5	17,5
Fill-Factor (FF) (%)	81,5	62,2	37,9	75
Maximum power density (mW/cm2	6,8	1,6	2,7	7,2

It can be seen from Table I that best cell voltage is provided by the SOI devices exceeding 14 mV to the worst cell whuch are the fusion bonding devices and 5 mV to the Flip-chip ones. In terms of the current density produced, it is lear that the fli-chip technique provides the best results although this may also be due to the smallest area of the SOI devices. In terms of the internal series resistance, we see that the FF produced by the fusion bonding process is very poor although the figures reached by the flip-chip and by the SOI devices are quite good even compared to conventional large area devices. May be the power density figure is a key one in the sense that determine the capability of the device to deliver an amount of power even using a low share of the total surface. In this case we see that the SOI devices get the highest figure.

Moreover the convergence to mainstream CMOS integrated circuit technology may advise the use of the SOI technique, because it is simpler, do not require flicp-chip and solder paste processing and avoids the use of wirebonding. This fact can also open the door to applications where the required voltage exceeds significantly the on chip power supply standards, such as MEMS actuators, today requiring step-up switched capacitors converters , or Lab-on-a-chip applications

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