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Active Inductor-Based Tunable Impedance Matching Network for RF Power Amplifier Application

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Abstract

This paper presents the use of a new structure of active inductor named cascoded flipped-active inductor (CASFAI) in a *T*-type high-pass tunable output matching network of a class-E RF power amplifier (RFPA) to control the output power and enhance the efficiency. The designed CASFAI behaves as an inductor in the frequency range of 0-6.9 *GHz*, and has reached to a maximum quality factor of 4406, inductance value of 7.56 *nH*, 3rd order harmonic distortion better than –30 dB for 0 *dBm* input power, while consumes only 2 *mW* power. In order to consider the performance of the proposed active inductor-based tunable output matching network on the output power level and power added efficiency (PAE) of RFPA, the CASFAI is applied as a variable inductor to the output matching network of RFPA. The overall circuit is designed and validated in ADS in a 0.18 µ*m* CMOS process and 1.5 *V* supply voltage. The results indicate that by increasing the inductance value of the matching network in constant operating frequency, the PAE peak moves from high power to low power levels without any degradation. Therefore, it is possible to maintain the power efficiency at the same maximum level for lower input drive levels.

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1. Introduction

Rapid progress in cellular communication and its spread applications have propelled manufacturers of radio transceivers to integrate their products and decrease the number of off-chip elements. Most of blocks forming the wireless communication systems need to be impedance matched with the inputs and/or outputs of other existing blocks in the system, like power amplifier (PA), low noise amplifier (LNA), etc. Power amplifiers are responsible for amplifying the input modulated RF signal before transferring to the antenna. Due to the limited battery life and also its linearity constraints, improving the efficiency of a PA in mobile applications is essentially important [1]. When designing the output matching network of a PA, the output impedance is usually considered constant. However, it is variable most of the time and imposes mismatch conditions to the amplifier, degrading important parameters such as effective output power, efficiency, and phase characteristic. For example, in mobile cell phones, the input impedance of the antenna can be considerably changed by the presence of humans in its vicinity [2]. Furthermore, a mismatch increases the reflection between blocks, and hence, decreases the RF circuit performance, considerably. The impedance matching network can decrease this reflection, maximizes the transferred power to the load, and also minimizes the returns from the load. The impedance matching occurs at a certain frequency (especially at the resonance frequency) and causes that the maximum power is transferred between the supply and load. For an efficient change in the load impedance of the output stage as a function of desired output power level and also for increasing the total efficiency of the PA, a tunable impedance matching network including one or more elements with tuning capability is needed to obtain a desired impedance value. Furthermore, these matching networks can compensate amplitude and phase distortions produced by transistors. On the other hand, amplifiers usually suffer from efficiency reduction in low power region [3]. Therefore, having an efficiency enhancement strategy for low power operating conditions is mandatory.

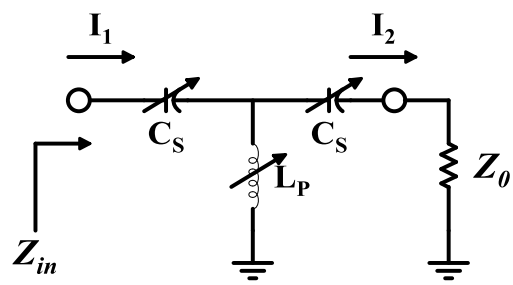


Fig. 1. Configuration of a variable impedance converter using a high-pass *T* network

Most architectures of tunable impedance matching network insert phase variation to the power gain, meaning that each output power has a different phase, causing AM-PM distortion. This will result in linearity degradation of a PA. One invoked method to overcome this issue is using a constant phase matching network. The *T*-type high-pass matching network, shown in Fig. 1, consisting of two high-pass LC networks with constant phase characteristic, is considered here as a variable impedance converter, which converts the system impedance Z_0 to the desired load impedance without any phase variation [3].

The input impedance and phase difference between input and output currents of the *T*-type matching network at the resonance frequency, $\omega = \omega_0 = \frac{1}{\sqrt{L_P C_S}}$, is as follow:

$$Z_{in} = R_{opt} = \frac{L_P}{Z_0 C_S} \qquad \& \qquad \Delta\phi = \frac{\pi}{2} \tag{1}$$

According to (1), at the specified resonance frequency, which corresponds to a constant value for the product of tunable capacitance, C_S, and inductance, L_P, the desired impedance can be varied as a ratio of inductance to capacitance, while the phase difference between the input and output signals is constant (π/2).

Although, there is a little circuit complexity in the matching networks consisting of passive elements, spiral inductors and variable capacitors (varactors), the tuning range of varactors are limited, while spiral inductors are very bulky with low and fixed inductance, low quality factor and self-resonance frequency, sensitive to temperature variation at high frequencies, and incompatible with low cost standard CMOS processes [4]. Therefore, this paper presents a *T*-type matching network with gyrator-based active inductor as a tunable matching network for RFPA, which has more advantages in terms of higher quality factor, tunability performance, ability to implement in low cost CMOS processes, and appropriate for reducing size and cost of the chips.

This paper is organized as follows; in section II, the proposed CMOS active inductor employed in the RFPA is introduced. Section III presents the RFPA design procedure with the active inductor-based tunable output matching network and the results are explored. Finally, conclusion is summarized in section IV.

2. Proposed active inductor

The idea of active inductor originates from the theory of gyrator which is based on two back-to-back connected positive and negative transconductors [5, 6]. As shown in Fig. 2(*a*), when the output port of gyrator is loaded by a capacitor, named gyrator-C network, its input impedance shows inductive behavior, as follow:

$$Z_{in} = s\frac{C}{g_{m1}\, g_{m2}} \quad \Rightarrow \quad L = \frac{C}{g_{m1}\, g_{m2}} \tag{2}$$

Since the input or output impedances of the transconductors in the gyrator-C network are limited, the synthesized inductor is lossy, meaning that it has parasitic resistance and capacitance. The small signal equivalent circuit of a lossy gyrator-C network can be represented by an RLC network as shown in Fig. 2(*b*). This means that the circuit has inductive characteristic only in a specific frequency range.

Usually, simple structures are preferred for RF circuits [7-11]. The configuration of basic flipped-active inductor (FAI) introduced in [9] and [10] is very simple and consists of only two transistors. As shown in Fig. 3(*a*), transistor M_2 located in the forward path has a positive transconductance (g_{m2}) while transistor M_1 in the feedback path provides a negative transconductance (g_{m1}). However, it suffers from low input voltage swing limited to the nMOS threshold voltage minus the overdrive voltage of transistor M_2, which is not sufficient in most applications and increases nonlinearity. Furthermore, this design requires more power consumption to achieve adequate inductance value and high quality factor. In order to overcome these problems, a cascoded flipped-active inductor (CASFAI) presented in [11] is used here for the tunable output matching network

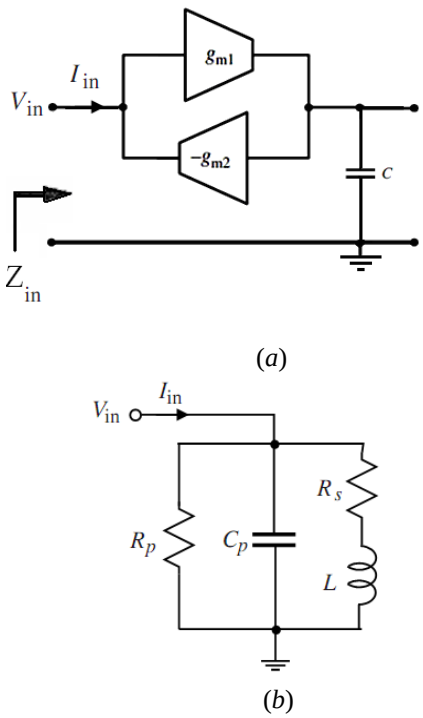


Fig. 2. (*a*) Gyrator-C network, (*b*) equivalent RLC model

of RFPA. In this structure, as shown in Fig. 3(*b*), a common-gate pMOS transistor M_3, added in the feedback path, increases the feedback gain and decreases the equivalent series resistance (R_S) of the inductor by a factor of $g_{m3}r_{o3}$, where r_{o3} is the output resistance of the aforementioned transistor M_3. This leads to an increase in the quality factor of CASFAI in comparison to the conventional FAI. Additionally, the input voltage swing of this architecture can be increased with respect to the conventional FAI, as the drain voltage of M_2 has a value of $V_{D2} = V_{SG3} + V_{G3}$, which can be close to V_{dd} [12]. Moreover, due to the additional loop gain provided by the transistor M_3, the drain voltage of transistor M_2 has a small variation, leading to a decrease in the effect of the channel length modulation, which in turn improves the linearity performance [11].

From Fig. 3(*c*), by neglecting the gate-drain capacitance and considering $g_m >> g_o$, the equivalent RLC model parameters of the CASFAI are as follows:

$$C_p = C_{gs2} \quad , \quad G_p = 1/R_p \approx g_{m2} \qquad (3)$$

$$R_s = \frac{g_{o2}g_{o3}}{g_{m1}g_{m2}g_{m3}} \quad , \quad L_s = \frac{C_{gs3}}{g_{m2}g_{m3}}$$

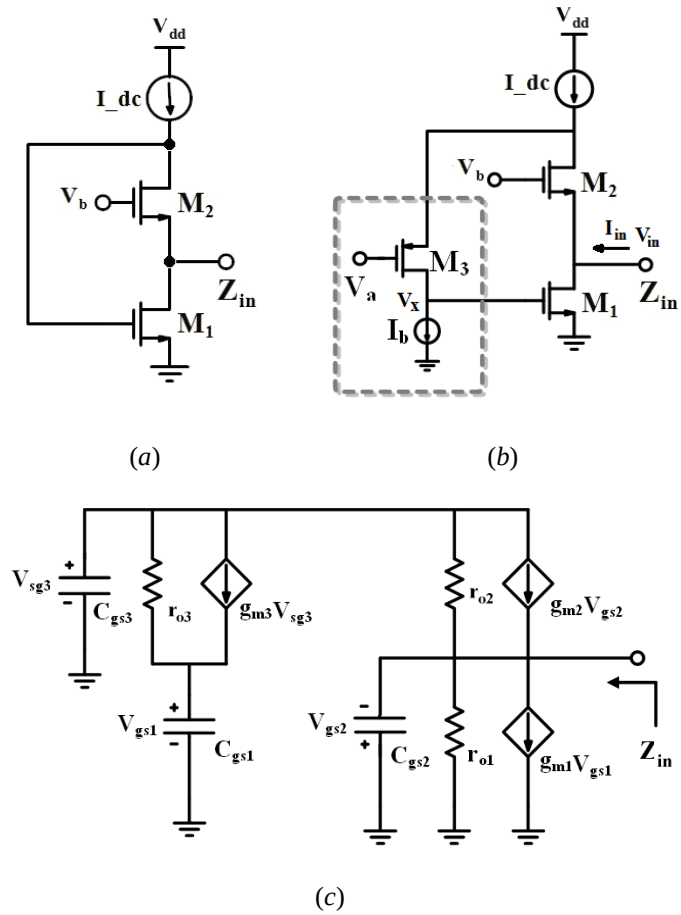


Fig. 3. (a) Basic flipped-active inductor, (b) cascoded flipped-active inductor, (c) small signal equivalent circuit

where g_{mi}, g_{oi}, and C_{gsi} are the transconductance, output conductance, and gate-source capacitance of transistor M_i, respectively. By neglecting the series resistance, the self-resonance frequency, ω_0, and Q of the CASFAI circuit can be expressed as:

$$\omega_0 = \sqrt{\omega_{t2}\omega_{t3}} \quad , \quad Q = \frac{\omega_0}{BW} = \sqrt{\frac{\omega_{t3}}{\omega_{t2}}} \qquad (4)$$

where $\omega_{ti} = g_{mi}/C_{gsi}$ is the unity-gain frequency of transistor M_i. An interesting point is that the transistor M_1 does not affect the inductance value of the CASFAI, leading to more degrees of freedom in the design procedure. Hence, increasing the dimensions of M_1 further reduces the series resistance and, opposite to the FAI structure, it helps to achieve a higher quality factor without degrading the inductance value. Additionally, the inductance value can be increased by reducing the transconductance of M_2, enhancing the parallel resistance

and the quality factor. In this case, the reduction effect of g_{m2} on the series resistance can be compensated by increasing g_{m1}. Alternatively, unlike the basic FAI structure, in order to have a high Q without degrading ω_0, ω_{t3} can be increased just by the bias current of the transistor M_3 (I_b) and without any additional current source [11].

One of the most important characteristics of the active inductor used in the RFPA is its linearity performance. Considering Fig. 3(*b*) to calculate the second and third order harmonic distortions, HD_2 and HD_3, of the proposed CASFAI, the input current of the inductor, I_{in}, should be determined as a nonlinear function of the input voltage, V_{in}. By using a Taylor series expansion and considering the first three terms, I_{in} versus V_{in} can be derived as follow:

$$I_{in} = \beta_1 V_{in} + \beta_2 V_{in}^2 + \beta_3 V_{in}^3 \tag{5}$$

where the coefficients β_1, β_2, and β_3 should be determined through the circuit analysis. On the other hand, the input current of the active inductor is achieved as:

$$I_{in} = I_1 - I_2 \tag{6}$$

where, I_1 and I_2 are the drain currents of the transistors M_1 and M_2, respectively. Using the Taylor series, the drain current of a NMOS transistor can be expressed as [13]:

$$I_d = I_{dc} + g_m V_{gs} + \frac{g'_m}{2} V_{gs}^2 + \frac{g''_m}{6} V_{gs}^3 \tag{7}$$

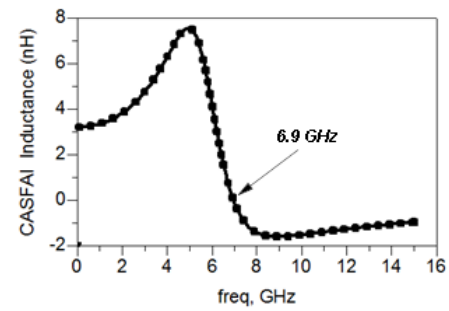
where I_{dc} is the DC bias current, V_{gs} is the voltage signal across the gate-source of the transistor, and g_m, g_m', and g_m'' are given by:

$$g_m = \frac{\partial I_d}{\partial V_{gs}}, \quad g'_m = \frac{\partial^2 I_d}{\partial V_{gs}^2}, \quad g''_m = \frac{\partial^3 I_d}{\partial V_{gs}^3} \tag{8}$$

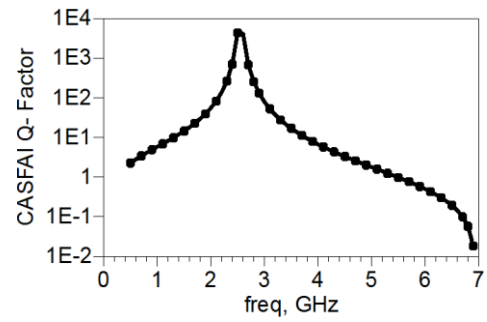
As a result, by considering just the current signal, the drain current of the transistor M_2, I_2, is as follow:

$$I_2 = -g_{m2} V_{in} + \frac{g'_{m2}}{2} V_{in}^2 - \frac{g''_{m2}}{6} V_{in}^3 \tag{9}$$

In order to calculate the drain current of the transistor M_1, we assume that the entire current signal of the transistor M_2 flows through the transistor M_3 and is converted to voltage at the gate of M_1 through the nonlinear resistance of the transistor M_3. So, the gate voltage of M_1, V_x, can be written as:



(*a*)



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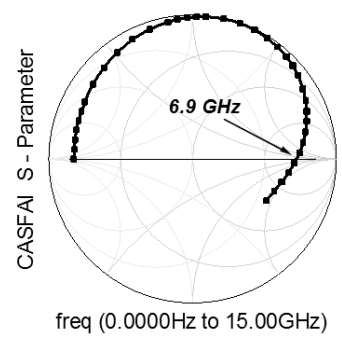
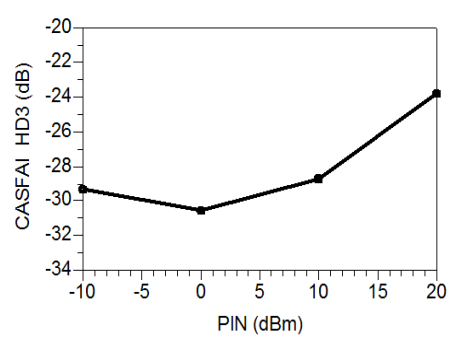


(*c*)



(*d*)

Fig. 4. Characterizations of the CASFAI: (*a*) Inductance value, (*b*) quality factor, (*c*) S-parameter, (*d*) HD_3 versus input power

$$V_x = \alpha_1 I_3 + \alpha_2 I_3^2 + \alpha_3 I_3^3 = -\alpha_1 I_2 + \alpha_2 I_2^2 - \alpha_3 I_2^3 \quad (10)$$

where:

$$\alpha_1 = \frac{\partial V_x}{\partial I_3}, \quad \alpha_2 = \frac{1}{2}\frac{\partial^2 V_x}{\partial I_3^2}, \quad \alpha_3 = \frac{1}{6}\frac{\partial^3 V_x}{\partial I_3^3} \quad (11)$$

As a result, the drain current of M_1 can be given by:

$$I_1 = g_{m1} V_x + \frac{g'_{m1}}{2} V_x^2 + \frac{g''_{m1}}{6} V_x^3 \quad (12)$$

By substituting Eqs. (9), (10), and (12) in (6), β_1, β_2, and β_3 can be derived, which are indicated in Eqs. (13)-(15). The second and third order harmonic distortions can be expressed as Eqs. (16) and (17), respectively.

A brief performance characteristic of the proposed CASFAI structure in a 0.18 µ*m* CMOS process and 1.5 *V* supply voltage is shown in Fig. 4. The width of transistors M_1-M_3 is 16 µ*m*, 17.5 µ*m*, and 24 µ*m*, respectively, all with the length of 0.18 µ*m*. As it is obvious, the proposed structure shows inductance behavior in the frequency range between 0-6.9 *GHz* and has reached to a high quality factor of 4406 and inductance value of 7.56 *nH*, while consumes only 2 *mW* power. Additionally, the proposed CASFAI has a proper linearity performance at 2.4 *GHz* Operating frequency due to its wider dynamic range and less sensitivity to channel length modulation. Fig. 5 shows the large signal S-parameter simulation of the proposed CASFAI at the same frequency. As it can be seen, the CASFAI starts to distort around 8 *dBm* input power level. However, the deviation of real part and imaginary part of S_{11} is around 0.5 *dB* and 0.06 *dB*, respectively for 0-15 *dBm* power range. Table I shows the maximum quality factor, power consumption, inductance value, inductance range, and supply voltage of the CASFAI in comparison with some other works. Although the inductance value of the CASFAI is lower than that in [4, 7, 14], its maximum quality factor as well as its inductance range is higher, while dissipates less power than [4, 7, 8].

3. Proposed RFPA with tunable active inductor-based output matching network

In this section, the performance characteristic of a class-E RFPA with *T*-type tunable output matching network based on the proposed active inductor is discussed. Fig. 6 shows the structure of a class-E PA circuit including the finite DC-feed inductance (L_{dc}), shunt capacitance (C_p), input and output matching networks (L_2-C_2-L_g & L_P-C_S), and a series resonance network (L_1-C_1) tuned at the fundamental harmonic of input signal, leading that only a sinusoidal signal will be passed to the load. The inductor L_g is also responsible for biasing the transistor M_E. The gate bias voltage (V_g) of transistor M_E is set to the threshold point to have a duty cycle of 50%.

Input matching network is used to increase the power gain, while output matching one increases the maximum output power level and efficiency for a given input power level [15]. This paper focuses on the output matching network which converts the standard load resistance (50 Ω) to the desired load (R_{opt}).

In order to have a PA with tunable output matching network, the passive inductor L_P in Fig. 6 is replaced by its proposed CASFAI active counterpart, as shown in Fig. 7, and the overall circuit is designed for 2.4 *GHz* operating frequency. As the inductance value of designed CASFAI equals 4.1 *nH* at 2.4 *GHz* and 1.5 *V* supply voltage (according to Fig. 4(*a*)), the needed capacitors C_S for the output matching network are as below:

$$\beta_1 = g_{m2}\left[1 + \alpha_1 g_{m1}\right] \quad (13)$$

$$\beta_2 = g_{m2}^2\left[\alpha_2 g_{m1} + \alpha_1^2 \frac{g'_{m1}}{2}\right] - \frac{g'_{m2}}{2}\left[1 + \alpha_1 g_{m1}\right] \quad (14)$$

$$\beta_3 = \frac{g''_{m2}}{6}\left[1 + \alpha_1 g_{m1}\right] + \alpha_1 g_{m2}^3\left[\alpha_2 g'_{m1} + \frac{\alpha_1^2 g''_{m1}}{6}\right] - g_{m2}\left[g'_{m2}\left(\alpha_2 g_{m1} + \alpha_1^2 \frac{g'_{m1}}{2}\right) - \alpha_3 g_{m1} g_{m2}^2\right] \quad (15)$$

$$HD_2 = \frac{1}{2}\frac{\beta_2}{\beta_1} V_{in} = \frac{V_{in}}{2}\frac{1}{(1+\alpha_1 g_{m1})}\left[g_{m2}\left(\alpha_2 g_{m1} + \alpha_1^2 \frac{g'_{m1}}{2}\right) - \frac{1}{2}\frac{g'_{m2}}{g_{m2}}(1+\alpha_1 g_{m1})\right] \quad (16)$$

$$HD_3 = \frac{1}{4}\frac{\beta_3}{\beta_1} v_{in}^2 = \frac{v_{in}^2}{4}\left[\frac{g''_{m2}}{6 g_{m2}} + \frac{1}{(1+\alpha_1 g_{m1})}\left(\alpha_1 g_{m2}^2\left(\alpha_2 g'_{m1} + \frac{\alpha_1^2 g''_{m1}}{6}\right) - g'_{m2}\left(\alpha_2 g_{m1} + \alpha_1^2 \frac{g'_{m1}}{2}\right) + \alpha_3 g_{m1} g_{m2}^2\right)\right] \quad (17)$$

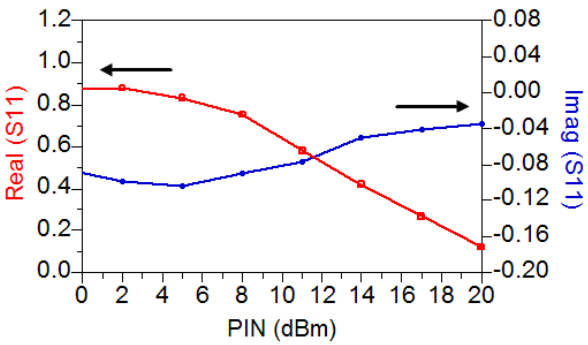


Fig. 5. Large signal S-parameter simulation of the CASFAI

Table I. Performance comparison of CASFAI with some works

Reference	[4]	[7]	[8]	[14]	**CASFAI**
Q-Factor	244	1.5	68000	1067	**4406**
Inductance Value (nH)	153	39	1.1	550	**7.56**
Power Consumption (mW)	10	3	5	0.65	**2**
Inductance Range (GHz)	0.16	0.35	0.53	5.6	**6.9**
Supply Voltage (V)	1.8	3	2	1.8	**1.5**

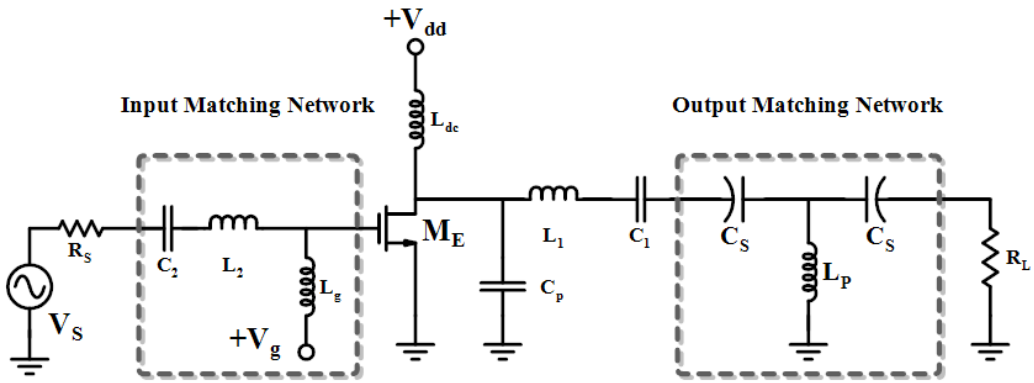


Fig. 6. Schematic of a CMOS class-*E* power amplifier with impedance matching networks

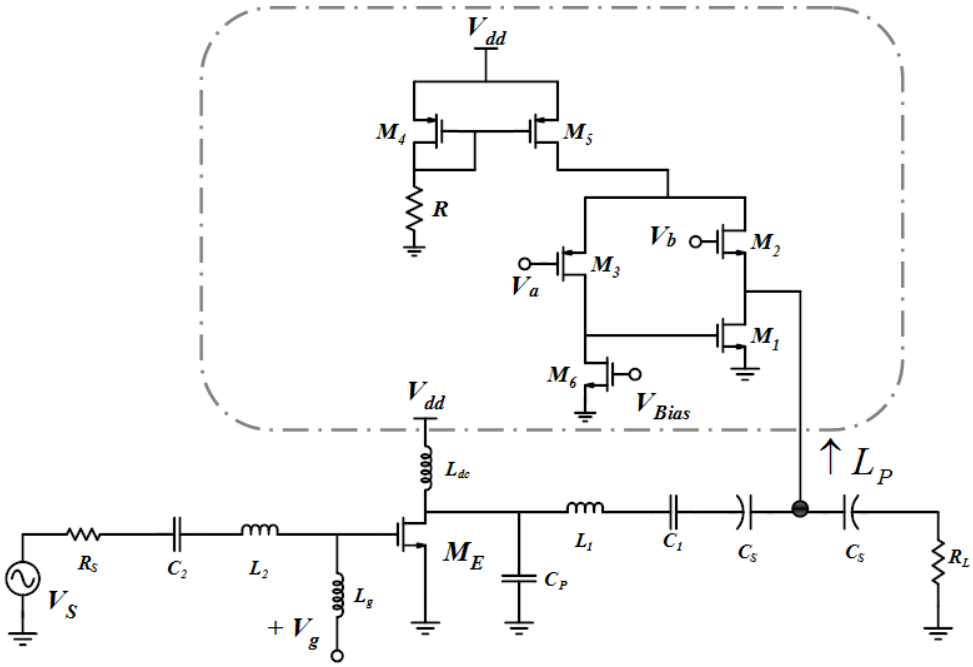


Fig. 7. Schematic of the class-E RFPA with the proposed active inductor-based output matching network

Table II. RFPA parameters

Parameter	Value	Parameter	Value
L_1	9 *nH*	L_2	0.01 *nH*
C_1	0.5 *pF*	C_2	0.5 *pF*
M_E	220 µ*m* / 0.18 µ*m*	L_g	5 *nH*

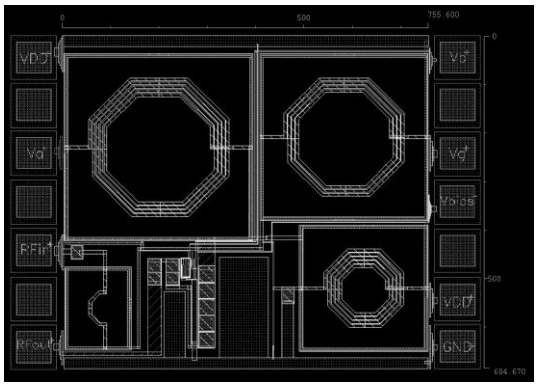


Fig. 8. Layout of the proposed RFPA with active inductor-based output matching network

$$C_S = \frac{1}{L_P \omega^2} \Rightarrow C_S = 1.1\, pF \tag{18}$$

According to Eq. (1) and based on the above parameters for the output matching network, the standard constant load resistance $R_L=50\ \Omega$ is converted to the desired load of $R_{opt}\approx 75\ \Omega$ through the output matching network. Therefore, the output power of the RFPA, P_{out}, DC-feed inductance, L_{dc}, and shunt capacitance, C_P, is obtained which equal approximately 16 *dBm*, 3.64 *nH*, and 0.6 *pF*, respectively, based on the class-E design equations, as below [16, 17]:

$$P_{out} = 1.365 \frac{V_{dd}^2}{R_{opt}} \tag{19}$$

$$L_{dc} = 0.732 \frac{R_{opt}}{\omega} \tag{20}$$

$$C_P = \frac{0.685}{\omega R_{opt}} \tag{21}$$

where V_{dd} and ω are the supply voltage and resonance frequency, respectively. Other parameters of the RFPA are listed in Table II.

The layout of the proposed RFPA with active inductor-based output matching network is shown in Fig. 8. The total chip area is 0.52 mm^2.

Fig. 9 shows the drain voltage and current waveforms of the RFPA, which confirms that the PA works as a class-E power amplifier with non-overlapping current and voltage. Additionally, the drain current and voltage are not at their maximum level at the same time, reducing the power dissipation of the power device.

Some characteristics of the RFPA are given in Fig. 10. In particular, on the one side, Fig. 10(*a*) shows the efficiency of the amplifier versus input power. As it can be seen, the power efficiency is about 72% at input power level of 0 *dBm*. Additionally, for the same input power level, the amplifier generates an output power about 15 *dBm* at the operating frequency of 2.4 *GHz*, as shown in Fig. 10(*b*). On the other hand, power gain and power added efficiency (PAE) versus output power level are given in Figs. 10(*c*) and (*d*), respectively. As it is obvious, for the mentioned output power level of 15 *dBm*, the RFPA has reached to the maximum PAE of 70%. Furthermore, the output power and PAE of the RFPA as a function of input power variations in the range of –20 to 10 *dBm* are demonstrated in Fig. 11. The results reveal that PAE has reached to its maximum value of 70% at the input power level of 0 *dBm*, in which the output power is 15 *dBm*.

The effect of temperature variation on the PAE and power gain of the RFPA with active inductor-based output matching network is given in Fig. 12. As it can be seen, when the temperature varies from -20 °C to +80 °C, the PAE and power gain change only 5% and 0.25 *dB*, respectively.

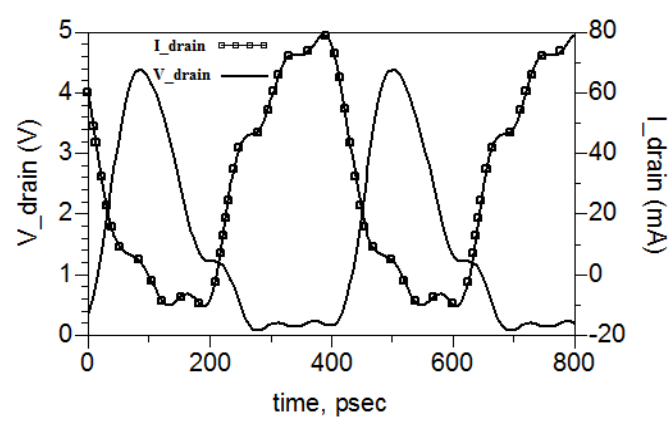
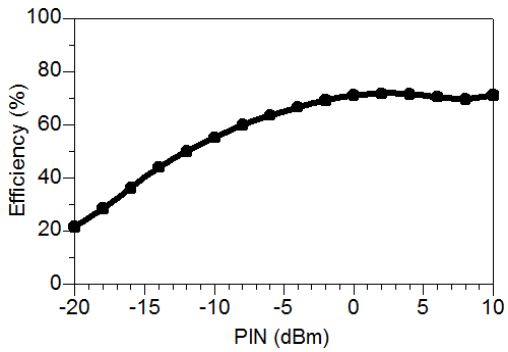
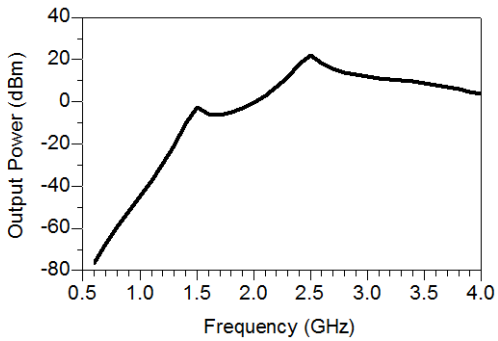


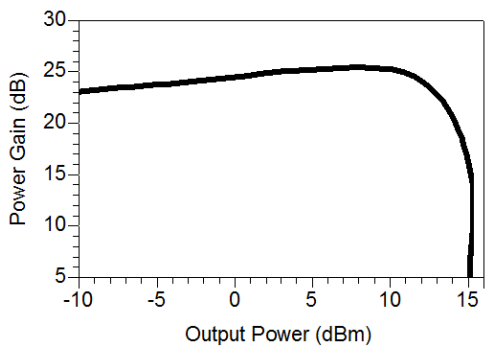
Fig. 9. Drain voltage and current waveforms of the RFPA



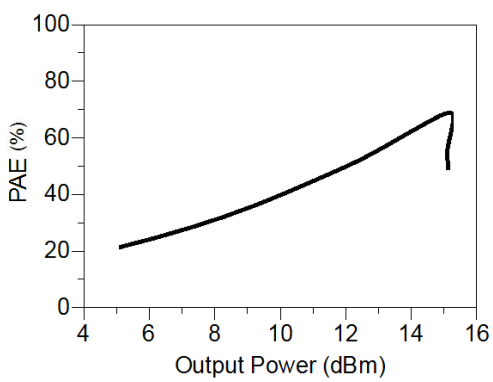
(*a*)



(*b*)



(*c*)



(*d*)

Fig. 10. Characterizations of the RFPA, (*a*) efficiency, (*b*) output power, (*c*) power gain, and (*d*) PAE

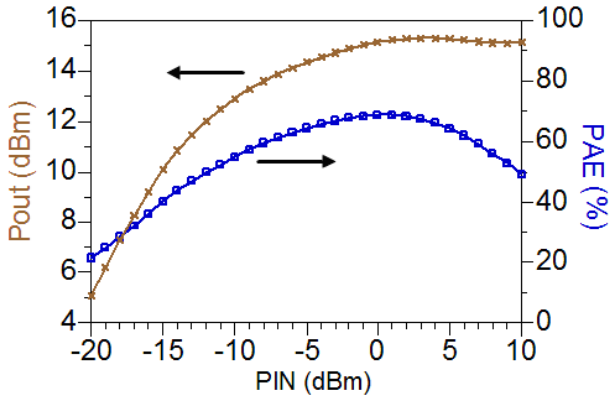
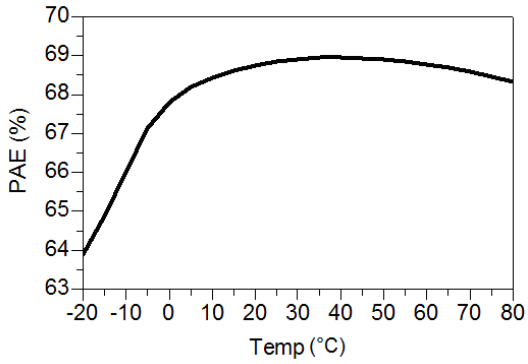
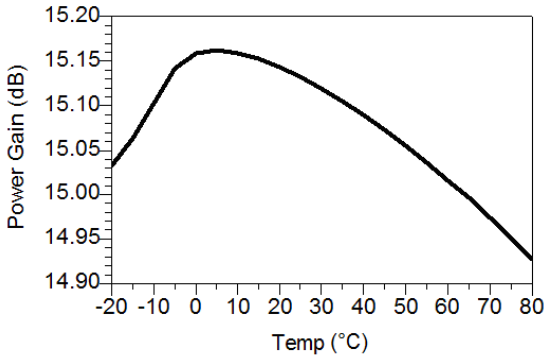


Fig. 11. Output power and PAE of the RFPA as a function of input power variations



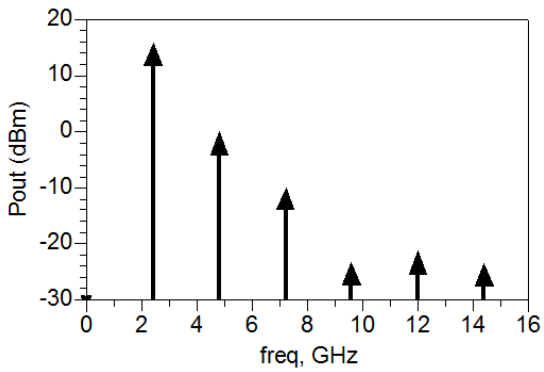
(*a*)



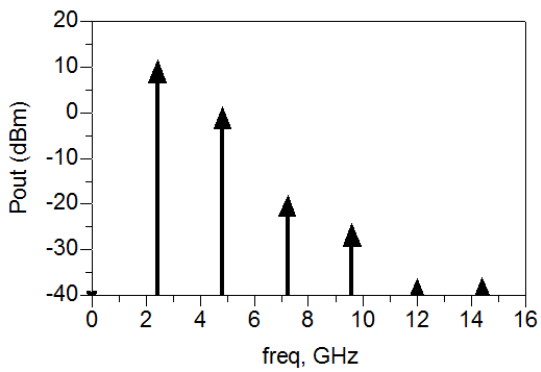
(*b*)

Fig. 12. Effect of temperature variation on (*a*) PAE, (*b*) power gain of the RFPA

In order to consider the effect of the active inductor on the RFPA nonlinearity, the output spectrum of the RFPA with active inductor-based output matching network is given in Fig. 13 in comparison with the case of using a passive spiral inductor in the output matching network of



(*a*)



(*b*)

Fig. 13. Output spectrum of the RFPA, (*a*) with active inductor-based output matching network, (*b*) with passive spiral inductor in the output matching network

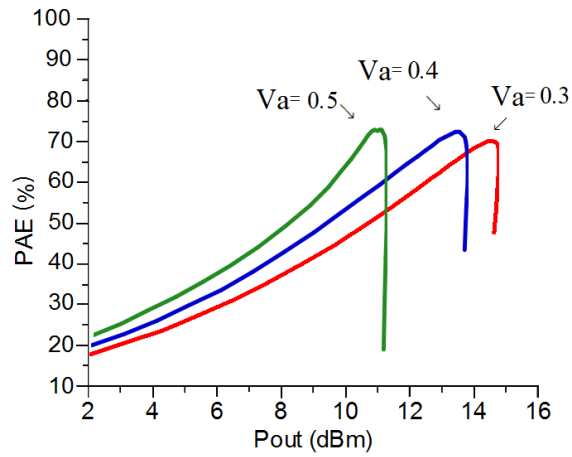
the RFPA. As it can be seen, the active inductor increases HD_3 of the overall circuit just by 3 *dB*. As a result, the utilized active inductor has no significant effect on the linearity performance of the RFPA.

In order to evaluate the tunability effect of the proposed active inductor-based tunable output matching network on the output power level control and PAE of the RFPA, Eq. (1) is rewritten versus active inductor L_P as (22), in which the product of C_S and L_P is considered constant according to the resonance frequency.

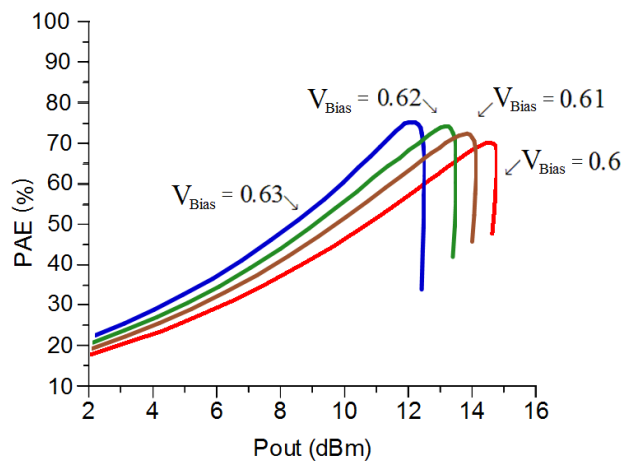
$$Z_{in} = R_{opt} = \frac{\left(L_P \omega_0\right)^2}{Z_0} \qquad (22)$$

As a consequence, at the constant operating frequency, the desired load resistance, and hence, output power level can be changed by considering different values for the tunable inductor. For this purpose, the inductance value has been increased in two ways by increasing the bias voltage of transistors M_3 or M_6 (V_a or V_{Bias} in Fig. 7).

Fig. 14 shows the PAE of the RFPA versus output power level for different values of the active inductor bias voltages. The results reveal that as the optimum load resistance increases by increasing the inductance value, the PAE peak moves from high power to low power levels without any degradation. Therefore, it is possible to retain the power efficiency at the same maximum level for lower input drive levels, whereas in the case of a fixed output matching network, the PAE will be degraded when the output power level moves down.



(*a*)



(*b*)

Fig. 14. Tunability effect of the proposed active inductor on PAE of the RFPA, the inductance value has been changed in two ways: (*a*) Changing V_a, and (*b*) changing V_{Bias}

Table III. Performance summary of the RFPA with active inductor-based output matching network in comparison with some works

Ref.	[3]	[17]	[18]		[19]	**This Work**
Data	Exp.	Pre-layout Sim.	Pre-layout Sim.	Post-layout Sim.	Sim.	**Pre-layout Sim.**
Freq. (GHz)	1.75	2.4	2.4		2.45	**2.4**
V_{dd} (V)	2	1.8	3.3		3.3	**1.5**
P_{in} (dBm)	---	0	16		+5	**0**
P_{out} (dBm)	15	21.1	26	23	24.1	**15**
PAE (%)	43	57	45	44.5	50.6	**70**
Area (mm^2)	-	-	0.37*		1.01	**0.52**

* This work used bond wires as inductors.

Performance characteristics of the proposed RFPA with active inductor-based output matching network in comparison with some other works [3, 17-19] are summarized in Table III. Although the output power of the proposed RFPA is lower than that in [17-19], its required input power is lower than [18, 19], while it has reached to a maximum PAE of 70%.

4. Conclusion

An active inductor-based *T*-type high-pass tunable output matching network with a new structure of CASFAI active inductor for a class-E RFPA is presented in order to control the output power and enhance the efficiency. The performance metrics of the designed CASFAI indicate that it behaves as an inductor in the frequency range of 0-6.9 *GHz*, and has reached to a maximum quality factor of 4406, inductance value of 7.56 *nH*, 3rd order harmonic distortion better than –30 dB for 0 *dBm* input power, while consumes only 2 *mW* power. To evaluate the tunability performance of the proposed CASFAI-based tunable output matching network on the output power level and PAE of RFPA, it is applied as a variable inductor to the output matching network of RFPA and the overall circuit is validated in ADS in a 0.18 µ*m* CMOS process and 1.5 *V* supply voltage. The results indicate that by increasing the inductance value of the matching network in constant operating frequency, the PAE peak moves from high power to low power region without any efficiency degradation, and hence, it is possible to maintain the power efficiency at the same maximum level for lower input drive levels.

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*Rebuttal Letter

Answers to the Reviewers' Comments

The authors would like to express their genuine appreciation both to the editors in charge of the paper and to the reviewers for their thorough and constructive comments. We have taken all of them into account and modified the paper accordingly. In the following, the answers to particular comments are shown in line:

Reviewers' comments:

Reviewer #1:

I would like to thank the authors for kindly answering the points I raised. Unfortunately, this reviewed version does not clarify the main issues of the first version. My main concerns are:

1 – Linearity

The inductor is at the circuit's output. The signal swing in considerably high and the active inductor is performing under large signal condition. The current in M2 and M1 is highly distorted.
In the manuscript, the authors bring a small signal analysis (Taylor series expansion) announcing it as if it were large signal analysis ("... the large signal input current of the inductor, Iin , should be determined as a nonlinear function of the input voltage, Vin . By using a Taylor series expansion and considering the first three terms, Iin versus Vin can be derived as follow ...").

R) Thank you. As it is mentioned by the valuable reviewer, the signal swing applied to the active inductor input port (Vin) is high. As a result, the input current of the inductor (Iin, a combination of the drain currents of M1 and M2) is a nonlinear function of Vin. Since, using the Taylor series expansion is one way to model the nonlinear expression [R1-R6], this method has been used in the revised version to have a hand-calculating observation. Finally, a large signal S-parameter simulation was done to show the nonlinearity of the active inductor. Additionally, the text stated above has been modified.

[R1] B. Kim et al., "A New Linearization Technique for MOSFET RF Amplifier Using Multiple Gated Transistors," *IEEE Microw. Guided Wave Lett.*, vol. 10, no. 9, pp. 371-373, Sept. 2000.
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Then, in Fig. 5, the author plots the result of a "large signal S-parameter simulation" (no frequency is informed, I assume it is 2.4 GHz) and he says the circuit starts to distort after 8 dBm. So, what is the criterion for recognizing distortion? Visual? Moreover, if in Table II the performance is defended with Pout of 15 dBm, the circuit is largely nonlinear (the recognized it performs badly after 8 dBm)!

R) Thank you for your thorough comment. The frequency is the same 2.4 GHz. Indeed, there is no standard method to find the compression point from the variation of S11. Hence, the mentioned power is visual. Actually, it is indicated in the paper that the active inductor starts to distort from 8 dBm input power. However, as is can be seen in Fig. 5, the deviation of the real part of S11, is around 0.5 dB and that of the imaginary part of S11 is less than 0.06 dB for 0-15 dBm power range. As a result, the circuit will not fall into a large nonlinearity at 15 dBm output power. In order to confirm this issue, the output spectrum of the active inductor-based RFPA was added to the paper in comparison with the case of using passive spiral inductor in the output matching network, which indicates that the active inductor increases the HD3 of the overall circuit just by 3 dB.

2 - Fig. 5 brings again the result of the inductor S11 versus Pin. Again, it makes no sense at all. DO the authors mean Available power from a 50 ohms power source? Because, since the inductor is ideally a pure reactive device, it consumes 0 w power (theoretically).

R) Yes. A 50 ohms power source was applied to the inductor to perform LSSP.

3 - In the authors' reply, they said the class-E design is straightforward. Well, I am not so confident. We do not find too many CMOS integrated class-E PA. Commonly, there are lots of concerns regarding the MOSFET switch, the drivers, the inductors quality factor, the parasitics and so forth. The layout looks like a small signal amplifier. Well, 30 mW is not too much power, but it is high enough for a painful headache. So, I would like to learn from the authors about the amplifier design. At least the device sizes are welcome.

R) Thank you. The overall circuit parameters are included in the revised version of the paper.

4 - The authors claim in the reply they did post-layout simulations. I would like to see PVT simulations as well. As well as the time waveforms and how all the simulations were done. Which methods were used? Harmonic Balance? Transient? How the authors guarantee the circuit is operating in class-E? Only time domain simulations can show it.

R) Thank you. The time domain waveforms of the drain voltage and current of the transistor was added to the paper, which indicate that the amplifier operates in Class-E mode. Additionally, the effect of temperature variations on the PAE and power gain of the RFPA was added to the paper.
About the simulations, indeed, S-parameter, transient, harmonic balance (HB), large signal S-parameter (LSSB), and DC simulations are used for various specifications.

5 - I have never seen a class-E PA with no driver and matched to 50 ohms. It is very strange.

R) Thank you for your comment. Usually, a class-F or another class-E amplifier is used as a driver stage.
Actually, the main emphasis of the paper was on using the active inductor as a tunable element in the output matching network of a RFPA. As a result, a driver stage is not considered for the RFPA.

6 - The reference regarding the class-E equation is not appropriate. In [15], they reproduce the equations from Grebennikov's paper.

R) Thank you. The reference was added.

Reviewer #2:

Thank you for the revised version of your work.
In my opinion it is suitable for publication with the updates provided by Authors.

R) Thank you for your constructive comments.

Reviewer #3:

1. Authors have included the layout; however authors did not show the post-layout simulation results to be compared with pre-layout simulation results.

R) Thank you for your comment. Actually, the layout was checked from the design rule checking (DRC) point of view. The extraction was not performed, since inductors could not be extractable by the used simulator. As a result, the data was based on pre-layout simulation.

2. In the Table II, Data must be clearly specified either Exp. data, post-layout data or pre-layout data. PAE of 70% may be from pre-layout simulation and hard to get when do the post-layout simulation.

R) Thank you. The comment was performed.

***Highlights (for review)**

The use of a new CASFAI in a tunable matching network of a class-E RFPA is presented. The designed CASFAI behaves as an inductor in the frequency range of 0-6.9 *GHz*. It has reached to a maximum quality factor of 4406 and inductance value of 7.56 *nH*. The CASFAI is applied as a variable inductor to the output matching network of RFPA. The overall circuit is validated in a 0.18 µ*m* CMOS process and 1.5 *V* supply voltage.