Mitigation strategies of the variability in 3T1D cell memories scaled beyond 22nm

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Abstract—**3T1D cell has been stated as a valid alternative to be implemented on L1 memory cache to substitute 6T, highly affected by device variability. In this contribution, we have shown that 22nm 3T1D memory cells present significant tolerance to high levels of device parameter fluctuation. Moreover, we have observed that the variability of the write access transistor has turn into the more detrimental device for the 3T1D cell performance. Furthermore, resizing and temperature control have been presented as some strategies to mitigate the cell variability.**

Keywords- variability, DRAM, temperature

I. INTRODUCTION

Currently, the variability influence on device behavior is well reported as one of main drawbacks for electronic devices in nanometer regime [1], since it leads to a worsening system behavior. Several types of variability coexist, but random doping fluctuation (RDF) has the largest impact on device performance [1] as it causes the largest threshold voltage (V_T) fluctuation. Indeed, memory systems are obviously affected by this variability, and the well established 6T-SRAM cells [2], [3] are highly influenced, because a relevant performance lost is manifested in speed reduction and cell instability [3], [4]. In this sense, the 3T1D-DRAM is a promising memory cell to substitute it in VLSI systems. Although, this cell is also affected by the process fluctuations, they do not necessarily impact the operating frequency, unlike 6T [3]. Moreover, 3T1D provides extra benefits: smaller cell area, non-destructive read process (in contrast to other DRAMs), and large retention time. Thus, the 3T1D-DRAM cell is presented as a suitable memory cell for L1 memory caches [3]. In this context, fast access times are required and low retention times are architecturally masked. Note that 3T1D cell is a Dynamic RAM, thus, the memory storage node is a capacitor (the gate capacitance in the gate-diode) and it stores temporarily the data. In order not to lose the contents, a periodic refresh is required to hold data for extended periods [3]. On the other hand, the constant dimension reduction of technology nodes produces an intolerable increase of leakage current and electric field present in devices. This implies lower carrier mobility and worse reliability [5]. To overcome this problem, the introduction of high-k dielectrics is a real option and it has also allowed a better 3T1D performance beyond 65nm technology node [2] due to the reduction of the leakage currents.

As a consequence, this work performs an analysis of the variability influence on 3T1D cells for technologies beyond 22nm node. So the, this work is organized as follow. Section II presents the cell scheme and its main parameters analyzed along this work. Section III illustrates the influence of the device variability on 3T1D-DRAM cell. Finally, Section IV reports some strategies to mitigate the memory cell variability.

II. EXPERIMENTAL WORK

The schematic structure for a 3T1D memory cell is shown in Fig. 1. This cell has been simulated using the 22nm High Performance Predictive Technology Model (HP PTM) [6] based on high-k materials as a gate dielectric. The optimal dimensions of all the cell devices have been extracted from [4] and a supply voltage (V_{DD}) of 1V has been applied. For comparison, the 3T1D memory cell has been also simulated using 16nm HP PTM [6] and 13nm TRAMS project model [7]. All the studies focus on the following 3T1D cell parameters:

a) Write Access Time (WAT) defined between $V(WL_w) = 0.5*V_{DD}$ and $V(S)=0.9*(V_{DD}-V_T)$.

b) Read Access Time (RAT) defined between $V(WL_w) = 0.5*V_{DD}$ and $V(BL_r)=0.9*V_{DD}$.

c) Dynamic Power consumption (PW) obtained by the average value along one cycle

d) Retention Time (RT) that it is the time required for the storage node voltage (V_S) in the cell to decay to V_{Smin} [8], that it is assumed as our reference parameter to analyze the cell performance.

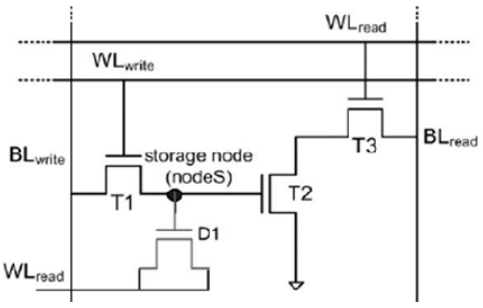

Figure 1. Schematic structure for a 3T1D DRAM memory cell.
WL: wordline BL: bitline

In order to study the impact of the devices fluctuation on the 3T1D cell parameters, 10000 Monte Carlo simulations have been performed. The variability influence has been reflected into a variation of the threshold voltage of the devices on memory cell [5]. Table I depicts the variability levels assumed along this work for all the technology nodes, following TRAMS project statement [9]. The Gaussian distribution will be spread as the variability level rise and for all the tables the fluctuation will be analyzed by the 3σ/μ ratio, expressed in percentage.

TABLE I. VARIABILITY SCENARIOS CONSIDERED FOR EACH TECHNOLOGY NODE.

Levels	22nm	16nm	13nm
Moderate (M)	8%	10%	X
High (H)	15%	20%	X
Very high (VH)	30%	40%	58%

III. VARIABILITY INFLUENCE ON 3T1D-DRAM CELLS

To analyze the influence of device parameters fluctuation (V_T-variation) on the performance of a 22nm 3T1D memory, we simulate different variability levels and compare to a non-variability scenario (Ref). Fig. 2 shows how the different level of fluctuation affects the retention time performance, the wider distribution the largest influence. In this sense, the very high process variation level (VH) presents the largest impact in the analyzed cell parameters and RT is the one subjected to highest variability relevance.

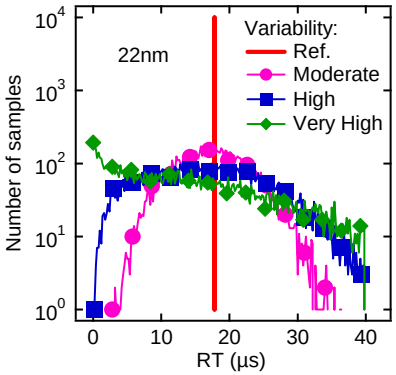

Figure 2. Influence of the variability on cell performance represented by RT results. The largest fluctuation level means higher impact on cell behavior. These results are obtained for 22nm cell devices, but similar effect is observed for smaller technologies.

In order to analyze in depth the previous results, we also study the impact produced by the variability of each individual transistor on the global circuit behavior. For instance, the scenario has been defined in a 3T1D cell based on 22nm devices with a moderate variability. To do this, we introduce V_T-fluctuation to just one cell device at a time, keeping the other ones without variability. Fig. 3 compares the global process variation obtained for the retention time, when all devices endure same variability level (line) and when only one cell device fluctuates (line+symbols). In this sense, we observe that the overall cell fluctuation is highly influenced by T1, since this exhibits the widest distribution (highest impact). Furthermore, Table II depicts the variability relevance of each device on cell parameters and the highest T1 impact on RT is confirmed, along with a high impact of T1 and D1 on WAT. Hence, the variability on T1 presents the highest impact on the overall cell performance, since it alters the two main 3T1D cell parameters (WAT and RT).

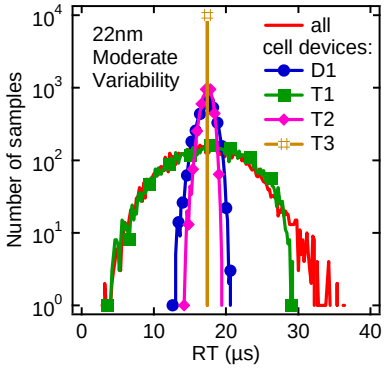

Figure 3. Influence in RT of each individual transistor on the global cell performance, based on 22nm, under a moderate variability. The impact of each device's fluctuation (line+symbols) is compared with the observed when all devices presents the same variability level (line).

TABLE II. INFLUENCE OF EACH 3T1D CELL TRANSISTOR VARIABILITY ON GLOBAL CELL BEHAVIOR.

3σ/μ (%)	T1	T2	T3	D1
WAT	3.6	0.8	0	4.1
RAT	0.2	0.1	4	0.1
PW	0.1	3	1.1	0.8
RT	27.6	4.6	0	4.6

The variability impact on different technology nodes (22nm, 16nm and 13nm) is studied in the following paragraphs. But, first, we have observed that when the technology node is reduced below 22nm and a very high variability level has been assumed, 4% of the samples become inoperative, as it is shown in Fig. 4. These samples present a large variability on T1, since V_{T1} is reduced to very low values [8], and as a consequence V_S discharges. Thus, storing logic '1' is impossible (i.e. cell fault). For 16nm and 13nm, T1 has shown again a high influence on 3T1D cell performance, and it seems to be more critical on the cell behavior than the gated diode [2] for the sub-22nm nodes. To demonstrate it, Fig. 3b shows V_S evolution for a 3T1D cell based on 13nm node when a high variability is introduced only at one device at a time. In this context, we observe that T1 device is the only one that involves the 3T1D final bad performance, since the other cell devices (T2, T3 and D1) do not present any faulty behavior. This confirms that the write access transistor (T1) presents a high influence on the global 3T1D cell performance.

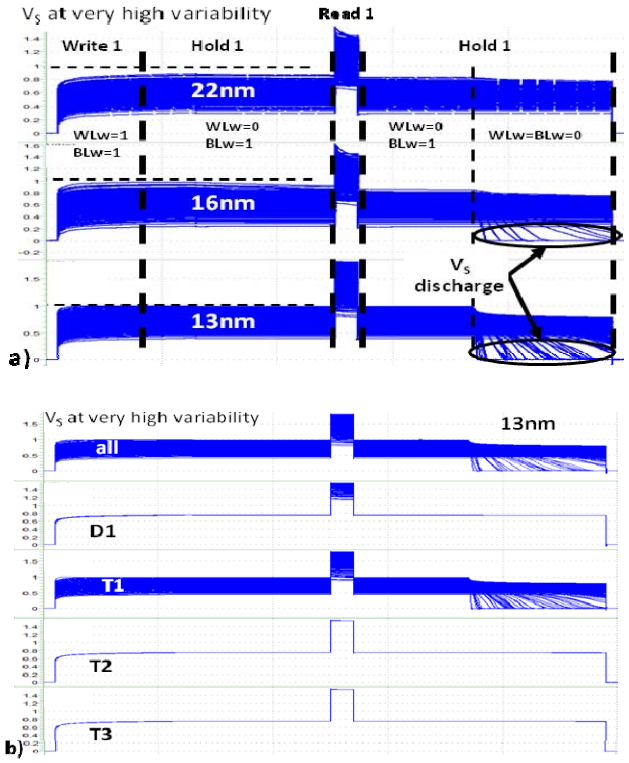

Figure 4. V_S performance obtained from Monte Carlo simulations at two scenarios: (a) when a 3T1D cell, based on 22-16-13nm nodes, is subjected to a '1' write operation. A cell malfunction is observed for the smaller nodes when WLw and BLw are not activated and V_S discharge is obtained, due to the small V_{T1} value [8]. (b) when very high variability level only affects one at a time of the 3T1D cell devices, based on 13nm node. T1 is the only one that presents a cell malfunction, since the other devices show no significant influence.

So then, taking away the faulty cells, Table III shows the impact of variability in sub-22nm memory cells. The results depict a high increase of the variability impact as the technology node is reduced, as it is expected, and retention time gets the biggest hit.

TABLE III. VARIABILITY IMPACT ON 3T1D-DRAM CELLS FOR DIFFERENT TECHNOLOGY NODES. SMALLER NODE LARGER PARAMETER VARIATION.

3σ/μ (%)	Moderate (M)		High (H)		Very high (VH)		
	22nm	16nm	22nm	16nm	22nm	16nm	13nm
WAT	5.5	6.8	10.4	16	23	40.6	47.3
RAT	4	6.7	7.8	16.9	19.8	32.9	37.9
PW	3.3	4.4	5.8	10.7	11.3	19.9	22.2
RT	29.3	33.2	48	59.3	79	101	130

IV. MITIGATION TECHNIQUES TO REDUCE VARIABILITY

The process variability has been shown to be a detrimental factor for sub-22nm 3T1D cells. In this sense, variability mitigation strategies are necessary, and thus, in this work, we present two solutions in the following sections.

A. *T1 resize to mitigate cell variability*

In order to mitigate the 3T1D memory variability, and also reduce the previous observed cell malfunction, one option could be increase the dimensions of T1, since we have previously determined as the most critical cell device. Then, an upsizing of T1 dimensions could reduce the variability impact on the cell performance [10]. Consequently, we have assumed the well-known higher impact of the width resize on device performance [11] to be only implemented on T1. Therefore, the width of cells based on 22nm and 13nm nodes will be enlarged by x2 and x4. Table IV shows that this slight device area increase has involved very promising results for both technology nodes. Since the variability impact on 3T1D cell behavior has been reduced for both, with larger improvement (lower fluctuation) for the 13nm cells. All the analyzed parameters present an improvement, but the highest remarkable reduction of variability impact is shown for the retention time. In particular, at very high variability level a 13 and 24% improvement is achieved respectively for both technologies. Thus, a modification of T1 width is a feasible option to mitigate the impact of the variability on 3T1D cells.

TABLE IV. VARIABILITY IMPACT ON A 3T1D CELL PERFORMANCE, FOR 22NM AND 13NM TECHNOLOGIES, WHEN T1 WIDTH (W) IS MODIFIED. LARGER T1 WIDTH RESULTS IN A LOWER VARIABILITY IMPACT.

3σ/μ (%)	22nm						13nm	
	Moderate		High		Very high		Very high	
	2W	4W	2W	4W	2W	4W	2W	4W
WAT	5.3	5.4	10.1	9.6	21.8	20.3	45.2	42.1
RAT	4	4	7.9	7.9	18.8	19	32.2	32.1
PW	3.1	2.5	5.5	4.9	11.2	11.3	18.8	15.7
RT	20.5	16.5	37.7	31.6	71	65.6	110.1	96.4

However, this would suppose a slight increase of area. This performance improvement also is also explained by the higher mean value (μ) obtained and similar standard deviation (σ), what involves a final lower variability impact on 3T1D behavior. Moreover, the previously observed cell malfunction (section III) caused by the bad performance of T1 on the sub-22nm nodes is highly reduced (<1%).

B. *Temperature influence on cell variability*

On the other hand, the environment temperature is always a relevant factor that influences the circuit performance and its impact on variability has been analyzed, as well. Table V studies the impact of high temperatures (100ºC) on 3T1D cells performance based on 22nm and 13nm nodes and different variability levels. Comparing with room temperature results (Table II), we observe a similar influence on RAT and PW values, whereas RT presents a high increase. This is caused by the V_{Smin} dependence on working temperature that directly affects the leakage current [8]. In particular, higher temperature is more detrimental for the smallest technology node, where an

increase of the variability impact on the retention time around 30% is observed. Additionally, WAT shows a slight enhancement, due to the lower variability impact.

TABLE V. VARIABILITY IMPACT ON 3T1D MEMORY CELL FOR 22 AND 13NM TECHNOLOGY NODES AND FOR ALL VARIABILITY LEVELS AT 100º. WORSENING PERFORMANCE AS THE TEMPERATURE RISES UP IS OBSERVED.

3σ/μ (%)	22nm			13nm
	Moderate	High	Very high	Very high
WAT	4.4	8.3	18.4	47.8
RAT	4.2	8.3	20	34.4
PW	3.2	5.7	11.6	24.7
RT	40.5	69	101.6	204

V. YIELD AT MEMORY BLOCK ARCHITECTURE

For a more realistic analysis, we have also computed the manufacturing yield of a 2kB cache memory block based on 3T1D cells. The circuit has been evaluated with a reconfigurable array of 32 cells per column, 512 columns and 24 redundant columns following [12]. For yield analysis, a 3T1D-DRAM cell with a retention time lower than 714ns is regarded as faulty. This time criteria ensure that the performance (IPC) loss in a system with 3T1Ds will be only 2% when comparing with an ideal 6T design [3]. Thus, Fig. 5 shows yield simulations for (a) 3T1D memories based on 22nm for a single cell, (b) a 22nm memory block and (c) sub-22nm one. Fig. 5a shows that, at cell level, more than 90% yield is achieved for 22nm cells in front of any variability scenario. On the other hand, Fig. 5b points out that the 90% yield of 2kB memory blocks on 22nm cells can be achieved only with moderate and high variability levels, showing a good performance of the simulated 3T1D cells. Finally, Fig. 5c shows that for the smaller technology nodes the performance is more pessimistic, since only for 16nm cells the moderate variability is able to meet the time criteria.

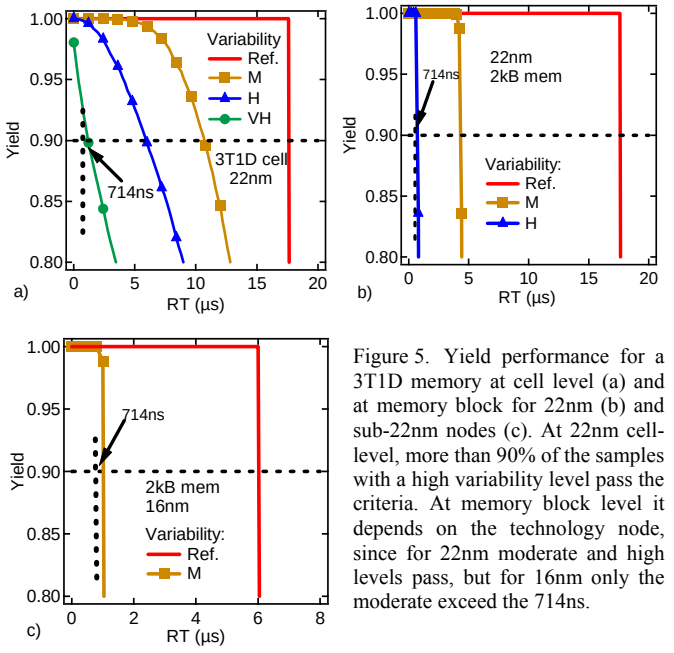

Figure 5. Yield performance for a 3T1D memory at cell level (a) and at memory block for 22nm (b) and sub-22nm nodes (c). At 22nm cell-level, more than 90% of the samples with a high variability level pass the criteria. At memory block level it depends on the technology node, since for 22nm moderate and high levels pass, but for 16nm only the moderate exceed the 714ns.

To complete this analysis, Fig. 6 presents the performance of memory blocks based on 22nm devices when the two mitigating scenarios are assumed. In this sense, Fig. 6a presents a relevant yield improvement when T1 width is enlarged at moderate and high fluctuation level, since larger retention times are obtained. So then, upsizing T1's width improves the cell performance. On the other hand, Fig. 6b points out a clear yield reduction when the system temperature is raised up to 100ºC. Showing that the system only fulfills the time criteria for a moderate variability level. For this, a control of the environment temperature is very important to reduce the variability impact.

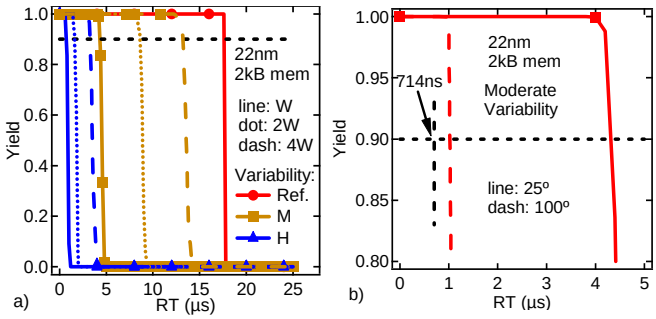

Figure 6. Yield performance of 2kB memory blocks based on 22nm 3T1D cells, when (a) T1 width is resized up and (b) the environment temperature is raised up. First, the enlargement of T1 width shows that the 90% of the memory blocks have larger retention times, improving, then, the cell performance. Meanwhile, for higher temperatures the 3T1D cells present a worsening behavior, since now the 22nm system only fulfill the retention time criteria under a moderate variability level.

VI. CONCLUSIONS

The 3T1D cell performance is analyzed under different variability scenarios. First, the device fluctuation analysis has pointed out that the effects of variability on write access transistor (T1) have the highest impact on circuit performance, becoming the critical cell device at reliability level.

In order to mitigate the observed cell variability several strategies has been presented and a) resize the width of the write access transistor, T1, has resulted in a relevant improvement of the cell tolerance to the device variability, and b) environment temperature has presented a cell worsening when is raised up, so, a control and reduction of the cell temperature has to take into account to reduce the device variability impact.

Moreover, the cell fluctuation on a 2kB memory block based on 22nm 3T1D cells has shown a yield larger than 90% for moderate and high variability levels, this means a better process variation tolerance than in the case of 6T cells.

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