Reliability issues in RRAM ternary memories affected by variability and aging mechanisms

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***Abstract*—Resistive switching Random Access Memories (RRAM) are being considered as a promising alternative for conventional memories mainly due to their high speed, scalability, CMOS compatibility, Non-Volatile behavior (NVM), and consequent orientation to low power consumption. Advances in the RRAM technology as well as enhancement of the control of the cells are opening the use of these devices for multi-valued logic. But the cycle-to-cycle variability and the still reduced endurance are becoming serious limitations. This paper analyzes the impact of both mechanisms on 1T1R cells and suggests potential adaptive mechanisms to enlarge its lifetime.**

Keywords—RRAM devices, ternary memories, variability, endurance, aging, adaptive mechanisms.

I. INTRODUCTION

Resistive RAMs (RRAMs) are ceaselessly displacing conventional Flash memories in such a way that they have already been reported devices with 32 and 16Gb [1,2] of storage capacity. Together with the scaling limitations of floating gate transistors, it is the excellent characteristics of emerging devices such as higher density, good scalability and compatibility with CMOS that causes this pressure. RRAM devices work at lower voltages (in comparison with flash cells) and keep a robust non-volatility and fast operation. Among a large list of metal oxide materials, the more deeply demonstrated cells are based on HfO_2 and TiO_2. With the maturity of technology, it is being demonstrated the possibility to include more than two levels of resistance state in a single cell enhancing consequently the memory density of potential modern memories to multi-valued. Fig. 1(a) shows the sandwiched (MIM, metal-insulator-metal) structure of a RRAM. Those devices exhibit a memristive behavior. The switching event from high resistance state (HRS) to low resistance state (LRS) is referred as the *Set* process. When fresh devices are considered this process requires higher voltage and power and it is referred as *electroforming*. After oxygen vacancies filaments are created (Fig. 1 (b)) the conductive device requires lower voltages and energy to switch from low resistance to high resistance (*Reset* process, Fig, 1 (c)) or the reversible *Set* process, cycle after cycle. Fig. 2 (a) shows the characteristic of a memristive device with set and reset voltages around 1.5V and -1V respectively. When a limitation in the current (current compliance, I_C) in the resistance switching is applied (usually thanks to the typical crossbar 1T1R cell, where the transistor actuates as switch and current limiter) it is possible to get intermediate states as are demonstrated in Fig. 1(c) and Fig.2 (a). This is the basis of the ternary variables (or multi-valued in general) storage in those cells. One of the drawbacks of these devices is the extraordinary and uncontrollable stochastic variability of the switching mechanism as it can be seen in Fig 2(b) where 10 contiguous cycles are displayed. This causes a random behavior on the set and reset voltages as well as on the values of the three levels of resistance considered (LRS, IRS, HRS). In Fig. 2(a) we get three levels of resistance (reading voltage +0.5 volts): 10kΩ, low state (LRS, current compliance 100μA), 100kΩ, intermediate state (IRS, current compliance 10 μA) and 7MΩ, high resistance (HRS, current compliance 0.8 μA).

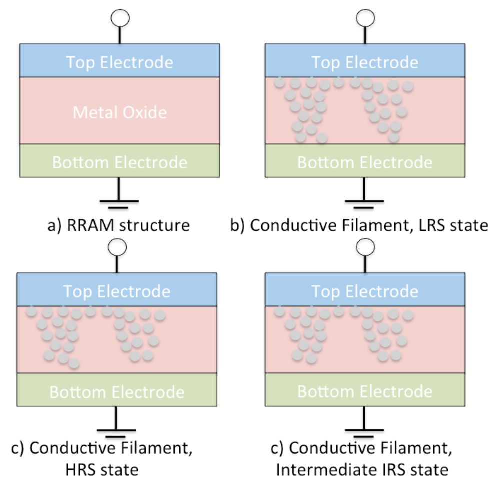


Fig. 1. Structure of RRAM and conductive filaments for three different states

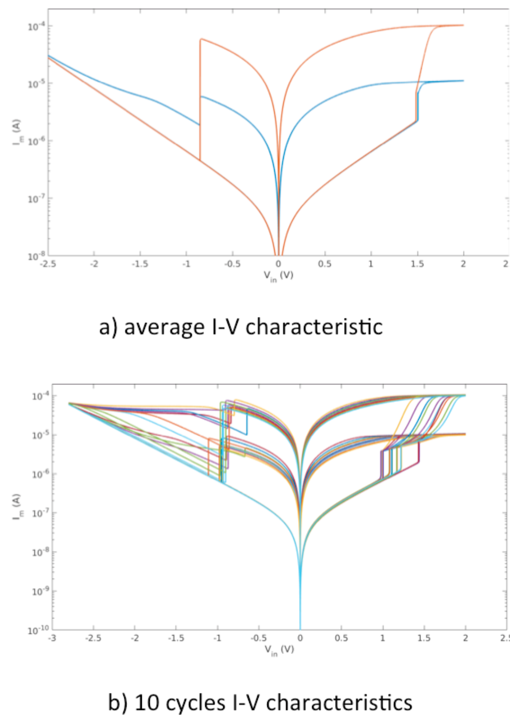


Fig. 2. Example I-V ternary characteristic, a) average value, b) 10 cycles.

In section II we introduce the device and model used in the work as well as the description of conductive and stochastic characteristics. We will introduce the level of cycle-to-cycle variability as well as the impact on reading stability. Section III introduces a well-known model of endurance limitation and the impact of that mechanism on the cell reading reliability will be analyzed. In section IV we show that it is possible to use some of the programming variables to palliate this impact. In section V we discuss and conclude the application of such an analysis to mitigating strategies to enlarge lifetime of the memory.

II. CYCLE-TO CYCLE VARIABILITY

In this section, we will use the Verilog-A/Spice compact model generated by the group of Stanford SystemX Alliance [3]. This model, contrasted with experimental measurements, follows a physical model of a single filament path RRAM including quantum behavior, temperature-dependency and stochastic cycle-to-cycle behavior. I-V characteristic displayed in 2(a) and 2(b) has been obtained from that model. Fig. 2(b) shows the cycle-to-cycle variability levels; in the figure only ten contiguous cycles are

displayed. With a larger number of samples, the variability and the statistical data obtained for the resistance variability of LRS, IRS and HRS are:

TABLE I. CYCLE-TO-CYCLE VARIABILITY CHARACTERISTICS

Level	Mean (kΩ)	Deviation, σ, (kΩ)
LRS	10	1
IRS	100	40
HRS	7e3	4e3

Observe the relative variability for LRS, IRS, and HRS states are 0.1, 0.4 and 0.6 respectively, the variability of HRS and IRS states are higher than LRS [3]. The relative variability increases at decreasing I_C, which can be explained as the decrease of the number of vacant in the filament [4]. Fig. 3 shows the resistance distributions in a logarithmic resistance axis.

In order to discriminate the stored state a window comparator is required with two threshold resistance references, one between LRS and IRS (-1 and 0) and other between IRS and HRS (0 and 1). The selected resistances Rref1 and Rref2, respectively, have a critical effect on the reading robustness through the probability of reading error, Pe. Fig. 3 shows the appropriated resistance ranges for those references. Rref 1 range between 25 and 35 kΩ,and 100kΩ to 2.5MΩ for Rref2.

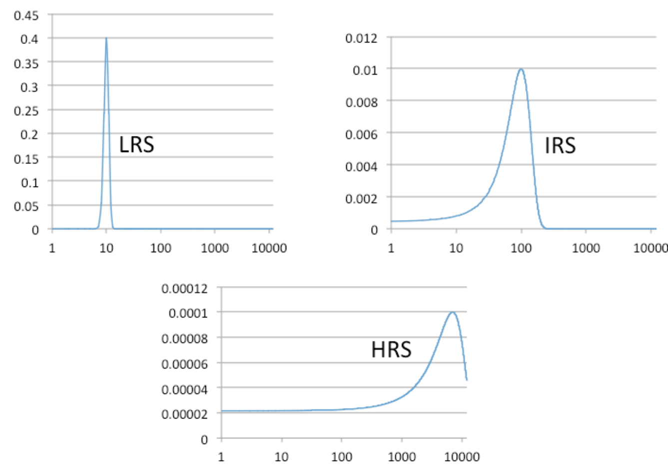


Fig. 3. Resistance distribution for the states LRS, IRS and HRS due to cycle-cycle variability. Horizontal axis in kΩ.

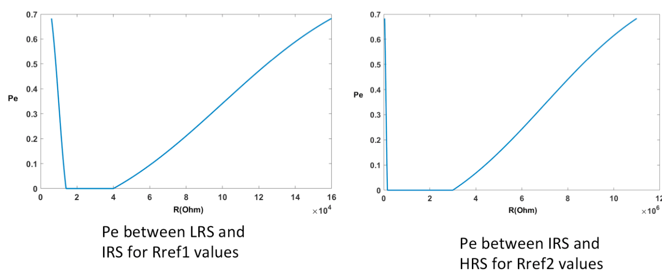


Fig. 4. Probability of reading error due to resistances variability showing the range of right threshold resistances.

III. ENDURANCE MODEL

Fig. 5 shows the effect of aging after a high number of operational cycles, phenomenon that causes a limitation in endurance [5]. This aging model indicates a gradual reduction of the HRS (and IRS) levels with cycling operations. This implies a shift of the HRS, IRS resistances distribution to lower values (to the left in Fig. 4) causing a drop in the discriminability of states and consequently an increase of Pe. The aging also spreads out the resistance distributions. Applying this model to our circuit after 10^6 cycles the new variability levels are shown in Table 2.

Fig. 5 Degradation model showing the depletion of O^2 induced HRS reduction [5].

As a consequence, the range of reference resistances becomes narrower increasing the reading error probability Pe. After 1 million of cycles the new range of resistance resistances take the value: Rref1 between 18kΩ and 20kΩ and between 200kΩ and 1MΩ for Ref2. This reduction can be understood as a decrease of the cell reading robustness, attempting reliability.

TABLE II. CYCLE-TO-CYCLE VARIABILITY CHARACTERISTICS AFTER 10^6 CYCLES AGING

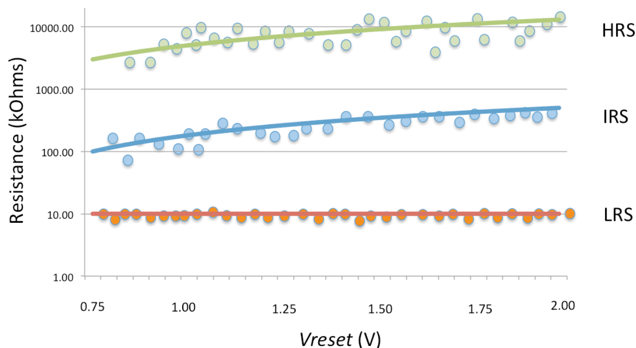
Level	Mean (kΩ)	Deviation, s, (kΩ)
LSR	10	4
ISR	70	50
HSR	5e3	5e3

IV. A MITIGATING APPROACH FOR RRAM VARIABILITY

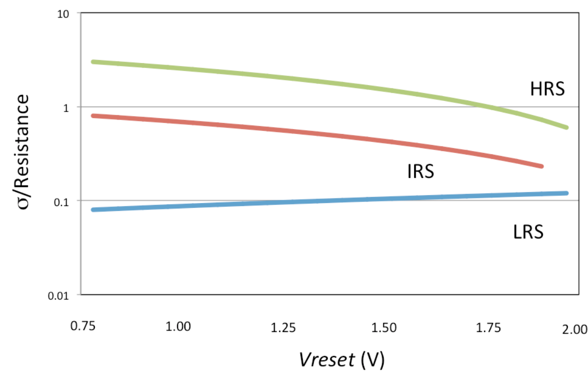
In the previous sections, for brevity reasons we have only mentioned the impact of the current compliance on the resistance state. The results presented in the precedent sections correspond to a set voltage of 1 volt and a reset voltage of -1 volt, in form of a 10μs pulse. These three variables (pulse width and reset and set levels) affect also the switching behavior (as well as temperature). In this section, we point out that one of these variables can be used to compensate the aging effect. This variable is the reset voltage, *Vreset*. It has been presented in [4] and [6] that the HRS distribution is strongly affected by *Vreset*. As *Vreset* increases the mean value of HRS resistance increases while the relative standard deviation decreases. This is just a compensating effect [7] of the aging mechanism. Physical justification of such effects can be found in [4,6]. We have simulated this effect and we observe a verification of such effects. Fig. 6 shows the results, a change in *Vreset* from -1 to -1.75 volts causes a significant increase in the mean resistance and a decrease in the standard deviation of the HRS and IRS resistance distributions, compensating aging.

V. DISCUSSION AND CONCLUSIONS

RRAM memories offer a vast range of advantages in front of other types of memories. Technology progress point out the possibility to store ternary or multi-valuated data in these devices. The principal drawbacks are cycle-to-cycle variability and endurance limitation due to aging. Variability requires an adequate reading circuit in order to avoid failures. But even designing with this rule aging causes a degradation of the distributions, fact that decreases reliability. Operational parameters, like the reset voltage level could be used to introduce compensating mechanisms alleviating the aging and enlarging lifetime.



a) Effect of *Vreset* on mean resistance value



b) Effect of *Vreset* on the relative variability of resistance

Fig. 6 Simulated impact of *Vreset* in mean and relative variability.

ACKNOWLEDGMENT

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